PROTECTION MADE SIMPLE.

SEG electronics

HighPROTEC

MRU4

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Build 63222

Revision A

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1 About This Reference Manual

This document is a reference of all the Setting Values, Direct Commands and Signals of the MRU4. In other words, it lists all parameters that are available (or can be made available) with the (optionally) full featured versions of the MRU4 protection device.

CAUTION!

This document does not intend to give long and/or detailed description, nor does it intend to replace the full Technical Manual in any way. Only a quite short description is given for each parameter.

This document is a reference of all the Setting Values, Direct Commands and Signals of the MRU4.

Every HighPROTEC protection device operates using a lot of digital values of various types. Throughout our Technical Documentation, we are talking of “settings” (or “parameters”) or “signals” or “(measured) values”, depending on the type.

Please consult the Technical Manual, in particular Chapter “Modules, Settings, Signals and Values”, for details of the existing data types.

Modules

The firmware of every HighPROTEC protection device can be thought of being sub-divided in several independent function blocks, the so-called “modules”. Every protection function, for example, is a module of its own. But one of the fundamental concepts of a HighPROTEC protection device is to implement this with great consequence.

There is even a general protection module (named »Prot«) that interacts all specific protection modules.

Every parameter, every value and every signal is therefore a member of some module.

But note that the settings dialogs (on the panel (HMI) or in the *Smart view* operating software) often omit the module name whenever it is clear from the menu branch. This means the parameters are often displayed only with their individual parameter names, i. e. simply *»Function«* instead of the full-blown *»I2>[1] . Function«*. This increases the overview and simplifies all configuration and operation work; however, it is good to know that the writing *»Function«* is just an abbreviation. In fact, **every** parameter **always** belongs to a module, and therefore – to make this concept absolutely clear – the reference tables have always the module name added in front of every parameter name

Especially for protection functions it is often required to have several instances active. For example, overcurrent protection usually has several “stages”, and all of these are running at the same time (using their individual setting values). Therefore it is an important feature of every HighPROTEC protection device that a lot of modules exist in several “instances”, which are numbered (in brackets), for example: »I2>[1]«, I2>[2]«

In the reference tables, usually every module has its own dedicated chapter, which lists the available number of instances at the beginning. Then, however, in the sub-chapters listing the various parameter types, only the first instance (e. g. »I2>[1]«) is mentioned, because all the other instances are identical anyway.

Structure of a Reference Table

Since (almost) every module can be activated or deactivated independently of the other modules and all parameters of an inactive module disappear from the menu branch it would not be helpful if this Reference Manual would list parameters sorted according to the menu structure. Instead, we list categories of modules (e. g. “Protection Functions”) and all the modules within a category.

For each parameter, there is a table with its properties, looking like this:

Module . Parameter	[Menu Path to This Parameter]	
Default Value For some parameters: • Availability restrictions	Value Range	
Type	*Short descriptive text explaining the functionality of this parameter.*	

“Type” is the data type of the parameter, which is denoted by a small icon. The following types are possible:

- Setting Parameter
- Direct Control
- Input State
- Signal (Output State)
- Statistical Value
- Counter
- (Measuring) Value
- Dialog — Such a dialog can feature several data objects using a special representation and/or functionality.

“Perm.” means “permission”, i. e. the access level and password that is required to modify the parameter. (Please refer to the “Security” chapter in the full Technical Manual for details.)

Several “access levels” exist, each having its individual password setting. (Each password is settable and can also be deactivated, see the MRU4 User Manual.)

In particular, the following permissions (access levels) can exist:

Short Designation in this Reference Manual	Name of Access Area (Panel or Smart view)	Access to:
"**RO**"	Read Only-Lv0	Level "**RO**" provides *Read Only* access to all settings and parameters of the device. The device will fall back into this level automatically after a configurable period or inactivity.
"**P.1**"	Prot-Lv1	This password provides access to the reset- and acknowledge options. In addition to that, it permits the execution of manual trigger signals.
"**P.2**"	Prot-Lv2	This password provides access to the reset and acknowledge options. In addition to that it permits changing of protection settings and the configuration of the trip manager.
"**C.1**"	Control-Lv1	This password grants permission for switching operations (switching switchgears).
"**C.2**"	Control-Lv2	This password grants permission for switching operations (switching switchgears). In addition to that it gives access to the switchgear settings (switching authority, interlockings, general settings of switchgears, Breaker wear...).
"**S.3**"	Supervisor-Lv3	This password grants non-restricted access to all parameters and settings of the device (device configuration). This includes also the devices planning, device parameters (e.g. Date and Time), Field Parameters, Service Parameters and Logic Parameters.

For some parameter types (e. g. Input and Output States), the second row (default, value range, permission) is useless and therefore omitted.

Example of a parameter:

ExP[1] . **Mode**	[Device planning]	
use	-, use ↳ Mode	S.3
general operation mode		

This means that one can find the parameter in the menu [Device planning], and its values are picked from a selection list named "Mode". The "↳" arrow indicates a cross-reference (hyperlink) into the "Selection Lists" chapter, and a click takes you to a table that lists all available choices.

The access level "S.3" means the access level "Supervisor-Lv3", which is required to modify the parameter.

Audience of This Manual

The manual serves as working basis for:

- Engineers in the protection field,
- commissioning engineers,
- people dealing with setting, testing and maintenance of protection and control devices,
- as well as trained personnel for electrical installations and power stations.

All functions concerning the MRU4 are listed. Should there be a description of any functions, parameters or inputs/outputs which do not apply to the device in use, please ignore that information.

This manual describes the (optionally) full featured versions of the devices.

All technical information and data included in this manual reflect their state at the time this document was issued. We reserve the right to carry out technical modifications in line with further development without changing this manual and without previous notice. Hence no claim can be brought based on the information and descriptions this manual includes.

We do not accept any liability for damage and operational failures caused by operating errors or disregarding the directions of this manual.

No part of this manual is allowed to be reproduced or passed on to others in any form, unless *SEG* have approved in writing.

This Reference Manual is part of the delivery scope when purchasing the device. In case the device is passed on (sold) to a third party, the manual has to be handed over as well.

Information Concerning Liability and Warranty

SEG does not accept any liability for damage resulting from conversions or changes carried out on the device or planning (projecting) work, parameter setting or adjustment changes done by the customer.

The warranty expires after a device has been opened by others than *SEG* specialists.

Warranty and liability conditions stated in *SEG* General Terms and Conditions are not supplemented by the above-mentioned explanations.

2 Device Configuration

MRU4	**#**	**#**	**#**	**#**	**#**	**#**
Version	**-2**					
Hardware Option1		**A**				
Hardware Option2			**0**			
Housing						
Flush mounting				**A**		
19 inch mounting (semi-flush)				**B**		
Customized Version 1				**H**		
Customized Version 2				**K**		
Communication						
Without					**A**	
RS 485: Modbus RTU | IEC 60870-5-103 | DNP3 RTU					**B**	
Ethernet: Modbus TCP | DNP3 UDP/TCP | IEC 60870-5-104					**C**	
Fiber Optics: Profibus-DP					**D**	
D-SUB: Profibus-DP					**E**	
Fiber Optics: Modbus RTU | IEC 60870-5-103 | DNP3 RTU					**F**	
RS 485/D-SUB: Modbus RTU | IEC 60870-5-103 | DNP3 RTU					**G**	
Ethernet: IEC 61850 communication | Modbus TCP | DNP3 UDP/TCP | IEC 60870-5-104					**H**	
RS 485, Ethernet: Modbus TCP/RTU | IEC 60870-5-103 | IEC 60870-5-104 | DNP3 UDP/TCP/RTU					**I**	
Ethernet/Fiber Optics: IEC 61850 communication | Modbus TCP | DNP3 UDP/TCP | IEC 60870-5-104					**K**	
Ethernet/Fiber Optics: Modbus TCP | DNP3 UDP/TCP | IEC 60870-5-104					**L**	
Red. Ethernet/Fiber Optics: Modbus TCP | DNP3 UDP/TCP | IEC 60870-5-104					**O**	
Red. Ethernet: Modbus TCP | DNP3 UDP/TCP | IEC 60870-5-104					**P**	
Red. Ethernet/Fiber Optics: Modbus TCP | DNP3 UDP/TCP | IEC 60870-5-104 | IEC 61850 communication					**Q**	
Red. Ethernet: Modbus TCP | DNP3 UDP/TCP | IEC 60870-5-104 | IEC 61850 communication					**R**	
RS 485, Ethernet: IEC 61850 | Modbus TCP/RTU | IEC 60870-5-103 | IEC 60870-5-104 | DNP3 UDP/TCP/RTU					**T**	
Printed Circuit Board						
Standard						**A**
printed circuit boards are conformal coated						**B**

3 Menu

3.1 Operation

3.1.1 Operation / Measured Values

3.1.1.1 Operation / Measured Values / Voltage

	»f«	Measured value: Frequency
	»VL12 «	Measured value: Phase-to-phase voltage (fundamental)
	»VL23 «	Measured value: Phase-to-phase voltage (fundamental)
	»VL31 «	Measured value: Phase-to-phase voltage (fundamental)
	»VL1 «	Measured value: Phase-to-neutral voltage (fundamental)
	»VL2 «	Measured value: Phase-to-neutral voltage (fundamental)
	»VL3 «	Measured value: Phase-to-neutral voltage (fundamental)
	»VX meas «	Measured value (measured): VX measured (fundamental)
	»VG calc «	Measured value (calculated): VG (fundamental)
	»V0 «	Measured value (calculated): Symmetrical components Zero voltage(fundamental)
	»V1 «	Measured value (calculated): Symmetrical components positive phase sequence voltage(fundamental)
	»V2 «	Measured value (calculated): Symmetrical components negative phase sequence voltage(fundamental)
	»%(V2/V1)«	Measured value (calculated): V2/V1, phase sequence will be taken into account automatically.
	»phi VL12«	Measured value (calculated): Angle of Phasor VL12 Reference phasor is required to calculate the angle. This is the first measured voltage (or current) channel with sufficiently high amplitude.
	»phi VL23«	Measured value (calculated): Angle of Phasor VL23 Reference phasor is required to calculate the angle. This is the first measured voltage (or current) channel with sufficiently high amplitude.
	»phi VL31«	Measured value (calculated): Angle of Phasor VL31 Reference phasor is required to calculate the angle. This is the first measured voltage (or current) channel with sufficiently high amplitude.
	»phi VL1«	Measured value (calculated): Angle of Phasor VL1 Reference phasor is required to calculate the angle. This is the first measured voltage (or current) channel with sufficiently high amplitude.
	»phi VL2«	Measured value (calculated): Angle of Phasor VL2 Reference phasor is required to calculate the angle. This is the first measured voltage (or current) channel with sufficiently high amplitude.
	»phi VL3«	Measured value (calculated): Angle of Phasor VL3 Reference phasor is required to calculate the angle. This is the first measured voltage (or current) channel with sufficiently high amplitude.
	»phi VX meas«	Measured value: Angle of Phasor VX meas Reference phasor is required to calculate the angle. This is the first measured voltage (or current) channel with sufficiently high amplitude.

	»phi VG calc«	Measured value (calculated): Angle of Phasor VG calc Reference phasor is required to calculate the angle. This is the first measured voltage (or current) channel with sufficiently high amplitude.
	»phi V0«	Measured value (calculated): Angle Zero Sequence System Reference phasor is required to calculate the angle. This is the first measured voltage (or current) channel with sufficiently high amplitude.
	»phi V1«	Measured value (calculated): Angle of Positive Sequence System Reference phasor is required to calculate the angle. This is the first measured voltage (or current) channel with sufficiently high amplitude.
	»phi V2«	Measured Value (calculated): Angle of Negative Sequence System Reference phasor is required to calculate the angle. This is the first measured voltage (or current) channel with sufficiently high amplitude.
	»df/dt«	Measured value (calculated): Rate-of-frequency-change.
	»delta phi«	Measured value (calculated): Vector surge

3.1.1.2 Operation / Measured Values / Voltage RMS

	»VL12 RMS«	Measured value: Phase-to-phase voltage (RMS)
	»VL23 RMS«	Measured value: Phase-to-phase voltage (RMS)
	»VL31 RMS«	Measured value: Phase-to-phase voltage (RMS)
	»VL1 RMS«	Measured value: Phase-to-neutral voltage (RMS)
	»VL2 RMS«	Measured value: Phase-to-neutral voltage (RMS)
	»VL3 RMS«	Measured value: Phase-to-neutral voltage (RMS)
	»VX meas RMS«	Measured value (measured): VX measured (RMS)
	»VG calc RMS«	Measured value (calculated): VG (RMS)
	»%VL12 THD«	Measured value (calculated): V12 Total Harmonic Distortion / Ground wave
	»%VL23 THD«	Measured value (calculated): V23 Total Harmonic Distortion / Ground wave
	»%VL31 THD«	Measured value (calculated): V31 Total Harmonic Distortion / Ground wave
	»%VL1 THD«	Measured value (calculated): VL1 Total Harmonic Distortion / Ground wave
	»%VL2 THD«	Measured value (calculated): VL2 Total Harmonic Distortion / Ground wave
	»%VL3 THD«	Measured value (calculated): VL3 Total Harmonic Distortion / Ground wave
	»VL12 THD«	Measured value (calculated): V12 Total Harmonic Distortion
	»VL23 THD«	Measured value (calculated): V23 Total Harmonic Distortion
	»VL31 THD«	Measured value (calculated): V31 Total Harmonic Distortion
	»VL1 THD«	Measured value (calculated): VL1 Total Harmonic Distortion
	»VL2 THD«	Measured value (calculated): VL2 Total Harmonic Distortion
	»VL3 THD«	Measured value (calculated): VL3 Total Harmonic Distortion

3.1.1.3 Operation / Measured Values / Synchronism

	»Slip Freq«	Slip frequency
	»Volt Diff«	Voltage difference between bus and line.
	»Angle Diff«	Angle difference between bus and line voltages.
	»f Bus«	Bus frequency
	»f Line«	Line frequency
	»V Bus«	Bus Voltage
	»V Line«	Line Voltage
	»Angle Bus«	Bus Angle (Reference)
	»Angle Line«	Line Angle

3.1.2 Operation / Statistics

3.1.2.1 Operation / Statistics / Max

3.1.2.1.1 Operation / Statistics / Max / Voltage

	»f max«	Max. frequency value
	»VL12 max RMS«	VL12 maximum value (RMS)
	»VL23 max RMS«	VL23 maximum value (RMS)
	»VL31 max RMS«	VL31 maximum value (RMS)
	»VL1 max RMS«	VL1 maximum value (RMS)
	»VL2 max RMS«	VL2 maximum value (RMS)
	»VL3 max RMS«	VL3 maximum value (RMS)
	»VX meas max RMS«	Measured value: VX maximum value (RMS)
	»VG calc max RMS«	Measured value (calculated):VX maximum value (RMS)
	»V1 max «	Maximum value: Symmetrical components positive phase sequence voltage(fundamental)
	»V2 max «	Maximum value: Symmetrical components negative phase sequence voltage(fundamental)
	»%(V2/V1) max«	Measured value (calculated):V2/V1 maximum value, phase sequence will be taken into account automatically
	»Res Cr Max values«	Number of resets since the last device restart. The timestamp shows date and time of the last reset.

3.1.2.2 Operation / Statistics / Min

3.1.2.2.1 Operation / Statistics / Min / Voltage

🗠	»f min «	Min. frequency value
🗠	»VL12 min RMS«	VL12 minimum value (RMS)
🗠	»VL23 min RMS«	VL23 minimum value (RMS)
🗠	»VL31 min RMS«	VL31 minimum value (RMS)
🗠	»VL1 min RMS«	VL1 minimum value (RMS)
🗠	»VL2 min RMS«	VL2 minimum value (RMS)
🗠	»VL3 min RMS«	VL3 minimum value (RMS)
🗠	»VX meas min RMS«	Measured value: VX minimum value (RMS)
🗠	»VG calc min RMS«	Measured value (calculated):VX minimum value (RMS)
🗠	»V1 min «	Minimum value: Symmetrical components positive phase sequence voltage(fundamental)
🗠	»V2 min «	Minimum value: Symmetrical components negative phase sequence voltage(fundamental)
🗠	»%(V2/V1) min«	Measured value (calculated):V2/V1 minimum value , phase sequence will be taken into account automatically
#	»Res Cr Min values«	Number of resets since the last device restart. The timestamp shows date and time of the last reset.

3.1.2.3 Operation / Statistics / Vavg

🗠	»VL12 avg RMS«	VL12 average value (RMS)
🗠	»VL23 avg RMS«	VL23 average value (RMS)
🗠	»VL31 avg RMS«	VL31 average value (RMS)
🗠	»VL1 avg RMS«	VL1 average value (RMS)
🗠	»VL2 avg RMS«	VL2 average value (RMS)
🗠	»VL3 avg RMS«	VL3 average value (RMS)
#	»Res Cr V avg«	Number of resets since the last device restart. The timestamp shows date and time of the last reset.

3.1.3 Operation / Status Display

3.1.3.1 Operation / Status Display / All Actives

⇧	»Prot . Active«	Signal: active
⇧	»V[1] . Active«	Signal: active

⇧	»V[2] . Active«	Signal: active
⇧	»V[3] . Active«	Signal: active
⇧	»V[4] . Active«	Signal: active
⇧	»V[5] . Active«	Signal: active
⇧	»V[6] . Active«	Signal: active
⇧	»df/dt . Active«	Signal: active
⇧	»delta phi . Active«	Signal: active
⇧	»Intertripping . Active«	Signal: active
⇧	»LVRT[1] . Active«	Signal: active
⇧	»LVRT[2] . Active«	Signal: active
⇧	»VG[1] . Active«	Signal: active
⇧	»VG[2] . Active«	Signal: active
⇧	»V012[1] . Active«	Signal: active
⇧	»V012[2] . Active«	Signal: active
⇧	»V012[3] . Active«	Signal: active
⇧	»V012[4] . Active«	Signal: active
⇧	»V012[5] . Active«	Signal: active
⇧	»V012[6] . Active«	Signal: active
⇧	»f[1] . Active«	Signal: active
⇧	»f[2] . Active«	Signal: active
⇧	»f[3] . Active«	Signal: active
⇧	»f[4] . Active«	Signal: active
⇧	»f[5] . Active«	Signal: active
⇧	»f[6] . Active«	Signal: active
⇧	»ReCon[1] . Active«	Signal: active
⇧	»ReCon[2] . Active«	Signal: active
⇧	»Sync . Active«	Signal: active
⇧	»ExP[1] . Active«	Signal: active
⇧	»ExP[2] . Active«	Signal: active
⇧	»ExP[3] . Active«	Signal: active
⇧	»ExP[4] . Active«	Signal: active
⇧	»CBF . Active«	Signal: active
⇧	»TCS . Active«	Signal: active
⇧	»VTS . Active«	Signal: active

⇧	»SysA . Active«	Signal: active

3.1.3.2 Operation / Status Display / Alarms

⇧	»Prot . Alarm«	Signal: General Alarm
⇧	»V[1] . Alarm«	Signal: Alarm voltage stage
⇧	»V[2] . Alarm«	Signal: Alarm voltage stage
⇧	»V[3] . Alarm«	Signal: Alarm voltage stage
⇧	»V[4] . Alarm«	Signal: Alarm voltage stage
⇧	»V[5] . Alarm«	Signal: Alarm voltage stage
⇧	»V[6] . Alarm«	Signal: Alarm voltage stage
⇧	»df/dt . Alarm«	Signal: Alarm Frequency Protection (collective signal)
⇧	»delta phi . Alarm«	Signal: Alarm Frequency Protection (collective signal)
⇧	»Intertripping . Alarm«	Signal: Alarm
⇧	»LVRT[1] . Alarm«	Signal: Alarm voltage stage
⇧	»LVRT[2] . Alarm«	Signal: Alarm voltage stage
⇧	»VG[1] . Alarm«	Signal: Alarm Residual Voltage Supervision-stage
⇧	»VG[2] . Alarm«	Signal: Alarm Residual Voltage Supervision-stage
⇧	»V012[1] . Alarm«	Signal: Alarm voltage asymmetry
⇧	»V012[2] . Alarm«	Signal: Alarm voltage asymmetry
⇧	»V012[3] . Alarm«	Signal: Alarm voltage asymmetry
⇧	»V012[4] . Alarm«	Signal: Alarm voltage asymmetry
⇧	»V012[5] . Alarm«	Signal: Alarm voltage asymmetry
⇧	»V012[6] . Alarm«	Signal: Alarm voltage asymmetry
⇧	»f[1] . Alarm«	Signal: Alarm Frequency Protection (collective signal)
⇧	»f[2] . Alarm«	Signal: Alarm Frequency Protection (collective signal)
⇧	»f[3] . Alarm«	Signal: Alarm Frequency Protection (collective signal)
⇧	»f[4] . Alarm«	Signal: Alarm Frequency Protection (collective signal)
⇧	»f[5] . Alarm«	Signal: Alarm Frequency Protection (collective signal)
⇧	»f[6] . Alarm«	Signal: Alarm Frequency Protection (collective signal)
⇧	»ExP[1] . Alarm«	Signal: Alarm
⇧	»ExP[2] . Alarm«	Signal: Alarm
⇧	»ExP[3] . Alarm«	Signal: Alarm
⇧	»ExP[4] . Alarm«	Signal: Alarm
⇧	»TCS . Alarm«	Signal: Alarm Trip Circuit Supervision

⇧	»VTS . Alarm«	Signal: Alarm Voltage Transformer Measuring Circuit Supervision

3.1.3.3 Operation / Status Display / Trips

⇧	»Prot . Trip«	Signal: General Trip
⇧	»V[1] . Trip«	Signal: Trip
⇧	»V[2] . Trip«	Signal: Trip
⇧	»V[3] . Trip«	Signal: Trip
⇧	»V[4] . Trip«	Signal: Trip
⇧	»V[5] . Trip«	Signal: Trip
⇧	»V[6] . Trip«	Signal: Trip
⇧	»df/dt . Trip«	Signal: Trip Frequency Protection (collective signal)
⇧	»delta phi . Trip«	Signal: Trip Frequency Protection (collective signal)
⇧	»Intertripping . Trip«	Signal: Trip
⇧	»LVRT[1] . Trip«	Signal: Trip
⇧	»LVRT[2] . Trip«	Signal: Trip
⇧	»VG[1] . Trip«	Signal: Trip
⇧	»VG[2] . Trip«	Signal: Trip
⇧	»V012[1] . Trip«	Signal: Trip
⇧	»V012[2] . Trip«	Signal: Trip
⇧	»V012[3] . Trip«	Signal: Trip
⇧	»V012[4] . Trip«	Signal: Trip
⇧	»V012[5] . Trip«	Signal: Trip
⇧	»V012[6] . Trip«	Signal: Trip
⇧	»f[1] . Trip«	Signal: Trip Frequency Protection (collective signal)
⇧	»f[2] . Trip«	Signal: Trip Frequency Protection (collective signal)
⇧	»f[3] . Trip«	Signal: Trip Frequency Protection (collective signal)
⇧	»f[4] . Trip«	Signal: Trip Frequency Protection (collective signal)
⇧	»f[5] . Trip«	Signal: Trip Frequency Protection (collective signal)
⇧	»f[6] . Trip«	Signal: Trip Frequency Protection (collective signal)
⇧	»ExP[1] . Trip«	Signal: Trip
⇧	»ExP[2] . Trip«	Signal: Trip
⇧	»ExP[3] . Trip«	Signal: Trip
⇧	»ExP[4] . Trip«	Signal: Trip

⇧	»CBF . Alarm«	Signal: Circuit Breaker Failure

3.1.3.4 Operation / Status Display / TripCmds

⇧	»SG[1] . TripCmd«	Signal: Trip Command
⇧	»V[1] . TripCmd«	Signal: Trip Command
⇧	»V[2] . TripCmd«	Signal: Trip Command
⇧	»V[3] . TripCmd«	Signal: Trip Command
⇧	»V[4] . TripCmd«	Signal: Trip Command
⇧	»V[5] . TripCmd«	Signal: Trip Command
⇧	»V[6] . TripCmd«	Signal: Trip Command
⇧	»df/dt . TripCmd«	Signal: Trip Command
⇧	»delta phi . TripCmd«	Signal: Trip Command
⇧	»Intertripping . TripCmd«	Signal: Trip Command
⇧	»LVRT[1] . TripCmd«	Signal: Trip Command
⇧	»LVRT[2] . TripCmd«	Signal: Trip Command
⇧	»VG[1] . TripCmd«	Signal: Trip Command
⇧	»VG[2] . TripCmd«	Signal: Trip Command
⇧	»V012[1] . TripCmd«	Signal: Trip Command
⇧	»V012[2] . TripCmd«	Signal: Trip Command
⇧	»V012[3] . TripCmd«	Signal: Trip Command
⇧	»V012[4] . TripCmd«	Signal: Trip Command
⇧	»V012[5] . TripCmd«	Signal: Trip Command
⇧	»V012[6] . TripCmd«	Signal: Trip Command
⇧	»f[1] . TripCmd«	Signal: Trip Command
⇧	»f[2] . TripCmd«	Signal: Trip Command
⇧	»f[3] . TripCmd«	Signal: Trip Command
⇧	»f[4] . TripCmd«	Signal: Trip Command
⇧	»f[5] . TripCmd«	Signal: Trip Command
⇧	»f[6] . TripCmd«	Signal: Trip Command
⇧	»ExP[1] . TripCmd«	Signal: Trip Command
⇧	»ExP[2] . TripCmd«	Signal: Trip Command
⇧	»ExP[3] . TripCmd«	Signal: Trip Command
⇧	»ExP[4] . TripCmd«	Signal: Trip Command

3.1.3.5 Operation / Status Display / Prot

⇧	»available«	Signal: Protection is available
⇧	»Active«	Signal: active
⇧	»ExBlo«	Signal: External Blocking
⇧	»Blo TripCmd«	Signal: Trip Command blocked
⇧	»ExBlo TripCmd«	Signal: External Blocking of the Trip Command
⇧	»Alarm L1«	Signal: General-Alarm L1
⇧	»Alarm L2«	Signal: General-Alarm L2
⇧	»Alarm L3«	Signal: General-Alarm L3
⇧	»Alarm G«	Signal: General-Alarm - Earth fault
⇧	»Alarm«	Signal: General Alarm
⇧	»Trip L1«	Signal: General Trip L1
⇧	»Trip L2«	Signal: General Trip L2
⇧	»Trip L3«	Signal: General Trip L3
⇧	»Trip G«	Signal: General Trip Ground fault
⇧	»Trip«	Signal: General Trip
⇧	»Res FaultNo a GridFaultNo«	Signal: Resetting of fault number and grid fault number.
⇩	»ExBlo1-I«	Module input state: External blocking1
⇩	»ExBlo2-I«	Module input state: External blocking2
⇩	»ExBlo TripCmd-I«	Module input state: External Blocking of the Trip Command

3.1.3.6 Operation / Status Display / Control

3.1.3.6.1 Operation / Status Display / Control / General Control

⇧	»Local«	Switching Authority: Local
⇧	»Remote«	Switching Authority: Remote
⇧	»NonInterl«	Non-Interlocking is active
⇧	»SG Indeterm«	(At least one) Switchgear is moving (Position cannot be determined).
⇧	»SG Disturb«	(At least one) Switchgear is disturbed.
⇧	»CES SAuthority«	Command Execution Supervision: Number of rejected Commands because of missing switching authority.
⇧	»CES DoubleOperating«	Command Execution Supervision: Number of rejected Commands because a second switch command is in conflict with a pending one.
⇩	»NonInterl-I«	Non-Interlocking

3.1.3.6.2 Operation / Status Display / Control / SG[1]

⇧	»SI SingleContactInd«	Signal: The Position of the Switchgear is detected by one auxiliary contact (pole) only. Thus indeterminate and disturbed Positions cannot be detected.
⇧	»Pos not ON«	Signal: Pos not ON
⇧	»Pos ON«	Signal: Circuit Breaker is in ON-Position
⇧	»Pos OFF«	Signal: Circuit Breaker is in OFF-Position
⇧	»Pos Indeterm«	Signal: Circuit Breaker is in Indeterminate Position
⇧	»Pos Disturb«	Signal: Circuit Breaker Disturbed - Undefined Breaker Position. The Position Indicators contradict themselves. After expiring of a supervision timer this signal becomes true.
⇧	»Pos«	Signal: Circuit Breaker Position (0 = Indeterminate, 1 = OFF, 2 = ON, 3 = Disturbed)
⇧	»Ready«	Signal: Circuit breaker is ready for operation.
⇧	»t-Dwell«	Signal: Dwell time
⇧	»Removed«	Signal: The withdrawable circuit breaker is Removed
⇧	»Interl ON«	Signal: One or more IL_On inputs are active.
⇧	»Interl OFF«	Signal: One or more IL_Off inputs are active.
⇧	»CES succesf«	Signal: Command Execution Supervision: Switching command executed successfully.
⇧	»CES Disturbed«	Signal: Command Execution Supervision: Switching Command unsuccessful. Switchgear in disturbed position.
⇧	»CES Fail TripCmd«	Signal: Command Execution Supervision: Command execution failed because trip command is pending.
⇧	»CES SwitchDir«	Signal: Command Execution Supervision respectively Switching Direction Control: This signal becomes true, if a switch command is issued even though the switchgear is already in the requested position. Example: A switchgear that is already OFF should be switched OFF again (doubly). The same applies to CLOSE commands.
⇧	»CES ON d OFF«	Signal: Command Execution Supervision: On Command during a pending OFF Command.
⇧	»CES SG not ready«	Signal: Command Execution Supervision: Switchgear not ready
⇧	»CES Fiel Interl«	Signal: Command Execution Supervision: Switching Command not executed because of field interlocking.
⇧	»CES SyncTimeout«	Signal: Command Execution Supervision: Switching Command not executed. No Synchronization signal while t-sync was running.
⇧	»CES SG removed«	Signal: Command Execution Supervision: Switching Command unsuccessful, Switchgear removed.
⇧	»Prot ON«	Signal: ON Command issued by the Prot module
⇧	»TripCmd«	Signal: Trip Command
⇧	»Ack TripCmd«	Signal: Acknowledge Trip Command
⇧	»ON incl Prot ON«	Signal: The ON Command includes the ON Command issued by the Protection module.
⇧	»OFF incl TripCmd«	Signal: The OFF Command includes the OFF Command issued by the Protection module.

⇧	»Position Ind manipul«	Signal: Position Indicators faked
⇧	»SGwear Slow SG«	Signal: Alarm, the circuit breaker (load-break switch) becomes slower
⇧	»Res SGwear Sl SG«	Signal: Resetting the slow Switchgear Alarm
⇧	»ON Cmd«	Signal: ON Command issued to the switchgear. Depending on the setting the signal may include the ON command of the Prot module.
⇧	»OFF Cmd«	Signal: OFF Command issued to the switchgear. Depending on the setting the signal may include the OFF command of the Prot module.
⇧	»ON Cmd manual«	Signal: ON Cmd manual
⇧	»OFF Cmd manual«	Signal: OFF Cmd manual
⇧	»Sync ON request«	Signal: Synchronous ON request
⇧	»Test Trip Cmd«	A trip command has been triggered manually (for testing purposes).
⇧	»Operations Alarm«	Signal: Too many Operations. (The operations counter »TripCmd Cr« has exceeded the limit set at »Operations Alarm«.)
⇧	»Res TripCmd Cr«	Signal: Resetting of the Counter: Total number of trips of the switchgear
⇩	»Interl ON1-I«	State of the module input: Interlocking of the ON command
⇩	»Interl ON2-I«	State of the module input: Interlocking of the ON command
⇩	»Interl ON3-I«	State of the module input: Interlocking of the ON command
⇩	»Interl OFF1-I«	State of the module input: Interlocking of the OFF command
⇩	»Interl OFF2-I«	State of the module input: Interlocking of the OFF command
⇩	»Interl OFF3-I«	State of the module input: Interlocking of the OFF command
⇩	»SCmd ON-I«	State of the module input: Switching ON Command, e.g. the state of the Logics or the state of the digital input
⇩	»SCmd OFF-I«	State of the module input: Switching OFF Command, e.g. the state of the Logics or the state of the digital input
⇩	»Aux ON-I«	Module Input State: Position indicator/check-back signal of the CB (52a)
⇩	»Aux OFF-I«	Module input state: Position indicator/check-back signal of the CB (52b)
⇩	»Ready-I«	Module input state: CB ready
⇩	»Sys-in-Sync-I«	State of the module input: This signals has to become true within the synchronization time. If not, switching is unsuccessful.
⇩	»Removed-I«	State of the module input: The withdrawable circuit breaker is Removed
⇩	»Ack TripCmd-I«	State of the module input: Acknowledgement Signal (for the Trip Command) Module input signal

3.1.3.7 Operation / Status Display / Intercon-Prot

3.1.3.7.1 Operation / Status Display / Intercon-Prot / Mains Decouplg

3.1.3.7.1.1 Operation / Status Display / Intercon-Prot / Mains Decouplg / df/dt

⇧	»Active«	Signal: active
⇧	»ExBlo«	Signal: External Blocking
⇧	»Blo by V<«	Signal: Module is blocked by undervoltage.
⇧	»Blo TripCmd«	Signal: Trip Command blocked
⇧	»ExBlo TripCmd«	Signal: External Blocking of the Trip Command
⇧	»Alarm«	Signal: Alarm Frequency Protection (collective signal)
⇧	»Trip«	Signal: Trip Frequency Protection (collective signal)
⇧	»TripCmd«	Signal: Trip Command
⇩	»ExBlo1-I«	Module input state: External blocking1
⇩	»ExBlo2-I«	Module input state: External blocking2
⇩	»ExBlo TripCmd-I«	Module input state: External Blocking of the Trip Command

3.1.3.7.1.2 Operation / Status Display / Intercon-Prot / Mains Decouplg / delta phi

⇧	»Active«	Signal: active
⇧	»ExBlo«	Signal: External Blocking
⇧	»Blo by V<«	Signal: Module is blocked by undervoltage.
⇧	»Blo TripCmd«	Signal: Trip Command blocked
⇧	»ExBlo TripCmd«	Signal: External Blocking of the Trip Command
⇧	»Alarm«	Signal: Alarm Frequency Protection (collective signal)
⇧	»Trip«	Signal: Trip Frequency Protection (collective signal)
⇧	»TripCmd«	Signal: Trip Command
⇩	»ExBlo1-I«	Module input state: External blocking1
⇩	»ExBlo2-I«	Module input state: External blocking2
⇩	»ExBlo TripCmd-I«	Module input state: External Blocking of the Trip Command

3.1.3.7.1.3 Operation / Status Display / Intercon-Prot / Mains Decouplg / Intertripping

⇧	»Active«	Signal: active
⇧	»ExBlo«	Signal: External Blocking
⇧	»Blo TripCmd«	Signal: Trip Command blocked
⇧	»ExBlo TripCmd«	Signal: External Blocking of the Trip Command
⇧	»Alarm«	Signal: Alarm
⇧	»Trip«	Signal: Trip
⇧	»TripCmd«	Signal: Trip Command
⇩	»ExBlo1-I«	Module input state: External blocking1
⇩	»ExBlo2-I«	Module input state: External blocking2
⇩	»ExBlo TripCmd-I«	Module input state: External Blocking of the Trip Command
⇩	»Alarm-I«	Module input state: Alarm
⇩	»Trip-I«	Module input state: Trip

3.1.3.7.2 Operation / Status Display / Intercon-Prot / LVRT[1]

⇧	»Active«	Signal: active
⇧	»ExBlo«	Signal: External Blocking
⇧	»Blo TripCmd«	Signal: Trip Command blocked
⇧	»ExBlo TripCmd«	Signal: External Blocking of the Trip Command
⇧	»Alarm L1«	Signal: Alarm L1
⇧	»Alarm L2«	Signal: Alarm L2
⇧	»Alarm L3«	Signal: Alarm L3
⇧	»Alarm«	Signal: Alarm voltage stage
⇧	»Trip L1«	Signal: General Trip Phase L1
⇧	»Trip L2«	Signal: General Trip Phase L2
⇧	»Trip L3«	Signal: General Trip Phase L3
⇧	»Trip«	Signal: Trip
⇧	»TripCmd«	Signal: Trip Command
⇧	»t-LVRT is running«	Signal: t-LVRT is running
⇩	»ExBlo1-I«	Module input state: External blocking1
⇩	»ExBlo2-I«	Module input state: External blocking2
⇩	»ExBlo TripCmd-I«	Module input state: External Blocking of the Trip Command

3.1.3.7.3 Operation / Status Display / Intercon-Prot / LVRT[2]

⇧	»Active«	Signal: active
⇧	»ExBlo«	Signal: External Blocking
⇧	»Blo TripCmd«	Signal: Trip Command blocked
⇧	»ExBlo TripCmd«	Signal: External Blocking of the Trip Command
⇧	»Alarm L1«	Signal: Alarm L1
⇧	»Alarm L2«	Signal: Alarm L2
⇧	»Alarm L3«	Signal: Alarm L3
⇧	»Alarm«	Signal: Alarm voltage stage
⇧	»Trip L1«	Signal: General Trip Phase L1
⇧	»Trip L2«	Signal: General Trip Phase L2
⇧	»Trip L3«	Signal: General Trip Phase L3
⇧	»Trip«	Signal: Trip
⇧	»TripCmd«	Signal: Trip Command
⇧	»t-LVRT is running«	Signal: t-LVRT is running
⇩	»ExBlo1-I«	Module input state: External blocking1
⇩	»ExBlo2-I«	Module input state: External blocking2
⇩	»ExBlo TripCmd-I«	Module input state: External Blocking of the Trip Command

3.1.3.7.4 Operation / Status Display / Intercon-Prot / ReCon[1]

⇧	»Active«	Signal: active
⇧	»ExBlo«	Signal: External Blocking
⇧	»Blo by Meas Circ Superv«	Signal: Module blocked by measuring cirucuit supervision
⇧	»Eval Recon-Conditions«	Signal: Evaluation of reconnection conditions after decoupling event
⇧	»t-Release running«	Signal: The timer "t-Release" is running. Thus, all conditions for reconnection are fulfilled. After the timer has expired reconnection release will be issued.
⇧	»Release Energy Res.«	Signal: Signal: Release Energy Resource.
⇧	»V out of range«	Signal: Reconnection release is blocked because voltage is out of range
⇧	»f out ouf range«	Signal: Reconnection release is blocked because frequency is out of range
⇩	»ExBlo1-I«	Module input state: External blocking1
⇩	»ExBlo2-I«	Module input state: External blocking2
⇩	»V Ext Release PCC-I«	Module input state: Release signal is being generated by the PCC (External Release)
⇩	»PCC Fuse Fail VT-I«	State of the module input: Blocking if the fuse of a voltage transformer has tripped at the PCC.
⇩	»reconnected-I«	This signal indicates the state "reconnected" (mains parallel).
⇩	»Decoupling1-I«	Decoupling function, that triggers the reconnection.
⇩	»Decoupling2-I«	Decoupling function, that triggers the reconnection.
⇩	»Decoupling3-I«	Decoupling function, that triggers the reconnection.
⇩	»Decoupling4-I«	Decoupling function, that triggers the reconnection.
⇩	»Decoupling5-I«	Decoupling function, that triggers the reconnection.
⇩	»Decoupling6-I«	Decoupling function, that triggers the reconnection.

3.1.3.7.5 Operation / Status Display / Intercon-Prot / ReCon[2]

⇧	»Active«	Signal: active
⇧	»ExBlo«	Signal: External Blocking
⇧	»Blo by Meas Circ Superv«	Signal: Module blocked by measuring cirucuit supervision
⇧	»Eval Recon-Conditions«	Signal: Evaluation of reconnection conditions after decoupling event
⇧	»t-Release running«	Signal: The timer "t-Release" is running. Thus, all conditions for reconnection are fulfilled. After the timer has expired reconnection release will be issued.
⇧	»Release Energy Res.«	Signal: Signal: Release Energy Resource.
⇧	»V out of range«	Signal: Reconnection release is blocked because voltage is out of range
⇧	»f out ouf range«	Signal: Reconnection release is blocked because frequency is out of range
⇩	»ExBlo1-I«	Module input state: External blocking1
⇩	»ExBlo2-I«	Module input state: External blocking2
⇩	»V Ext Release PCC-I«	Module input state: Release signal is being generated by the PCC (External Release)
⇩	»PCC Fuse Fail VT-I«	State of the module input: Blocking if the fuse of a voltage transformer has tripped at the PCC.
⇩	»reconnected-I«	This signal indicates the state "reconnected" (mains parallel).
⇩	»Decoupling1-I«	Decoupling function, that triggers the reconnection.
⇩	»Decoupling2-I«	Decoupling function, that triggers the reconnection.
⇩	»Decoupling3-I«	Decoupling function, that triggers the reconnection.
⇩	»Decoupling4-I«	Decoupling function, that triggers the reconnection.
⇩	»Decoupling5-I«	Decoupling function, that triggers the reconnection.
⇩	»Decoupling6-I«	Decoupling function, that triggers the reconnection.

3.1.3.7.6 Operation / Status Display / Intercon-Prot / Sync

⇧	»Active«	Signal: active
⇧	»ExBlo«	Signal: External Blocking
⇧	»LiveBus«	Signal: Live-Bus flag: 1=Live-Bus, 0=Voltage is below the LiveBus threshold
⇧	»LiveLine«	Signal: Live Line flag: 1=Live-Line, 0=Voltage is below the LiveLine threshold
⇧	»SynchronRunTiming«	Signal: Synchron-Run-timer is timing (This timer starts when Close-Initiate is coming and stops if breaker is closed. Timeout means synchronizing failed.)
⇧	»SynchronFailed«	Signal: This signal indicates a failed synchronization. It is set for 5s when the circuit breaker is still open after the Synchron-Run-timer has timed out.
⇧	»SyncOverridden«	Signal:Synchronism Check is overridden because one of the Synchronism overriding conditions (DB/DL or ExtBypass) is met.
⇧	»VDiffTooHigh«	Signal: Voltage difference between bus and line too high.
⇧	»SlipTooHigh«	Signal: Frequency difference (slip frequency) between bus and line voltages too high.
⇧	»AngleDiffTooHigh«	Signal: Phase Angle difference between bus and line voltages too high.
⇧	»Sys-in-Sync«	Signal: Bus and line voltages are in synchronism according to the system synchronism criteria.
⇧	»Ready to Close«	Signal: Ready to Close
⇩	»ExBlo1-I«	Module input state: External blocking1
⇩	»ExBlo2-I«	Module input state: External blocking2
⇩	»Bypass-I«	State of the module input: The Synchrocheck will be bypassed if the state of the assigned signal (logic input) becomes true.
⇩	»CBCloseInitiate-I«	State of the module input: Breaker Close Initiate with synchronism check from any control sources (e.g. HMI / SCADA). If the state of the assigned signal becomes true, a Breaker Close will be initiated (Trigger Source).

3.1.3.8 Operation / Status Display / V-Prot

3.1.3.8.1 Operation / Status Display / V-Prot / V[1]

⇧	»Active«	Signal: active
⇧	»ExBlo«	Signal: External Blocking
⇧	»Blo TripCmd«	Signal: Trip Command blocked
⇧	»ExBlo TripCmd«	Signal: External Blocking of the Trip Command
⇧	»Alarm L1«	Signal: Alarm L1
⇧	»Alarm L2«	Signal: Alarm L2
⇧	»Alarm L3«	Signal: Alarm L3
⇧	»Alarm«	Signal: Alarm voltage stage
⇧	»Trip L1«	Signal: General Trip Phase L1
⇧	»Trip L2«	Signal: General Trip Phase L2
⇧	»Trip L3«	Signal: General Trip Phase L3
⇧	»Trip«	Signal: Trip
⇧	»TripCmd«	Signal: Trip Command
⇩	»ExBlo1-I«	Module input state: External blocking1
⇩	»ExBlo2-I«	Module input state: External blocking2
⇩	»ExBlo TripCmd-I«	Module input state: External Blocking of the Trip Command

3.1.3.8.2 Operation / Status Display / V-Prot / V[2]

⇧	»Active«	Signal: active
⇧	»ExBlo«	Signal: External Blocking
⇧	»Blo TripCmd«	Signal: Trip Command blocked
⇧	»ExBlo TripCmd«	Signal: External Blocking of the Trip Command
⇧	»Alarm L1«	Signal: Alarm L1
⇧	»Alarm L2«	Signal: Alarm L2
⇧	»Alarm L3«	Signal: Alarm L3
⇧	»Alarm«	Signal: Alarm voltage stage
⇧	»Trip L1«	Signal: General Trip Phase L1
⇧	»Trip L2«	Signal: General Trip Phase L2
⇧	»Trip L3«	Signal: General Trip Phase L3
⇧	»Trip«	Signal: Trip
⇧	»TripCmd«	Signal: Trip Command
⇩	»ExBlo1-I«	Module input state: External blocking1
⇩	»ExBlo2-I«	Module input state: External blocking2
⇩	»ExBlo TripCmd-I«	Module input state: External Blocking of the Trip Command

3.1.3.8.3 Operation / Status Display / V-Prot / V[3]

⇧	»Active«	Signal: active
⇧	»ExBlo«	Signal: External Blocking
⇧	»Blo TripCmd«	Signal: Trip Command blocked
⇧	»ExBlo TripCmd«	Signal: External Blocking of the Trip Command
⇧	»Alarm L1«	Signal: Alarm L1
⇧	»Alarm L2«	Signal: Alarm L2
⇧	»Alarm L3«	Signal: Alarm L3
⇧	»Alarm«	Signal: Alarm voltage stage
⇧	»Trip L1«	Signal: General Trip Phase L1
⇧	»Trip L2«	Signal: General Trip Phase L2
⇧	»Trip L3«	Signal: General Trip Phase L3
⇧	»Trip«	Signal: Trip
⇧	»TripCmd«	Signal: Trip Command
⇩	»ExBlo1-I«	Module input state: External blocking1
⇩	»ExBlo2-I«	Module input state: External blocking2
⇩	»ExBlo TripCmd-I«	Module input state: External Blocking of the Trip Command

3.1.3.8.4 Operation / Status Display / V-Prot / V[4]

⇧	»Active«	Signal: active
⇧	»ExBlo«	Signal: External Blocking
⇧	»Blo TripCmd«	Signal: Trip Command blocked
⇧	»ExBlo TripCmd«	Signal: External Blocking of the Trip Command
⇧	»Alarm L1«	Signal: Alarm L1
⇧	»Alarm L2«	Signal: Alarm L2
⇧	»Alarm L3«	Signal: Alarm L3
⇧	»Alarm«	Signal: Alarm voltage stage
⇧	»Trip L1«	Signal: General Trip Phase L1
⇧	»Trip L2«	Signal: General Trip Phase L2
⇧	»Trip L3«	Signal: General Trip Phase L3
⇧	»Trip«	Signal: Trip
⇧	»TripCmd«	Signal: Trip Command
⇩	»ExBlo1-I«	Module input state: External blocking1
⇩	»ExBlo2-I«	Module input state: External blocking2
⇩	»ExBlo TripCmd-I«	Module input state: External Blocking of the Trip Command

3.1.3.8.5 Operation / Status Display / V-Prot / V[5]

⇧	»Active«	Signal: active
⇧	»ExBlo«	Signal: External Blocking
⇧	»Blo TripCmd«	Signal: Trip Command blocked
⇧	»ExBlo TripCmd«	Signal: External Blocking of the Trip Command
⇧	»Alarm L1«	Signal: Alarm L1
⇧	»Alarm L2«	Signal: Alarm L2
⇧	»Alarm L3«	Signal: Alarm L3
⇧	»Alarm«	Signal: Alarm voltage stage
⇧	»Trip L1«	Signal: General Trip Phase L1
⇧	»Trip L2«	Signal: General Trip Phase L2
⇧	»Trip L3«	Signal: General Trip Phase L3
⇧	»Trip«	Signal: Trip
⇧	»TripCmd«	Signal: Trip Command
⇩	»ExBlo1-I«	Module input state: External blocking1
⇩	»ExBlo2-I«	Module input state: External blocking2
⇩	»ExBlo TripCmd-I«	Module input state: External Blocking of the Trip Command

3.1.3.8.6 Operation / Status Display / V-Prot / V[6]

⇧	»Active«	Signal: active
⇧	»ExBlo«	Signal: External Blocking
⇧	»Blo TripCmd«	Signal: Trip Command blocked
⇧	»ExBlo TripCmd«	Signal: External Blocking of the Trip Command
⇧	»Alarm L1«	Signal: Alarm L1
⇧	»Alarm L2«	Signal: Alarm L2
⇧	»Alarm L3«	Signal: Alarm L3
⇧	»Alarm«	Signal: Alarm voltage stage
⇧	»Trip L1«	Signal: General Trip Phase L1
⇧	»Trip L2«	Signal: General Trip Phase L2
⇧	»Trip L3«	Signal: General Trip Phase L3
⇧	»Trip«	Signal: Trip
⇧	»TripCmd«	Signal: Trip Command
⇩	»ExBlo1-I«	Module input state: External blocking1
⇩	»ExBlo2-I«	Module input state: External blocking2
⇩	»ExBlo TripCmd-I«	Module input state: External Blocking of the Trip Command

3.1.3.8.7 Operation / Status Display / V-Prot / VG[1]

⇧	»Active«	Signal: active
⇧	»ExBlo«	Signal: External Blocking
⇧	»Blo TripCmd«	Signal: Trip Command blocked
⇧	»ExBlo TripCmd«	Signal: External Blocking of the Trip Command
⇧	»Alarm«	Signal: Alarm Residual Voltage Supervision-stage
⇧	»Trip«	Signal: Trip
⇧	»TripCmd«	Signal: Trip Command
⇩	»ExBlo1-I«	Module input state: External blocking1
⇩	»ExBlo2-I«	Module input state: External blocking2
⇩	»ExBlo TripCmd-I«	Module input state: External Blocking of the Trip Command

3.1.3.8.8 Operation / Status Display / V-Prot / VG[2]

⇧	»Active«	Signal: active
⇧	»ExBlo«	Signal: External Blocking
⇧	»Blo TripCmd«	Signal: Trip Command blocked
⇧	»ExBlo TripCmd«	Signal: External Blocking of the Trip Command
⇧	»Alarm«	Signal: Alarm Residual Voltage Supervision-stage
⇧	»Trip«	Signal: Trip
⇧	»TripCmd«	Signal: Trip Command
⇩	»ExBlo1-I«	Module input state: External blocking1
⇩	»ExBlo2-I«	Module input state: External blocking2
⇩	»ExBlo TripCmd-I«	Module input state: External Blocking of the Trip Command

3.1.3.8.9 Operation / Status Display / V-Prot / V012[1]

⇧	»Active«	Signal: active
⇧	»ExBlo«	Signal: External Blocking
⇧	»Blo TripCmd«	Signal: Trip Command blocked
⇧	»ExBlo TripCmd«	Signal: External Blocking of the Trip Command
⇧	»Alarm«	Signal: Alarm voltage asymmetry
⇧	»Trip«	Signal: Trip
⇧	»TripCmd«	Signal: Trip Command
⇩	»ExBlo1-I«	Module input state: External blocking1
⇩	»ExBlo2-I«	Module input state: External blocking2
⇩	»ExBlo TripCmd-I«	Module input state: External Blocking of the Trip Command

3.1.3.8.10 Operation / Status Display / V-Prot / V012[2]

⇧	»Active«	Signal: active
⇧	»ExBlo«	Signal: External Blocking
⇧	»Blo TripCmd«	Signal: Trip Command blocked
⇧	»ExBlo TripCmd«	Signal: External Blocking of the Trip Command
⇧	»Alarm«	Signal: Alarm voltage asymmetry
⇧	»Trip«	Signal: Trip
⇧	»TripCmd«	Signal: Trip Command
⇩	»ExBlo1-I«	Module input state: External blocking1
⇩	»ExBlo2-I«	Module input state: External blocking2
⇩	»ExBlo TripCmd-I«	Module input state: External Blocking of the Trip Command

3.1.3.8.11 Operation / Status Display / V-Prot / V012[3]

⇧	»Active«	Signal: active
⇧	»ExBlo«	Signal: External Blocking
⇧	»Blo TripCmd«	Signal: Trip Command blocked
⇧	»ExBlo TripCmd«	Signal: External Blocking of the Trip Command
⇧	»Alarm«	Signal: Alarm voltage asymmetry
⇧	»Trip«	Signal: Trip
⇧	»TripCmd«	Signal: Trip Command
⇩	»ExBlo1-I«	Module input state: External blocking1
⇩	»ExBlo2-I«	Module input state: External blocking2
⇩	»ExBlo TripCmd-I«	Module input state: External Blocking of the Trip Command

3.1.3.8.12 Operation / Status Display / V-Prot / V012[4]

⇧	»Active«	Signal: active
⇧	»ExBlo«	Signal: External Blocking
⇧	»Blo TripCmd«	Signal: Trip Command blocked
⇧	»ExBlo TripCmd«	Signal: External Blocking of the Trip Command
⇧	»Alarm«	Signal: Alarm voltage asymmetry
⇧	»Trip«	Signal: Trip
⇧	»TripCmd«	Signal: Trip Command
⇩	»ExBlo1-I«	Module input state: External blocking1
⇩	»ExBlo2-I«	Module input state: External blocking2
⇩	»ExBlo TripCmd-I«	Module input state: External Blocking of the Trip Command

3.1.3.8.13 Operation / Status Display / V-Prot / V012[5]

⇧	»Active«	Signal: active
⇧	»ExBlo«	Signal: External Blocking
⇧	»Blo TripCmd«	Signal: Trip Command blocked
⇧	»ExBlo TripCmd«	Signal: External Blocking of the Trip Command
⇧	»Alarm«	Signal: Alarm voltage asymmetry
⇧	»Trip«	Signal: Trip
⇧	»TripCmd«	Signal: Trip Command
⇩	»ExBlo1-I«	Module input state: External blocking1
⇩	»ExBlo2-I«	Module input state: External blocking2
⇩	»ExBlo TripCmd-I«	Module input state: External Blocking of the Trip Command

3.1.3.8.14 Operation / Status Display / V-Prot / V012[6]

⇧	»Active«	Signal: active
⇧	»ExBlo«	Signal: External Blocking
⇧	»Blo TripCmd«	Signal: Trip Command blocked
⇧	»ExBlo TripCmd«	Signal: External Blocking of the Trip Command
⇧	»Alarm«	Signal: Alarm voltage asymmetry
⇧	»Trip«	Signal: Trip
⇧	»TripCmd«	Signal: Trip Command
⇩	»ExBlo1-I«	Module input state: External blocking1
⇩	»ExBlo2-I«	Module input state: External blocking2
⇩	»ExBlo TripCmd-I«	Module input state: External Blocking of the Trip Command

3.1.3.9 Operation / Status Display / f-Prot

3.1.3.9.1 Operation / Status Display / f-Prot / f[1]

⇧	»Active«	Signal: active
⇧	»ExBlo«	Signal: External Blocking
⇧	»Blo by V<«	Signal: Module is blocked by undervoltage.
⇧	»Blo TripCmd«	Signal: Trip Command blocked
⇧	»ExBlo TripCmd«	Signal: External Blocking of the Trip Command
⇧	»Alarm f«	Signal: Alarm Frequency Protection
⇧	»Alarm df/dt | DF/DT«	Alarm instantaneous or average value of the rate-of-frequency-change
⇧	»Alarm delta phi«	Signal: Alarm Vector Surge
⇧	»Alarm«	Signal: Alarm Frequency Protection (collective signal)
⇧	»Trip f«	Signal: Frequency has exceeded the limit.
⇧	»Trip df/dt | DF/DT«	Signal: Trip df/dt or DF/DT
⇧	»Trip delta phi«	Signal: Trip Vector Surge
⇧	»Trip«	Signal: Trip Frequency Protection (collective signal)
⇧	»TripCmd«	Signal: Trip Command
⇩	»ExBlo1-I«	Module input state: External blocking1
⇩	»ExBlo2-I«	Module input state: External blocking2
⇩	»ExBlo TripCmd-I«	Module input state: External Blocking of the Trip Command

3.1.3.9.2 Operation / Status Display / f-Prot / f[2]

⇧	»Active«	Signal: active
⇧	»ExBlo«	Signal: External Blocking
⇧	»Blo by V<«	Signal: Module is blocked by undervoltage.
⇧	»Blo TripCmd«	Signal: Trip Command blocked
⇧	»ExBlo TripCmd«	Signal: External Blocking of the Trip Command
⇧	»Alarm f«	Signal: Alarm Frequency Protection
⇧	»Alarm df/dt | DF/DT«	Alarm instantaneous or average value of the rate-of-frequency-change
⇧	»Alarm delta phi«	Signal: Alarm Vector Surge
⇧	»Alarm«	Signal: Alarm Frequency Protection (collective signal)
⇧	»Trip f«	Signal: Frequency has exceeded the limit.
⇧	»Trip df/dt | DF/DT«	Signal: Trip df/dt or DF/DT
⇧	»Trip delta phi«	Signal: Trip Vector Surge
⇧	»Trip«	Signal: Trip Frequency Protection (collective signal)
⇧	»TripCmd«	Signal: Trip Command
⇩	»ExBlo1-I«	Module input state: External blocking1
⇩	»ExBlo2-I«	Module input state: External blocking2
⇩	»ExBlo TripCmd-I«	Module input state: External Blocking of the Trip Command

3.1.3.9.3 Operation / Status Display / f-Prot / f[3]

⇧	»Active«	Signal: active
⇧	»ExBlo«	Signal: External Blocking
⇧	»Blo by V<«	Signal: Module is blocked by undervoltage.
⇧	»Blo TripCmd«	Signal: Trip Command blocked
⇧	»ExBlo TripCmd«	Signal: External Blocking of the Trip Command
⇧	»Alarm f«	Signal: Alarm Frequency Protection
⇧	»Alarm df/dt | DF/DT«	Alarm instantaneous or average value of the rate-of-frequency-change
⇧	»Alarm delta phi«	Signal: Alarm Vector Surge
⇧	»Alarm«	Signal: Alarm Frequency Protection (collective signal)
⇧	»Trip f«	Signal: Frequency has exceeded the limit.
⇧	»Trip df/dt | DF/DT«	Signal: Trip df/dt or DF/DT
⇧	»Trip delta phi«	Signal: Trip Vector Surge
⇧	»Trip«	Signal: Trip Frequency Protection (collective signal)
⇧	»TripCmd«	Signal: Trip Command
⇩	»ExBlo1-I«	Module input state: External blocking1
⇩	»ExBlo2-I«	Module input state: External blocking2
⇩	»ExBlo TripCmd-I«	Module input state: External Blocking of the Trip Command

3.1.3.9.4 Operation / Status Display / f-Prot / f[4]

⇧	»Active«	Signal: active
⇧	»ExBlo«	Signal: External Blocking
⇧	»Blo by V<«	Signal: Module is blocked by undervoltage.
⇧	»Blo TripCmd«	Signal: Trip Command blocked
⇧	»ExBlo TripCmd«	Signal: External Blocking of the Trip Command
⇧	»Alarm f«	Signal: Alarm Frequency Protection
⇧	»Alarm df/dt | DF/DT«	Alarm instantaneous or average value of the rate-of-frequency-change
⇧	»Alarm delta phi«	Signal: Alarm Vector Surge
⇧	»Alarm«	Signal: Alarm Frequency Protection (collective signal)
⇧	»Trip f«	Signal: Frequency has exceeded the limit.
⇧	»Trip df/dt | DF/DT«	Signal: Trip df/dt or DF/DT
⇧	»Trip delta phi«	Signal: Trip Vector Surge
⇧	»Trip«	Signal: Trip Frequency Protection (collective signal)
⇧	»TripCmd«	Signal: Trip Command
⇩	»ExBlo1-I«	Module input state: External blocking1
⇩	»ExBlo2-I«	Module input state: External blocking2
⇩	»ExBlo TripCmd-I«	Module input state: External Blocking of the Trip Command

3.1.3.9.5 Operation / Status Display / f-Prot / f[5]

⇧	»Active«	Signal: active
⇧	»ExBlo«	Signal: External Blocking
⇧	»Blo by V<«	Signal: Module is blocked by undervoltage.
⇧	»Blo TripCmd«	Signal: Trip Command blocked
⇧	»ExBlo TripCmd«	Signal: External Blocking of the Trip Command
⇧	»Alarm f«	Signal: Alarm Frequency Protection
⇧	»Alarm df/dt | DF/DT«	Alarm instantaneous or average value of the rate-of-frequency-change
⇧	»Alarm delta phi«	Signal: Alarm Vector Surge
⇧	»Alarm«	Signal: Alarm Frequency Protection (collective signal)
⇧	»Trip f«	Signal: Frequency has exceeded the limit.
⇧	»Trip df/dt | DF/DT«	Signal: Trip df/dt or DF/DT
⇧	»Trip delta phi«	Signal: Trip Vector Surge
⇧	»Trip«	Signal: Trip Frequency Protection (collective signal)
⇧	»TripCmd«	Signal: Trip Command
⇩	»ExBlo1-I«	Module input state: External blocking1
⇩	»ExBlo2-I«	Module input state: External blocking2
⇩	»ExBlo TripCmd-I«	Module input state: External Blocking of the Trip Command

3.1.3.9.6 Operation / Status Display / f-Prot / f[6]

⇧	»Active«	Signal: active
⇧	»ExBlo«	Signal: External Blocking
⇧	»Blo by V<«	Signal: Module is blocked by undervoltage.
⇧	»Blo TripCmd«	Signal: Trip Command blocked
⇧	»ExBlo TripCmd«	Signal: External Blocking of the Trip Command
⇧	»Alarm f«	Signal: Alarm Frequency Protection
⇧	»Alarm df/dt | DF/DT«	Alarm instantaneous or average value of the rate-of-frequency-change
⇧	»Alarm delta phi«	Signal: Alarm Vector Surge
⇧	»Alarm«	Signal: Alarm Frequency Protection (collective signal)
⇧	»Trip f«	Signal: Frequency has exceeded the limit.
⇧	»Trip df/dt | DF/DT«	Signal: Trip df/dt or DF/DT
⇧	»Trip delta phi«	Signal: Trip Vector Surge
⇧	»Trip«	Signal: Trip Frequency Protection (collective signal)
⇧	»TripCmd«	Signal: Trip Command
⇩	»ExBlo1-I«	Module input state: External blocking1
⇩	»ExBlo2-I«	Module input state: External blocking2
⇩	»ExBlo TripCmd-I«	Module input state: External Blocking of the Trip Command

3.1.3.10 Operation / Status Display / ExP

3.1.3.10.1 Operation / Status Display / ExP / ExP[1]

⇧	»Active«	Signal: active
⇧	»ExBlo«	Signal: External Blocking
⇧	»Blo TripCmd«	Signal: Trip Command blocked
⇧	»ExBlo TripCmd«	Signal: External Blocking of the Trip Command
⇧	»Alarm«	Signal: Alarm
⇧	»Trip«	Signal: Trip
⇧	»TripCmd«	Signal: Trip Command
⇩	»ExBlo1-I«	Module input state: External blocking1
⇩	»ExBlo2-I«	Module input state: External blocking2
⇩	»ExBlo TripCmd-I«	Module input state: External Blocking of the Trip Command
⇩	»Alarm-I«	Module input state: Alarm
⇩	»Trip-I«	Module input state: Trip

3.1.3.10.2 Operation / Status Display / ExP / ExP[2]

⇧	»Active«	Signal: active
⇧	»ExBlo«	Signal: External Blocking
⇧	»Blo TripCmd«	Signal: Trip Command blocked
⇧	»ExBlo TripCmd«	Signal: External Blocking of the Trip Command
⇧	»Alarm«	Signal: Alarm
⇧	»Trip«	Signal: Trip
⇧	»TripCmd«	Signal: Trip Command
⇩	»ExBlo1-I«	Module input state: External blocking1
⇩	»ExBlo2-I«	Module input state: External blocking2
⇩	»ExBlo TripCmd-I«	Module input state: External Blocking of the Trip Command
⇩	»Alarm-I«	Module input state: Alarm
⇩	»Trip-I«	Module input state: Trip

3.1.3.10.3 Operation / Status Display / ExP / ExP[3]

⇧	»Active«	Signal: active
⇧	»ExBlo«	Signal: External Blocking
⇧	»Blo TripCmd«	Signal: Trip Command blocked
⇧	»ExBlo TripCmd«	Signal: External Blocking of the Trip Command
⇧	»Alarm«	Signal: Alarm
⇧	»Trip«	Signal: Trip
⇧	»TripCmd«	Signal: Trip Command
⇩	»ExBlo1-I«	Module input state: External blocking1
⇩	»ExBlo2-I«	Module input state: External blocking2
⇩	»ExBlo TripCmd-I«	Module input state: External Blocking of the Trip Command
⇩	»Alarm-I«	Module input state: Alarm
⇩	»Trip-I«	Module input state: Trip

3.1.3.10.4 Operation / Status Display / ExP / ExP[4]

⇧	»Active«	Signal: active
⇧	»ExBlo«	Signal: External Blocking
⇧	»Blo TripCmd«	Signal: Trip Command blocked
⇧	»ExBlo TripCmd«	Signal: External Blocking of the Trip Command
⇧	»Alarm«	Signal: Alarm
⇧	»Trip«	Signal: Trip
⇧	»TripCmd«	Signal: Trip Command
⇩	»ExBlo1-I«	Module input state: External blocking1
⇩	»ExBlo2-I«	Module input state: External blocking2
⇩	»ExBlo TripCmd-I«	Module input state: External Blocking of the Trip Command
⇩	»Alarm-I«	Module input state: Alarm
⇩	»Trip-I«	Module input state: Trip

3.1.3.11 Operation / Status Display / Supervision

3.1.3.11.1 Operation / Status Display / Supervision / CBF

⇧	»Active«	Signal: active
⇧	»ExBlo«	Signal: External Blocking
⇧	»Waiting for Trigger«	Waiting for Trigger
⇧	»running«	Signal: CBF-Module started
⇧	»Alarm«	Signal: Circuit Breaker Failure
⇧	»Lockout«	Signal: Lockout
⇧	»Res Lockout«	Signal: Reset Lockout
⇩	»ExBlo1-I«	Module input state: External blocking1
⇩	»ExBlo2-I«	Module input state: External blocking2
⇩	»Trigger1-I«	Module Input: Trigger that will start the CBF
⇩	»Trigger2-I«	Module Input: Trigger that will start the CBF
⇩	»Trigger3-I«	Module Input: Trigger that will start the CBF

3.1.3.11.2 Operation / Status Display / Supervision / TCS

⇧	»Active«	Signal: active
⇧	»ExBlo«	Signal: External Blocking
⇧	»Alarm«	Signal: Alarm Trip Circuit Supervision
⇧	»Not Possible«	Not possible because no state indicator assigned to the breaker.
⇩	»Aux ON-I«	Module Input State: Position indicator/check-back signal of the CB (52a)
⇩	»Aux OFF-I«	Module input state: Position indicator/check-back signal of the CB (52b)
⇩	»ExBlo1-I«	Module input state: External blocking1
⇩	»ExBlo2-I«	Module input state: External blocking2

3.1.3.11.3 Operation / Status Display / Supervision / VTS

⇧	»Active«	Signal: active
⇧	»ExBlo«	Signal: External Blocking
⇧	»Alarm ΔV«	Signal: Alarm ΔV Voltage Transformer Measuring Circuit Supervision
⇧	»Alarm«	Signal: Alarm Voltage Transformer Measuring Circuit Supervision
⇧	»Ex FF VT«	Signal: Ex FF VT
⇧	»Ex FF EVT«	Signal: Alarm Fuse Failure Earth Voltage Transformers
⇩	»Ex Fuse Fail VT-I«	Module input state: External fuse failure voltage transformers
⇩	»Ex Fuse Fail EVT-I«	Module input state: External fuse failure earth voltage transformer
⇩	»ExBlo1-I«	Module input state: External blocking1
⇩	»ExBlo2-I«	Module input state: External blocking2

3.1.3.11.4 Operation / Status Display / Supervision / Phase Sequence

⇧	»VT . Phase seq. wrong«	Signal that the device has detected a phase sequence (L1-L2-L3 / L1-L3-L2) that is different from the one that had been set at [Field settings / General Settings] »Phase Sequence«.

3.1.3.12 Operation / Status Display / Logics

⇧	»LE1.Gate Out« ... »LE80.Gate Out«	Signal: Output of the logic gate
⇧	»LE1.Timer Out« ... »LE80.Timer Out«	Signal: Timer Output
⇧	»LE1.Out« ... »LE80.Out«	Signal: Latched Output (Q)
⇧	»LE1.Out inverted« ... »LE80.Out inverted«	Signal: Negated Latched Output (Q NOT)
⇩	»LE1.Gate In1-I« ... »LE80.Gate In4-I«	State of the module input: Assignment of the Input Signal
⇩	»LE1.Reset Latch-I«	State of the module input: Reset Signal for the Latching

	... »LE80.Reset Latch-I«	

3.1.3.13 Operation / Status Display / DI Slot X1

	»DI 1«	Signal: Digital Input
	»DI 2«	Signal: Digital Input
	»DI 3«	Signal: Digital Input
	»DI 4«	Signal: Digital Input
	»DI 5«	Signal: Digital Input
	»DI 6«	Signal: Digital Input
	»DI 7«	Signal: Digital Input
	»DI 8«	Signal: Digital Input

3.1.3.14 Operation / Status Display / BO Slot X2

	»BO 1«	Signal: Binary Output Relay
	»BO 2«	Signal: Binary Output Relay
	»BO 3«	Signal: Binary Output Relay
	»BO 4«	Signal: Binary Output Relay
	»BO 5«	Signal: Binary Output Relay
	»DISARMED!«	Signal: CAUTION! RELAYS DISARMED in order to safely perform maintenance while eliminating the risk of taking an entire process off-line. (Note: The Self Supervision Contact cannot be disarmed). YOU MUST ENSURE that the relays are ARMED AGAIN after maintenance
	»Outs forced«	Signal: The State of at least one Relay Output has been set by force. That means that the state of at least one Relay is forced and hence does not show the state of the assigned signals.

3.1.3.15 Operation / Status Display / Recorders

3.1.3.15.1 Operation / Status Display / Recorders / Event rec

	»Res all records«	Signal: All records are being deleted. (Remark: Immediately afterwards, this signal becomes inactive again.)

3.1.3.15.2 Operation / Status Display / Recorders / Disturb rec

	»Rec state«	Recording state
	»Error code«	Error code
	»recording«	Signal: Recording
	»memory full«	Signal: Memory full
	»Clear fail«	Signal: Clear failure in memory
	»Res all records«	Signal: All records are being deleted. (Remark: Immediately afterwards, this signal becomes inactive again.)
	»Res record«	Signal: Delete record
	»Man Trigger«	Signal: Manual Trigger
	»Start1-I«	State of the module input:: Trigger event / start recording
	»Start2-I«	State of the module input:: Trigger event / start recording
	»Start3-I«	State of the module input:: Trigger event / start recording
	»Start4-I«	State of the module input:: Trigger event / start recording
	»Start5-I«	State of the module input:: Trigger event / start recording
	»Start6-I«	State of the module input:: Trigger event / start recording
	»Start7-I«	State of the module input:: Trigger event / start recording
	»Start8-I«	State of the module input:: Trigger event / start recording

3.1.3.15.3 Operation / Status Display / Recorders / Fault rec

	»Res record«	Signal: Delete record

3.1.3.15.4 Operation / Status Display / Recorders / Trend rec

	»Res all records«	Signal: All records are being deleted. (Remark: Immediately afterwards, this signal becomes inactive again.)

3.1.3.16 Operation / Status Display / Scada

	»SCADA connected«	At least one SCADA System is connected to the device.
	»SCADA not connected«	No SCADA System is connected to the device

3.1.3.17 Operation / Status Display / Red.Ethernet

	»Uplink A«	Uplink A
	»OpenRingA«	Open HSR ring detected on port A. A
	»Duplex mode A«	Duplex mode
	»Speed A«	Speed
	»Uplink B«	Uplink B
	»OpenRingB«	Open HSR ring detected on port A. B
	»Duplex mode B«	Duplex mode
	»Speed B«	Speed

3.1.3.18 Operation / Status Display / DNP3

3.1.3.18.1 Operation / Status Display / DNP3 / State

	»busy«	This message is set if the protocol is started. It will be reset if the protocol is shut down.
	»ready«	The message will be set if the protocol is successfully started and ready for data exchange.
	»Active«	The communication with the Master (SCADA) is active. Note that for TCP/UDP, this state is permanently “Low” unless »DataLink confirm« is set to “Always”.

3.1.3.18.2 Operation / Status Display / DNP3 / Binary Inputs

	»BinaryInput0-I« ... »BinaryInput63-I«	Virtual Digital Input (DNP). This corresponds to a virtual binary output of the protective device.

3.1.3.18.3 Operation / Status Display / DNP3 / Double Bit Inputs

⇩	»DoubleBitInput0-I«	Double Bit Digital Input (DNP). This corresponds to a double bit binary output of the protective device.
⇩	»DoubleBitInput1-I«	Double Bit Digital Input (DNP). This corresponds to a double bit binary output of the protective device.
⇩	»DoubleBitInput2-I«	Double Bit Digital Input (DNP). This corresponds to a double bit binary output of the protective device.
⇩	»DoubleBitInput3-I«	Double Bit Digital Input (DNP). This corresponds to a double bit binary output of the protective device.
⇩	»DoubleBitInput4-I«	Double Bit Digital Input (DNP). This corresponds to a double bit binary output of the protective device.
⇩	»DoubleBitInput5-I«	Double Bit Digital Input (DNP). This corresponds to a double bit binary output of the protective device.

3.1.3.19 Operation / Status Display / Modbus

3.1.3.19.1 Operation / Status Display / Modbus / State

⇧	»Transmission RTU«	Signal: SCADA active
⇧	»Transmission TCP«	Signal: SCADA active
⇧	»Device Type«	Device type code for relationship between device name and its Modbus code. HighPROTEC: MRI4 - 1000 MRU4 - 1001 MRA4 - 1002 MCA4 - 1003 MRDT4 - 1005 MCDTV4 - 1006 MCDGV4 - 1007 MRM4 - 1009 MRMV4 - 1010 MCDLV4 - 1011
⇧	»Comm Version«	Modbus Communication version. This version number changes if something becomes incompatible between different Modbus releases.

3.1.3.19.2 Operation / Status Display / Modbus / Commands

⇧	»Scada Cmd 1«	Scada Command
⇧	»Scada Cmd 2«	Scada Command
⇧	»Scada Cmd 3«	Scada Command
⇧	»Scada Cmd 4«	Scada Command
⇧	»Scada Cmd 5«	Scada Command
⇧	»Scada Cmd 6«	Scada Command
⇧	»Scada Cmd 7«	Scada Command
⇧	»Scada Cmd 8«	Scada Command
⇧	»Scada Cmd 9«	Scada Command
⇧	»Scada Cmd 10«	Scada Command
⇧	»Scada Cmd 11«	Scada Command
⇧	»Scada Cmd 12«	Scada Command
⇧	»Scada Cmd 13«	Scada Command
⇧	»Scada Cmd 14«	Scada Command
⇧	»Scada Cmd 15«	Scada Command
⇧	»Scada Cmd 16«	Scada Command

3.1.3.19.3 Operation / Status Display / Modbus / Configb Registers

⇩	»Config Bin Inp1-I« ... »Config Bin Inp32-I«	State of the module input: Config Bin Inp

3.1.3.20 Operation / Status Display / IEC 61850

3.1.3.20.1 Operation / Status Display / IEC 61850 / State

⇗	»GoosePublisherState«	State of the GOOSE Publisher (on or off)
⇗	»GooseSubscriberState«	State of the GOOSE Subscriber (on or off)
⇗	»MmsServerState«	State of MMS Server (on or off)
⇧	»MMS Client connected«	At least one MMS client is connected to the device
⇧	»All Goose Subscriber active«	All Goose subscriber in the device are working

3.1.3.20.2 Operation / Status Display / IEC 61850 / ControlInputs

⇧	»CTLGGIO1.SPCSO1.stVal« ... »CTLGGIO1.SPCSO32.stVal«	Status bit that can be set by clients like e.g. SCADA (Single Point Controllable Status Output).

3.1.3.20.3 Operation / Status Display / IEC 61850 / Virtual Inputs 1

⇧	»GOSINGGIO1.Ind1.stVal« ... »GOSINGGIO1.Ind32.stVal«	Signal: Virtual Input (IEC61850 GGIO Ind): State
⇧	»GOSINGGIO1.Ind1.q« ... »GOSINGGIO1.Ind32.q«	Signal: Virtual Input (IEC61850 GGIO Ind): Self-Supervision of the GGIO Input

3.1.3.20.4 Operation / Status Display / IEC 61850 / Virtual Inputs 2

⇧	»GOSINGGIO2.Ind1.stVal« ... »GOSINGGIO2.Ind32.stVal«	Signal: Virtual Input (IEC61850 GGIO Ind): State
⇧	»GOSINGGIO2.Ind1.q« ... »GOSINGGIO2.Ind32.q«	Signal: Virtual Input (IEC61850 GGIO Ind): Self-Supervision of the GGIO Input

3.1.3.20.5 Operation / Status Display / IEC 61850 / Virtual Outputs 1

⇩	»COUTGGIO1.Ind1.stVal-I« ... »COUTGGIO1.Ind32.stVal-I«	Module input state: Binary state of the Virtual Output (GGIO)

3.1.3.20.6 Operation / Status Display / IEC 61850 / Virtual Outputs 2

⇩	»COUTGGIO2.Ind1.stVal-I« ... »COUTGGIO2.Ind32.stVal-I«	Module input state: Binary state of the Virtual Output (GGIO)

3.1.3.21 Operation / Status Display / IEC103

⇧	»Scada Cmd 1«	Scada Command
⇧	»Scada Cmd 2«	Scada Command
⇧	»Scada Cmd 3«	Scada Command
⇧	»Scada Cmd 4«	Scada Command
⇧	»Scada Cmd 5«	Scada Command
⇧	»Scada Cmd 6«	Scada Command
⇧	»Scada Cmd 7«	Scada Command
⇧	»Scada Cmd 8«	Scada Command
⇧	»Scada Cmd 9«	Scada Command
⇧	»Scada Cmd 10«	Scada Command
⇧	»Transmission«	Signal: SCADA active
⇧	»Failure Event lost«	Failure event lost
⇧	»Test mode active«	Signal: IEC103 communication has been switched over into Test Mode.
⇧	»Block MD active«	Signal: The blocking of IEC103 transmission in monitor direction has been activated.

3.1.3.22 Operation / Status Display / IEC104

⇧	»Scada Cmd 1« ... »Scada Cmd 16«	Scada Command
⇧	»busy«	This message is set if the protocol is started. It will be reset if the protocol is shut down.
⇧	»ready«	The message will be set if the protocol is successfully started and ready for data exchange.
⇧	»Transmission«	Signal: SCADA active
⇧	»Failure Event lost«	Failure event lost

3.1.3.23 Operation / Status Display / Profibus

3.1.3.23.1 Operation / Status Display / Profibus / State

	»Data OK«	Data within the Input field are OK (Yes=1)
	»SubModul Err«	Assignable Signal, Failure in Sub-Module, Communication Failure.
	»Connection active«	Connection active
	»Slave State«	Communication State between Slave and Master.
	»Baud rate«	The baud rate that has been detected lastly, will still be shown after a connection issue.
	»PNO Id«	PNO Identification Number. GSD Identification Number.
	»Master ID«	Device address (Master ID) within the bus system. Each device address has to be unique within a bus system.
	»HO Id PSub«	Handoff Id of PbSub
	»t-WatchDog«	The Profibus Chip detects a communication issue if this timer is expired without any communication (Parameterising telegram).
	»Config info«	Configuration comment (entered by the user during SCADA configuration)
	»Config version«	Version of the user-defined SCADA configuration
	»Config status«	Status of the user-defined SCADA configuration. Possible values:
	»Slave ID«	Device address (Slave ID) within the bus system. Each device address has to be unique within a bus system.

3.1.3.23.2 Operation / Status Display / Profibus / Commands

	»Scada Cmd 1«	Scada Command
	»Scada Cmd 2«	Scada Command
	»Scada Cmd 3«	Scada Command
	»Scada Cmd 4«	Scada Command
	»Scada Cmd 5«	Scada Command
	»Scada Cmd 6«	Scada Command
	»Scada Cmd 7«	Scada Command
	»Scada Cmd 8«	Scada Command
	»Scada Cmd 9«	Scada Command
	»Scada Cmd 10«	Scada Command
	»Scada Cmd 11«	Scada Command
	»Scada Cmd 12«	Scada Command
	»Scada Cmd 13«	Scada Command
	»Scada Cmd 14«	Scada Command
	»Scada Cmd 15«	Scada Command
	»Scada Cmd 16«	Scada Command

3.1.3.23.3 Operation / Status Display / Profibus / ConfigBinInp 1-16

	»Assignment 1-I«	Module input state: Scada Assignment
	»Assignment 2-I«	Module input state: Scada Assignment
	»Assignment 3-I«	Module input state: Scada Assignment
	»Assignment 4-I«	Module input state: Scada Assignment
	»Assignment 5-I«	Module input state: Scada Assignment
	»Assignment 6-I«	Module input state: Scada Assignment
	»Assignment 7-I«	Module input state: Scada Assignment
	»Assignment 8-I«	Module input state: Scada Assignment
	»Assignment 9-I«	Module input state: Scada Assignment
	»Assignment 10-I«	Module input state: Scada Assignment
	»Assignment 11-I«	Module input state: Scada Assignment
	»Assignment 12-I«	Module input state: Scada Assignment
	»Assignment 13-I«	Module input state: Scada Assignment
	»Assignment 14-I«	Module input state: Scada Assignment
	»Assignment 15-I«	Module input state: Scada Assignment
	»Assignment 16-I«	Module input state: Scada Assignment

3.1.3.23.4 Operation / Status Display / Profibus / ConfigBinInp 17-32

⇩	»Assignment 17-I«	Module input state: Scada Assignment
⇩	»Assignment 18-I«	Module input state: Scada Assignment
⇩	»Assignment 19-I«	Module input state: Scada Assignment
⇩	»Assignment 20-I«	Module input state: Scada Assignment
⇩	»Assignment 21-I«	Module input state: Scada Assignment
⇩	»Assignment 22-I«	Module input state: Scada Assignment
⇩	»Assignment 23-I«	Module input state: Scada Assignment
⇩	»Assignment 24-I«	Module input state: Scada Assignment
⇩	»Assignment 25-I«	Module input state: Scada Assignment
⇩	»Assignment 26-I«	Module input state: Scada Assignment
⇩	»Assignment 27-I«	Module input state: Scada Assignment
⇩	»Assignment 28-I«	Module input state: Scada Assignment
⇩	»Assignment 29-I«	Module input state: Scada Assignment
⇩	»Assignment 30-I«	Module input state: Scada Assignment
⇩	»Assignment 31-I«	Module input state: Scada Assignment
⇩	»Assignment 32-I«	Module input state: Scada Assignment

3.1.3.24 Operation / Status Display / TimeSync

3.1.3.24.1 Operation / Status Display / TimeSync / TimeSync

⇧	»synchronized«	Clock is synchronized.

3.1.3.24.2 Operation / Status Display / TimeSync / PTP

⇧	»PTP active«	PTP active
⇘	»Master ID«	Grandmaster Clock ID
⇘	»Sync Status«	Synchronization Status
⇘	»Delay mech.«	Path delay mechanism
⇘	»Path delay time«	Path delay time
⇘	»PathDelay PortA«	Path delay time PortA
⇘	»PathDelay PortB«	PathDelay PortB
⇘	»Offs.«	Offset
⇘	»Drift«	Drift

3.1.3.24.3 Operation / Status Display / TimeSync / IRIG-B

⇧	»IRIG-B active«	Signal: If there is no valid IRIG-B signal for 60 sec, IRIG-B is regarded as inactive.
⇧	»High-Low Invert«	Signal: The High and Low signals of the IRIG-B are inverted. This does NOT mean that the wiring is faulty. If the wiring is faulty no IRIG-B signal will be detected.
⇧	»Control Signal1« ... »Control Signal18«	Signal: IRIG-B Control Signal. The external IRIG-B generator can set these signals. They can be used for further control procedures inside the device (e.g. logic funtions).

3.1.3.24.4 Operation / Status Display / TimeSync / SNTP

⇧	»SNTP active«	Signal: If there is no valid SNTP signal for 120 sec, SNTP is regarded as inactive.
⟋	»Used Server«	Which Server is used for SNTP synchronization.
#	»StratumServer1«	Stratum of Server 1
⟋	»PrecServer1«	Precision of Server 1
#	»StratumServer2«	Stratum of Server 2
⟋	»PrecServer2«	Precision of Server 2
⟋	»ServerQlty«	Quality of Server used for Synchronization (GOOD, SUFFICIENT, BAD)
⟋	»NetConn«	Quality of Network Connection (GOOD, SUFFICIENT, BAD).

3.1.3.25 Operation / Status Display / SysA

⇧	»Active«	Signal: active
⇧	»ExBlo«	Signal: External Blocking
⇧	»Alarm V THD«	Signal: Alarm Total Harmonic Distortion Voltage
⇧	»Trip V THD«	Signal: Trip Total Harmonic Distortion Voltage
⇩	»ExBlo-I«	Module input state: External blocking

3.1.3.26 Operation / Status Display / Syslog

⇧	»Active«	Signal: active

3.1.3.27 Operation / Status Display / Statistics

⇧	»ResFc all«	Signal: Resetting of all Statistic values (Current Demand, Power Demand, Min, Max)
⇧	»ResFc Vavg«	Signal: Resetting of the sliding average calculation.
⇧	»ResFc Max«	Signal: Resetting of all Maximum values
⇧	»ResFc Min«	Signal: Resetting of all Minimum values
⇩	»StartFc Vavg-I«	State of the module input: Start of Statistics Average Voltage

3.1.3.28 Operation / Status Display / Sys

⇧	»Reboot«	Signal: Rebooting the device. Device Start-up Codes: 1=Normal Start-up; 2=Reboot by the Operator; 3=Reboot by means of Super Reset; 4=outdated; 5=outdated; 6=Unknown Error Source; 7=Forced Reboot (initiated by the main processor); 8=Exceeded Time Limit of the Protection Cycle; 9= Forced Reboot (initiated by the digital signal processor); 10=Exceeded Time Limit of the Measured Value Processing; 11=Sags of the Supply Voltage; 12=Illegal Memory Access.
⇧	»Act Set«	Signal: Active Parameter Set
⇧	»PS 1«	Signal: The currently active Parameter Set is PS 1
⇧	»PS 2«	Signal: The currently active Parameter Set is PS 2
⇧	»PS 3«	Signal: The currently active Parameter Set is PS 3
⇧	»PS 4«	Signal: The currently active Parameter Set is PS 4
⇧	»PSS manual«	Signal: Manual Switch over of a Parameter Set
⇧	»PSS via Scada«	Signal: Parameter Set Switch via Scada. Write into this output byte the integer of the parameter set that should become active (e.g. 4 => Switch onto parameter set 4).
⇧	»PSS via Inp fct«	Signal: Parameter Set Switch via input function
⇧	»min 1 param changed«	Signal: At least one parameter has been changed
⇧	»Setting Lock Bypass«	Signal: Short-period unlock of the Setting Lock
⇧	»Maint Mode Active«	Signal: Arc Flash Reduction Maintenance Active
⇧	»Maint Mode Inactive«	Signal: Arc Flash Reduction Maintenance Inactive
⇧	»MaintMode Manually«	Signal: Arc Flash Reduction Maintenance Manual Mode
⇧	»Maint Mode SCADA«	Signal: Arc Flash Reduction Maintenance SCADA Mode
⇧	»Maint Mode DI«	Signal: Arc Flash Reduction Maintenance Digital Input Mode
⇧	»Ack LED«	Signal: LEDs acknowledgement
⇧	»Ack BO«	Signal: Acknowledgement of the Binary Outputs
⇧	»Ack Scada«	Signal: Acknowledge latched SCADA signals
⇧	»Ack TripCmd«	Signal: Reset Trip Command
⇧	»Ack LED-HMI«	Signal: LEDs acknowledgement, triggered at the HMI
⇧	»Ack BO-HMI«	Signal: Acknowledgement of the Binary Outputs, triggered at the HMI

⇧	»Ack Scada-HMI«	Signal: Acknowledge latched SCADA signals, triggered at the HMI
⇧	»Ack TripCmd-HMI«	Signal: Reset Trip Command, triggered at the HMI
⇧	»Ack LED-Sca«	Signal: LEDs acknowledgement, triggered via SCADA
⇧	»Ack BO-Sca«	Signal: Acknowledgement of the Binary Outputs, triggered via SCADA
⇧	»Ack Counter-Sca«	Signal: Reset of all Counters, triggered via SCADA
⇧	»Ack Scada-Sca«	Signal: Acknowledge latched SCADA signals, triggered via SCADA
⇧	»Ack TripCmd-Sca«	Signal: Reset Trip Command, triggered via SCADA
⇧	»Res OperationsCr«	Signal:: Res OperationsCr
⇧	»Res AlarmCr«	Signal:: Res AlarmCr
⇧	»Res TripCmdCr«	Signal:: Res TripCmdCr
⇧	»Res TotalCr«	Signal:: Res TotalCr
⇩	»Ack LED-I«	Module input state: LEDs acknowledgement by digital input
⇩	»Ack BO-I«	Module input state: Acknowledgement of the binary Output Relays
⇩	»Ack Scada-I«	Module input state: Acknowledge latched SCADA signals.
⇩	»PS1-I«	State of the module input respectively of the signal, that should activate this Parameter Setting Group.
⇩	»PS2-I«	State of the module input respectively of the signal, that should activate this Parameter Setting Group.
⇩	»PS3-I«	State of the module input respectively of the signal, that should activate this Parameter Setting Group.
⇩	»PS4-I«	State of the module input respectively of the signal, that should activate this Parameter Setting Group.
⇩	»Setting Lock-I«	State of the module input: No parameters can be changed as long as this input is true. The parameter settings are locked.
⇩	»Maint Mode-I«	Module Input State: Arc Flash Reduction Maintenance Switch

3.1.3.29 Operation / Status Display / Sgen

⇧	»Manual Start«	Fault Simulation has been started manually.
⇧	»Manual Stop«	Fault Simulation has been stopped manually.
⇧	»Running«	Signal: Measuring value simulation is running
⇧	»Started«	Fault Simulation has been started
⇧	»Stopped«	Fault Simulation has been stopped
⇧	»State«	Signal: Wave generation states: 0=Off, 1=PreFault, 2=Fault, 3=PostFault, 4=InitReset
⇩	»Ex Start Simulation-I«	State of the module input:External Start of Fault Simulation (Using the test parameters)
⇩	»ExBlo1-I«	Module input state: External blocking1
⇩	»ExBlo2-I«	Module input state: External blocking2
⇩	»Ex ForcePost-I«	State of the module input:Force Post state. Abort simulation.

3.1.4 Operation / Count and RevData

3.1.4.1 Operation / Count and RevData / Prot

⇧	»Fault No.«	Fault number

3.1.4.2 Operation / Count and RevData / Control

3.1.4.2.1 Operation / Count and RevData / Control / Ctrl

⇘	»Switch.Cmds per s«	The number of switching commands per second. (This is mainly an internal diagnosis value.)
⇘	»Rej. Switch.Cmds«	The percentage of rejected switching commands per second. (This is mainly an internal diagnosis value.)
⇘	»Switch.Cmds max«	The maximum number of switching commands per second. (This is mainly an internal diagnosis value.)
⇘	»Rej.Swtch.Cmds max«	The maximum percentage of rejected switching commands per second. (This is mainly an internal diagnosis value.)

3.1.4.2.2 Operation / Count and RevData / Control / SG[1]

#	»TripCmd Cr«	Counter: Total number of trips of the switchgear.

3.1.4.3 Operation / Count and RevData / LVRT[1]

#	»Num Vdips in t-LVRT«	Number of Voltage dips during t-LVRT
#	»Cr Tot Numb of Vdips«	Counter Total number of voltage dips.
#	»Cr Num Vdips to Trip«	Counter Total number of voltage dips that caused a Trip

3.1.4.4 Operation / Count and RevData / LVRT[2]

#	»Num Vdips in t-LVRT«	Number of Voltage dips during t-LVRT
#	»Cr Tot Numb of Vdips«	Counter Total number of voltage dips.
#	»Cr Num Vdips to Trip«	Counter Total number of voltage dips that caused a Trip

3.1.4.5 Operation / Count and RevData / Red.Ethernet

#	»DiagCounter1_«	Number of total requests (all slave addresses on bus)_
#	»DiagCounter2_«	Number of requests for this slave address_
#	»DiagCounter3_«	Number of total response messages_
#	»DiagCounter4_«	Number of total response messages_
#	»DiagCounter5_«	Number of total response messages_
#	»DiagCounter6_«	Number of total response messages_
#	»DiagCounter7_«	Number of total response messages_
#	»DiagCounter8_«	Number of total response messages_
#	»CountSentFramesA«	Number of frames sent on port A.
#	»CountSentFramesB«	Number of frames sent on port B.
#	»CountResFramesA«	Number of frames received on port A.
#	»CountResFramesB«	Number of frames received on port B.
#	»CountErrorPA«	Number of errors on port A.
#	»CountErrorPB«	Number of errors on port B.
#	»CountMissDupl«	Number of missing duplicated frames.
#	»MaxDuplFrDelay«	Max delay time of a duplicated frames.
#	»CountTxMsg«	Total number of received frames.
#	»CountRxMsg«	Total number of sent frames.
#	»CountDuplMsg«	Total number of duplicate frames rejected in software.
#	»CountSigMapOverflow«	Total number of forced erase entries from Rx frame signature map.
#	»MaxSigMapEntries«	Maximum reached size of Rx frame signature map.
#	»CountSigMapEntries«	Current size of Rx frame signature map.

3.1.4.6 Operation / Count and RevData / Profibus

#	»Fr Sync Err«	Frames, that were sent from the Master to the Slave are faulty.
#	»Num. CRC err.«	Number of CRC errors that the subsystem manager has recognized in the received response frames from the subsystem. (Each error caused a subsystem reset.)
#	»Num. frame loss err.«	Number of frame loss errors that the subsystem manager has recognized in the received response frames from the subsystem. (Each error caused a subsystem reset.)
#	»Num. trig. CRC err.«	Number of CRC errors that the subsystem has recognized in the received trigger frames from the host.
#	»Num. subsys. res.«	Number of subsystem restarts or resets that the subsystem manager has caused.

3.1.4.7 Operation / Count and RevData / DNP3

#	»NReceived«	Diagnostic counter: Number of received characters
#	»NSent«	Diagnostic counter: Number of sent characters
#	»NBadFramings«	Diagnostic counter: Number of bad framings. A large number indicates a disturbed serial connection.
#	»NBadParities«	Diagnostic counter: Number of parity errrors. A large number indicates a disturbed serial connection.
#	»NBreakSignals«	Diagnostic counter: Number of break signals. A large number indicates a disturbed serial connection.
#	»NBadChecksum«	Diagnostic counter: Number of frames received with bad checksum.
◉	»Res all Diag Cr«	Reset all diagnosis counters

3.1.4.8 Operation / Count and RevData / Modbus

3.1.4.8.1 Operation / Count and RevData / Modbus / TCP

#	»NoOfRequestsTotal«	Total number of requests. Includes requests for other slaves.
#	»NoOfReqForMe«	Total Number of requests for this slave.
#	»NoOfResponse«	Total number of requests having been responded.
#	»NoOfQueryInvalid«	Total number of Request errors. Request could not be interpreted
#	»NoOfInternalError«	Total Number of Internal errors while interpreting the request.

3.1.4.8.2 Operation / Count and RevData / Modbus / RTU

#	»NoOfRequestsTotal«	Total number of requests. Includes requests for other slaves.
#	»NoOfReqForMe«	Total Number of requests for this slave.
#	»NoOfResponse«	Total number of requests having been responded.
#	»NoOfFrameErrors«	Total Number of Frame Errors. Physically corrupted Frame.
#	»NoOfParityErrors«	Total number of parity errors. Physically corrupted Frame.
#	»NoOfRespTimeOverruns«	Total number of requests with exceeded response time. Physically corrupted Frame.
#	»NoOfOverrunErros«	Total Number of Overrun Failures. Physically corrupted Frame.
#	»NoOfBreaks«	Number of detected communication aborts

3.1.4.8.3 Operation / Count and RevData / Modbus / Measured Values

	»Mapped Meas 1«	Mapped Measured Values. They can be used to provide measured values to the Modbus Master.
	»Mapped Meas 2«	Mapped Measured Values. They can be used to provide measured values to the Modbus Master.
	»Mapped Meas 3«	Mapped Measured Values. They can be used to provide measured values to the Modbus Master.
	»Mapped Meas 4«	Mapped Measured Values. They can be used to provide measured values to the Modbus Master.
	»Mapped Meas 5«	Mapped Measured Values. They can be used to provide measured values to the Modbus Master.
	»Mapped Meas 6«	Mapped Measured Values. They can be used to provide measured values to the Modbus Master.
	»Mapped Meas 7«	Mapped Measured Values. They can be used to provide measured values to the Modbus Master.
	»Mapped Meas 8«	Mapped Measured Values. They can be used to provide measured values to the Modbus Master.
	»Mapped Meas 9«	Mapped Measured Values. They can be used to provide measured values to the Modbus Master.
	»Mapped Meas 10«	Mapped Measured Values. They can be used to provide measured values to the Modbus Master.
	»Mapped Meas 11«	Mapped Measured Values. They can be used to provide measured values to the Modbus Master.
	»Mapped Meas 12«	Mapped Measured Values. They can be used to provide measured values to the Modbus Master.
	»Mapped Meas 13«	Mapped Measured Values. They can be used to provide measured values to the Modbus Master.
	»Mapped Meas 14«	Mapped Measured Values. They can be used to provide measured values to the Modbus Master.
	»Mapped Meas 15«	Mapped Measured Values. They can be used to provide measured values to the Modbus Master.
	»Mapped Meas 16«	Mapped Measured Values. They can be used to provide measured values to the Modbus Master.

3.1.4.9 Operation / Count and RevData / IEC 61850

#	»NoOfGooseRxAll«	Total number of received GOOSE messages including messages for other devices (subscribed and not subscribed messages).
#	»NoOfGooseRxSubscribed«	Total Number of subscribed GOOSE messages including messages with incorrect content.
#	»NoOfGooseRxCorrect«	Total Number of subscribed and correctly received GOOSE messages.
#	»NoOfGooseRxNew«	Number of subscribed and correctly received GOOSE messages with new content.
#	»NoOfGooseTxAll«	Total Number of GOOSE messages that have been published by this device.
#	»NoOfGooseTxNew«	Total Number of new GOOSE messages (modified content) that have been published by this device.
#	»NoOf Srv.Req.All«	Total number of MMS Server requests including incorrect requests.
#	»NoOfDataReadAll«	Total Number of values read from this device including incorrect requests.
#	»NoOfDataReadCorrect«	Total Number of correctly read values from this device.
#	»NoOfDataWrittenAll«	Total Number of values written by this device including incorrect ones.
#	»NoOfDataWrittenCorrect«	Total Number of correctly written values by this device.
#	»NoOfDataChangeNotification«	Number of detected changes within the datasets that are published with GOOSE messages.
#	»No of Client Connections«	Number of active MMS client connections

3.1.4.10 Operation / Count and RevData / IEC103

#	»NReceived«	Total Number of received Messages
#	»NSent«	Total Number of sent Messages
#	»NBadFramings«	Number of bad Messages
#	»NBadParities«	Number of Parity Errors
#	»NBreakSignals«	Number of transmission errors with respect to the (electric) signal transport (physical layer). If the counter value gets increased constantly you should check for problems with the electrical connection (e.g. missing termination impedance of the serial interface), and make sure the transmission parameters (especially the baud rate) are correct.
#	»NInternalError«	Number of Internal Errors
#	»NBadCharChecksum«	Number of Checksum Errors

3.1.4.11 Operation / Count and RevData / IEC104

#	»NReceived«	Diagnostic counter: Number of received characters
#	»NSent«	Diagnostic counter: Number of sent characters
#	»Num. of lost conn.«	Diagnostic counter: Number of lost connections
#	»NBadChecksum«	Diagnostic counter: Number of frames received with bad checksum.

3.1.4.12 Operation / Count and RevData / TimeSync

3.1.4.12.1 Operation / Count and RevData / TimeSync / PTP

#	»Sync msg«	Sync message
#	»Sync followUp msg«	Sync follow up message
#	»Announce msg«	Announce message
#	»DelayReq Tx msg«	Delay request transmit message
#	»DelayResp Rx msg«	Delay response receive message
#	»PDelayReq Tx msg«	Peer delay request transmit message
#	»PDelayResp Rx msg«	Peer delay response receive message
#	»PDelayRespFolUp Rx msg«	Peer delay response follow up receive message
#	»PDelayReq Rx msg«	Peer delay request receive message
#	»PDelayResp Tx msg«	Peer delay response transmit message
#	»Unhandled Rx msg«	Unhandled receive message

3.1.4.12.2 Operation / Count and RevData / TimeSync / IRIG-B

#	»NoOfFramesOK«	Total Number valid Frames.
#	»NoOfFrameErrors«	Total Number of Frame Errors. Physically corrupted Frame.
#	»Edges«	Edges: Total number of rising and falling edges. This signal indicates if a signal is available at the IRIG-B input.

3.1.4.12.3 Operation / Count and RevData / TimeSync / SNTP

#	»NoOfSyncs«	Total Number of Synchronizations.
#	»NoOfConnectLost«	Total Number of lost SNTP Connections (no sync for 120 sec).
#	»NoOfSmallSyncs«	Service counter: Total Number of very small Time Corrections.
#	»NoOfNormSyncs«	Service counter: Total Number of normal Time Corrections
#	»NoOfBigSyncs«	Service counter: Total Number of big Time Corrections
#	»NoOfFiltSyncs«	Service counter: Total Number of filtered Time Corrections
#	»NoOfSlowTrans«	Service counter: Total Number of slow Transfers.
#	»NoOfHighOffs«	Service counter: Total Number of high Offsets.
#	»NoOfIntTimeouts«	Service counter: Total Number of internal timeouts.

3.1.4.13 Operation / Count and RevData / Trend rec

#	»Max avail Entries«	Maximum available entries in the current configuration

3.1.4.14 Operation / Count and RevData / Sys

	»Operating hours Cr«	Operating hours counter of the protective device

3.1.5 Operation / Recorders

	»Event rec«	The event recorder logs all events like switching operations, change of parameters, alarms, trips, operating mode selections, blockings and state transitions of inputs and outputs.
	»Disturb rec«	After a trigger event has become true, the disturbance recorder writes analogue and digital tracks
	»Fault rec«	The values measured at the time of tripping are saved by the Fault Recorder.
	»Trend rec«	Trend Recorder

3.1.5.1 Operation / Recorders / Man Trigger

	»Disturb rec . Man Trigger«	Manual Trigger

3.1.6 Operation / Security

	»Security Logger«	Security-related messages

3.1.6.1 Operation / Security / Security States

	»Sys . Smart view via USB«	Information whether or not the Smart view access via the USB interface is activated (allowed).
	»Sys . Smart view via Eth«	Information whether or not the Smart view access via the Ethernet interface is activated (allowed).
	»Modbus . Smart view via Modbus«	Activate (allow) or inactivate (disallow) the Smart view access via the Modbus tunnel.
	»Sys . Passw. for USB conn.«	Type / Security-level of the connection password that is used for a USB connection.
	»Sys . Passw.remote net.conn. «	Type / Security-level of the connection password that is used for a Smart view connection via some network interface.
	»Sys . TLS Certificate«	Type of certificate that the device uses for the encrypted communication. This value is directly related to the security-level of the communication.
	»Ctrl . Switching Authority«	Switching Authority
	»HMI . Conf. Dev. Reset«	If the »C« key is pressed while the device is performing a cold restart a general Reset Dialog appears on the screen. Select which options shall be available with this dialog.

3.1.7 Operation / Self-Supervision

	»Messages«	Internal messages

3.1.7.1 Operation / Self-Supervision / System State

	»System Error«	Signal: Device Failure
	»New error«	Signal: A new error message has been issued.
	»New warning«	Signal: A new warning message has been issued.
	»Test SC«	A drop of SelfSuperVision Contact (SC) has been triggered manually (for testing purposes).
	»SelfSuperVision Contact«	Signal: SelfSuperVision Contact
	»Cr No of free sockets«	Counter for network diagnosis. Number of free sockets.

3.1.8 Operation / Acknowledge

◉	»Sys . Ack BO LED Scd Trips«	Acknowledge (reset) latched binary output relays, LEDs, SCADA and Trips.
◉	»Sys . Ack LED«	All acknowledgeable LEDs will be acknowledged.
◉	»Sys . Ack BO«	All acknowledgeable binary output relays are acknowledged.
◉	»Sys . Ack Scada«	Latched SCADA signals are acknowledged.
◉	»SG[1] . Ack TripCmd«	Acknowledge Trip Command
◉	»SSV . Ack System LED «	Acknowledge System LED (red/green flashing LED)

3.1.9 Operation / Reset

◉	»Prot . Res FaultNo a GridFaultNo«	Resetting of fault number and grid fault number.
◉	»Ctrl . Reset max values«	Direct Command to reset the maximum values of: switching comands per second, and percentage of rejected commands.
◉	»SG[1] . Res SGwear Sl SG«	Resetting the slow Switchgear Alarm
◉	»SG[1] . Res TripCmd Cr«	Resetting of the Counter: Total number of trips of the switchgear
◉	»CBF . Res Lockout«	Reset Lockout
◉	»LVRT[1] . Res LVRT Cr«	Reset of the counter for the total number of voltage dips and reset of the counter of the total number of voltage dips that caused a trip.
◉	»LVRT[2] . Res LVRT Cr«	Reset of the counter for the total number of voltage dips and reset of the counter of the total number of voltage dips that caused a trip.
◉	»Statistics . ResFc all«	Resetting of all Statistic values (Current Demand, Power Demand, Min, Max)
◉	»Statistics . ResFc Max«	Resetting of all Maximum values
◉	»Statistics . ResFc Min«	Resetting of all Minimum values
◉	»Statistics . ResFc Vavg«	Resetting of the sliding average calculation.
◉	»DNP3 . Res all Diag Cr«	Reset all diagnosis counters
◉	»Red.Ethernet . Res Counter«	Reset all Counters.
◉	»PTP . Res Counter«	Reset all Counters.
◉	»Modbus . Res Diagn Cr«	All Modbus Diagnosis Counters will be reset.
◉	»Profibus . Reset Comds«	All Profibus Commands will be reset.
◉	»IEC103 . Res all Diag Cr«	Reset all diagnosis counters
◉	»IEC104 . Res all Diag Cr«	Reset all diagnosis counters
◉	»IRIG-B . Res IRIG-B Cr«	Resetting of the Diagnosis Counters: IRIG-B
◉	»SNTP . Res Counter«	Reset all Counters.
◉	»IEC 61850 . ResetStatistic«	Reset of all IEC61850 diagnostic counters
◉	»Event rec . Res all rec«	Reset all records
◉	»Disturb rec . Res all rec«	Reset all records

	»Fault rec . Res all rec«	Reset all records
	»Trend rec . Res all rec«	Reset all records

3.2 Device planning

3.2.1 Device planning / Projected Elements

	»V[1] . Mode«	Voltage-stage, general operation mode
	»V[2] . Mode«	Voltage-stage, general operation mode
	»V[3] . Mode«	Voltage-stage, general operation mode
	»V[4] . Mode«	Voltage-stage, general operation mode
	»V[5] . Mode«	Voltage-stage, general operation mode
	»V[6] . Mode«	Voltage-stage, general operation mode
	»df/dt . Mode«	Frequency Protection Module, general operation mode
	»delta phi . Mode«	Frequency Protection Module, general operation mode
	»Intertripping . Mode«	External Protection - Module, general operation mode
	»LVRT[1] . Mode«	general operation mode
	»LVRT[2] . Mode«	general operation mode
	»VG[1] . Mode«	Residual voltage-Stage, general operation mode
	»VG[2] . Mode«	Residual voltage-Stage, general operation mode
	»V012[1] . Mode«	Unbalance Protection: Supervision of the Voltage System
	»V012[2] . Mode«	Unbalance Protection: Supervision of the Voltage System
	»V012[3] . Mode«	Unbalance Protection: Supervision of the Voltage System
	»V012[4] . Mode«	Unbalance Protection: Supervision of the Voltage System
	»V012[5] . Mode«	Unbalance Protection: Supervision of the Voltage System
	»V012[6] . Mode«	Unbalance Protection: Supervision of the Voltage System
	»f[1] . Mode«	Frequency Protection Module, general operation mode
	»f[2] . Mode«	Frequency Protection Module, general operation mode
	»f[3] . Mode«	Frequency Protection Module, general operation mode
	»f[4] . Mode«	Frequency Protection Module, general operation mode
	»f[5] . Mode«	Frequency Protection Module, general operation mode
	»f[6] . Mode«	Frequency Protection Module, general operation mode
	»ReCon[1] . Mode«	general operation mode
	»ReCon[2] . Mode«	general operation mode
	»Sync . Mode«	Synchrocheck, general operation mode

	»ExP[1] . Mode«	External Protection - Module, general operation mode
	»ExP[2] . Mode«	External Protection - Module, general operation mode
	»ExP[3] . Mode«	External Protection - Module, general operation mode
	»ExP[4] . Mode«	External Protection - Module, general operation mode
	»CBF . Mode«	Module Circuit Breaker Failure protection, general operation mode
	»TCS . Mode«	Trip Circuit Supervision, general operation mode
	»VTS . Mode«	Voltage transformer supervision, general operation mode
	»SysA . Mode«	general operation mode
	»Syslog . Mode«	Syslog [Module for sending (device-internal) log messages to some server computer via network (UDP/IP)], general operation mode
	»Scada . Protocol«	Select the SCADA protocol to be used.
	»Red.Ethernet . Mode«	Redundant Ethernet, general operation mode
	»PTP . Mode«	PTP-Module, general operation mode
	»IRIG-B . Mode«	IRIG-B-Module, general operation mode
	»SNTP . Mode«	SNTP-Module, general operation mode
	»Logics . No of Equations:«	Number of required Logic Equations:
	»Sgen . Mode«	Sine wave generator, general operation mode

3.2.2 Device planning / Definition

	»V[1] . Superv. only«	Voltage-stage, if set to “Yes”: Restriction of the function to a supervision functionality, i.e. there is no general alarm, no general trip and no trip command.
	»V[2] . Superv. only«	Voltage-stage, if set to “Yes”: Restriction of the function to a supervision functionality, i.e. there is no general alarm, no general trip and no trip command.
	»V[3] . Superv. only«	Voltage-stage, if set to “Yes”: Restriction of the function to a supervision functionality, i.e. there is no general alarm, no general trip and no trip command.
	»V[4] . Superv. only«	Voltage-stage, if set to “Yes”: Restriction of the function to a supervision functionality, i.e. there is no general alarm, no general trip and no trip command.
	»V[5] . Superv. only«	Voltage-stage, if set to “Yes”: Restriction of the function to a supervision functionality, i.e. there is no general alarm, no general trip and no trip command.
	»V[6] . Superv. only«	Voltage-stage, if set to “Yes”: Restriction of the function to a supervision functionality, i.e. there is no general alarm, no general trip and no trip command.
	»df/dt . Superv. only«	Frequency Protection Module, if set to “Yes”: Restriction of the function to a supervision functionality, i.e. there is no general alarm, no general trip and no trip command.
	»delta phi . Superv. only«	Frequency Protection Module, if set to “Yes”: Restriction of the function to a supervision functionality, i.e. there is no general alarm, no general trip and no trip command.
	»LVRT[1] . Superv. only«	Low Voltage Ride Through, if set to “Yes”: Restriction of the function to a supervision functionality, i.e. there is no general alarm, no general trip and no trip command.

	»LVRT[2] . Superv. only«	Low Voltage Ride Through, if set to “Yes”: Restriction of the function to a supervision functionality, i.e. there is no general alarm, no general trip and no trip command.
	»VG[1] . Superv. only«	Residual voltage-Stage, if set to “Yes”: Restriction of the function to a supervision functionality, i.e. there is no general alarm, no general trip and no trip command.
	»VG[2] . Superv. only«	Residual voltage-Stage, if set to “Yes”: Restriction of the function to a supervision functionality, i.e. there is no general alarm, no general trip and no trip command.
	»V012[1] . Superv. only«	Symmetrical Components: Supervision of the Positive Phase Sequence or Negative Phase Sequence, if set to “Yes”: Restriction of the function to a supervision functionality, i.e. there is no general alarm, no general trip and no trip command.
	»V012[2] . Superv. only«	Symmetrical Components: Supervision of the Positive Phase Sequence or Negative Phase Sequence, if set to “Yes”: Restriction of the function to a supervision functionality, i.e. there is no general alarm, no general trip and no trip command.
	»V012[3] . Superv. only«	Symmetrical Components: Supervision of the Positive Phase Sequence or Negative Phase Sequence, if set to “Yes”: Restriction of the function to a supervision functionality, i.e. there is no general alarm, no general trip and no trip command.
	»V012[4] . Superv. only«	Symmetrical Components: Supervision of the Positive Phase Sequence or Negative Phase Sequence, if set to “Yes”: Restriction of the function to a supervision functionality, i.e. there is no general alarm, no general trip and no trip command.
	»V012[5] . Superv. only«	Symmetrical Components: Supervision of the Positive Phase Sequence or Negative Phase Sequence, if set to “Yes”: Restriction of the function to a supervision functionality, i.e. there is no general alarm, no general trip and no trip command.
	»V012[6] . Superv. only«	Symmetrical Components: Supervision of the Positive Phase Sequence or Negative Phase Sequence, if set to “Yes”: Restriction of the function to a supervision functionality, i.e. there is no general alarm, no general trip and no trip command.
	»f[1] . Superv. only«	Frequency Protection Module, if set to “Yes”: Restriction of the function to a supervision functionality, i.e. there is no general alarm, no general trip and no trip command.
	»f[2] . Superv. only«	Frequency Protection Module, if set to “Yes”: Restriction of the function to a supervision functionality, i.e. there is no general alarm, no general trip and no trip command.
	»f[3] . Superv. only«	Frequency Protection Module, if set to “Yes”: Restriction of the function to a supervision functionality, i.e. there is no general alarm, no general trip and no trip command.
	»f[4] . Superv. only«	Frequency Protection Module, if set to “Yes”: Restriction of the function to a supervision functionality, i.e. there is no general alarm, no general trip and no trip command.
	»f[5] . Superv. only«	Frequency Protection Module, if set to “Yes”: Restriction of the function to a supervision functionality, i.e. there is no general alarm, no general trip and no trip command.
	»f[6] . Superv. only«	Frequency Protection Module, if set to “Yes”: Restriction of the function to a supervision functionality, i.e. there is no general alarm, no general trip and no trip command.
	»ExP[1] . Superv. only«	External Protection - Module, if set to “Yes”: Restriction of the function to a supervision functionality, i.e. there is no general alarm, no general trip and no trip command.
	»ExP[2] . Superv. only«	External Protection - Module, if set to “Yes”: Restriction of the function to a supervision functionality, i.e. there is no general alarm, no general trip and no trip command.
	»ExP[3] . Superv. only«	External Protection - Module, if set to “Yes”: Restriction of the function to a supervision functionality, i.e. there is no general alarm, no general trip and no trip command.

	»ExP[4] . Superv. only«	External Protection - Module, if set to “Yes”: Restriction of the function to a supervision functionality, i.e. there is no general alarm, no general trip and no trip command.

3.3 Device Para

3.3.1 Device Para / Measurem Display

3.3.1.1 Device Para / Measurem Display / General Settings

	»Scaling«	Display of the measured values as primary, secondary or per unit values

3.3.1.2 Device Para / Measurem Display / Voltage

	»V Cutoff Level«	The Phase Voltage shown in the Display or within the PC Software will be displayed as zero, if the Phase Voltage falls below this Cutoff Level. This parameter has no impact on recorders. This parameter is related to the voltage that is connected to the device (phase-to-phase or phase-to-earth).
	»VG meas Cutoff Level«	The measured Residual Voltage shown in the Display or within the PC Software will be displayed as zero, if the measured Residual Voltage falls below this Cutoff Level. This parameter has no impact on recorders.
	»VG calc Cutoff Level«	The calculated Residual Voltage shown in the Display or within the PC Software will be displayed as zero, if the calculated Residual Voltage falls below this Cutoff Level. This parameter has no impact on recorders.
	»V012 Comp Cutoff Level«	The Symmetrical Component shown in the Display or within the PC Software will be displayed as zero, if the Symmetrical Component falls below this Cutoff Level. This parameter has no impact on recorders.

3.3.2 Device Para / Digital Inputs

3.3.2.1 Device Para / Digital Inputs / DI Slot X1

3.3.2.1.1 Device Para / Digital Inputs / DI Slot X1 / Group 1

	»Nom voltage«	Nominal voltage of the digital inputs
	»Inverting 1«	Inverting the input signals.
	»Debouncing time 1«	A state change at the input is recognised immediately and simultaneously the debouncing timer is started. The state remains stable while the timer is running. Only after the debouncing time has elapsed is another state change accepted and the timer restarted.

3.3.2.1.2 Device Para / Digital Inputs / DI Slot X1 / Group 2

	»Nom voltage«	Nominal voltage of the digital inputs
	»Inverting 2«	Inverting the input signals.
	»Debouncing time 2«	A state change at the input is recognised immediately and simultaneously the debouncing timer is started. The state remains stable while the timer is running. Only after the debouncing time has elapsed is another state change accepted and the timer restarted.

3.3.2.1.3 Device Para / Digital Inputs / DI Slot X1 / Group 3

	»Nom voltage«	Nominal voltage of the digital inputs
	»Inverting 3«	Inverting the input signals.
	»Inverting 4«	Inverting the input signals.
	»Inverting 5«	Inverting the input signals.
	»Inverting 6«	Inverting the input signals.
	»Inverting 7«	Inverting the input signals.
	»Inverting 8«	Inverting the input signals.
	»Debouncing time 3«	A state change at the input is recognised immediately and simultaneously the debouncing timer is started. The state remains stable while the timer is running. Only after the debouncing time has elapsed is another state change accepted and the timer restarted.
	»Debouncing time 4«	A state change at the input is recognised immediately and simultaneously the debouncing timer is started. The state remains stable while the timer is running. Only after the debouncing time has elapsed is another state change accepted and the timer restarted.
	»Debouncing time 5«	A state change at the input is recognised immediately and simultaneously the debouncing timer is started. The state remains stable while the timer is running. Only after the debouncing time has elapsed is another state change accepted and the timer restarted.
	»Debouncing time 6«	A state change at the input is recognised immediately and simultaneously the debouncing timer is started. The state remains stable while the timer is running. Only after the debouncing time has elapsed is another state change accepted and the timer restarted.
	»Debouncing time 7«	A state change at the input is recognised immediately and simultaneously the debouncing timer is started. The state remains stable while the timer is running. Only after the debouncing time has elapsed is another state change accepted and the timer restarted.
	»Debouncing time 8«	A state change at the input is recognised immediately and simultaneously the debouncing timer is started. The state remains stable while the timer is running. Only after the debouncing time has elapsed is another state change accepted and the timer restarted.

3.3.3 Device Para / Binary Outputs

3.3.3.1 Device Para / Binary Outputs / BO Slot X2

3.3.3.1.1 Device Para / Binary Outputs / BO Slot X2 / BO 1

	»Operating Mode«	Operating Mode
	»t-hold«	To clearly identify the state transition of a binary output relay, the "new state" is being hold, at least for the duration of the hold time.
	»t-Off Delay«	Switch Off Delay
	»Latched«	Defines whether the Relay Output will be latched when it picks up.
	»Acknowledgement«	Acknowledgement Signal - An acknowledgement signal (that acknowledges the corresponding binary output relay) can be assigned to each output relay. The acknowledgement-signal is only effective if the parameter "Latched" is set to active.
	»Inverting«	Inverting of the collective signal (OR-gate/disjunction). In combination with inverted input signals an AND-gate can be programmed (Conjunction).
	»Assignment 1« ... »Assignment 7«	Assignment
	»Inverting 1« ... »Inverting 7«	Inverting of the state of the assigned signal.

3.3.3.1.2 Device Para / Binary Outputs / BO Slot X2 / BO 2

	»Operating Mode«	Operating Mode
	»t-hold«	To clearly identify the state transition of a binary output relay, the "new state" is being hold, at least for the duration of the hold time.
	»t-Off Delay«	Switch Off Delay
	»Latched«	Defines whether the Relay Output will be latched when it picks up.
	»Acknowledgement«	Acknowledgement Signal - An acknowledgement signal (that acknowledges the corresponding binary output relay) can be assigned to each output relay. The acknowledgement-signal is only effective if the parameter "Latched" is set to active.
	»Inverting«	Inverting of the collective signal (OR-gate/disjunction). In combination with inverted input signals an AND-gate can be programmed (Conjunction).
	»Assignment 1« ... »Assignment 7«	Assignment
	»Inverting 1« ... »Inverting 7«	Inverting of the state of the assigned signal.

3.3.3.1.3 Device Para / Binary Outputs / BO Slot X2 / BO 3

	»Operating Mode«	Operating Mode
	»t-hold«	To clearly identify the state transition of a binary output relay, the "new state" is being hold, at least for the duration of the hold time.
	»t-Off Delay«	Switch Off Delay
	»Latched«	Defines whether the Relay Output will be latched when it picks up.
	»Acknowledgement«	Acknowledgement Signal - An acknowledgement signal (that acknowledges the corresponding binary output relay) can be assigned to each output relay. The acknowledgement-signal is only effective if the parameter "Latched" is set to active.
	»Inverting«	Inverting of the collective signal (OR-gate/disjunction). In combination with inverted input signals an AND-gate can be programmed (Conjunction).
	»Assignment 1« ... »Assignment 7«	Assignment
	»Inverting 1« ... »Inverting 7«	Inverting of the state of the assigned signal.

3.3.3.1.4 Device Para / Binary Outputs / BO Slot X2 / BO 4

	»Operating Mode«	Operating Mode
	»t-hold«	To clearly identify the state transition of a binary output relay, the "new state" is being hold, at least for the duration of the hold time.
	»t-Off Delay«	Switch Off Delay
	»Latched«	Defines whether the Relay Output will be latched when it picks up.
	»Acknowledgement«	Acknowledgement Signal - An acknowledgement signal (that acknowledges the corresponding binary output relay) can be assigned to each output relay. The acknowledgement-signal is only effective if the parameter "Latched" is set to active.
	»Inverting«	Inverting of the collective signal (OR-gate/disjunction). In combination with inverted input signals an AND-gate can be programmed (Conjunction).
	»Assignment 1« ... »Assignment 7«	Assignment
	»Inverting 1« ... »Inverting 7«	Inverting of the state of the assigned signal.

3.3.3.1.5 Device Para / Binary Outputs / BO Slot X2 / BO 5

	»Operating Mode«	Operating Mode
	»t-hold«	To clearly identify the state transition of a binary output relay, the "new state" is being hold, at least for the duration of the hold time.
	»t-Off Delay«	Switch Off Delay
	»Latched«	Defines whether the Relay Output will be latched when it picks up.
	»Acknowledgement«	Acknowledgement Signal - An acknowledgement signal (that acknowledges the corresponding binary output relay) can be assigned to each output relay. The acknowledgement-signal is only effective if the parameter "Latched" is set to active.
	»Inverting«	Inverting of the collective signal (OR-gate/disjunction). In combination with inverted input signals an AND-gate can be programmed (Conjunction).
	»Assignment 1« ... »Assignment 7«	Assignment
	»Inverting 1« ... »Inverting 7«	Inverting of the state of the assigned signal.

3.3.4 Device Para / LEDs

3.3.4.1 Device Para / LEDs / LED 1

	»Latched«	Defines whether the LED will be latched when it picks up.
	»Ack signal«	Acknowledgement signal for the LED. If latching is set to active the LED can only be acknowledged if those signals that initiated the setting are no longer present.
	»LED active color«	The LED lights up in this color if the state of the OR-assignment of the signals is true.
	»LED inactive color«	The LED lights up in this color if the state of the OR-assignment of the signals is untrue.
	»Assignment 1«	Assignment
	»Assignment 2«	Assignment
	»Assignment 3«	Assignment
	»Assignment 4«	Assignment
	»Assignment 5«	Assignment
	»Inverting 1«	Inverting of the state of the assigned signal.
	»Inverting 2«	Inverting of the state of the assigned signal.
	»Inverting 3«	Inverting of the state of the assigned signal.
	»Inverting 4«	Inverting of the state of the assigned signal.
	»Inverting 5«	Inverting of the state of the assigned signal.

3.3.4.2 Device Para / LEDs / LED 2

	»Latched«	Defines whether the LED will be latched when it picks up.
	»Ack signal«	Acknowledgement signal for the LED. If latching is set to active the LED can only be acknowledged if those signals that initiated the setting are no longer present.
	»LED active color«	The LED lights up in this color if the state of the OR-assignment of the signals is true.
	»LED inactive color«	The LED lights up in this color if the state of the OR-assignment of the signals is untrue.
	»Assignment 1«	Assignment
	»Assignment 2«	Assignment
	»Assignment 3«	Assignment
	»Assignment 4«	Assignment
	»Assignment 5«	Assignment
	»Inverting 1«	Inverting of the state of the assigned signal.
	»Inverting 2«	Inverting of the state of the assigned signal.
	»Inverting 3«	Inverting of the state of the assigned signal.
	»Inverting 4«	Inverting of the state of the assigned signal.
	»Inverting 5«	Inverting of the state of the assigned signal.

3.3.4.3 Device Para / LEDs / LED 3

	»Latched«	Defines whether the LED will be latched when it picks up.
	»Ack signal«	Acknowledgement signal for the LED. If latching is set to active the LED can only be acknowledged if those signals that initiated the setting are no longer present.
	»LED active color«	The LED lights up in this color if the state of the OR-assignment of the signals is true.
	»LED inactive color«	The LED lights up in this color if the state of the OR-assignment of the signals is untrue.
	»Assignment 1«	Assignment
	»Assignment 2«	Assignment
	»Assignment 3«	Assignment
	»Assignment 4«	Assignment
	»Assignment 5«	Assignment
	»Inverting 1«	Inverting of the state of the assigned signal.
	»Inverting 2«	Inverting of the state of the assigned signal.
	»Inverting 3«	Inverting of the state of the assigned signal.
	»Inverting 4«	Inverting of the state of the assigned signal.
	»Inverting 5«	Inverting of the state of the assigned signal.

3.3.4.4 Device Para / LEDs / LED 4

	»Latched«	Defines whether the LED will be latched when it picks up.
	»Ack signal«	Acknowledgement signal for the LED. If latching is set to active the LED can only be acknowledged if those signals that initiated the setting are no longer present.
	»LED active color«	The LED lights up in this color if the state of the OR-assignment of the signals is true.
	»LED inactive color«	The LED lights up in this color if the state of the OR-assignment of the signals is untrue.
	»Assignment 1«	Assignment
	»Assignment 2«	Assignment
	»Assignment 3«	Assignment
	»Assignment 4«	Assignment
	»Assignment 5«	Assignment
	»Inverting 1«	Inverting of the state of the assigned signal.
	»Inverting 2«	Inverting of the state of the assigned signal.
	»Inverting 3«	Inverting of the state of the assigned signal.
	»Inverting 4«	Inverting of the state of the assigned signal.
	»Inverting 5«	Inverting of the state of the assigned signal.

3.3.4.5 Device Para / LEDs / LED 5

	»Latched«	Defines whether the LED will be latched when it picks up.
	»Ack signal«	Acknowledgement signal for the LED. If latching is set to active the LED can only be acknowledged if those signals that initiated the setting are no longer present.
	»LED active color«	The LED lights up in this color if the state of the OR-assignment of the signals is true.
	»LED inactive color«	The LED lights up in this color if the state of the OR-assignment of the signals is untrue.
	»Assignment 1«	Assignment
	»Assignment 2«	Assignment
	»Assignment 3«	Assignment
	»Assignment 4«	Assignment
	»Assignment 5«	Assignment
	»Inverting 1«	Inverting of the state of the assigned signal.
	»Inverting 2«	Inverting of the state of the assigned signal.
	»Inverting 3«	Inverting of the state of the assigned signal.
	»Inverting 4«	Inverting of the state of the assigned signal.
	»Inverting 5«	Inverting of the state of the assigned signal.

3.3.4.6 Device Para / LEDs / LED 6

	»Latched«	Defines whether the LED will be latched when it picks up.
	»Ack signal«	Acknowledgement signal for the LED. If latching is set to active the LED can only be acknowledged if those signals that initiated the setting are no longer present.
	»LED active color«	The LED lights up in this color if the state of the OR-assignment of the signals is true.
	»LED inactive color«	The LED lights up in this color if the state of the OR-assignment of the signals is untrue.
	»Assignment 1«	Assignment
	»Assignment 2«	Assignment
	»Assignment 3«	Assignment
	»Assignment 4«	Assignment
	»Assignment 5«	Assignment
	»Inverting 1«	Inverting of the state of the assigned signal.
	»Inverting 2«	Inverting of the state of the assigned signal.
	»Inverting 3«	Inverting of the state of the assigned signal.
	»Inverting 4«	Inverting of the state of the assigned signal.
	»Inverting 5«	Inverting of the state of the assigned signal.

3.3.4.7 Device Para / LEDs / LED 7

	»Latched«	Defines whether the LED will be latched when it picks up.
	»Ack signal«	Acknowledgement signal for the LED. If latching is set to active the LED can only be acknowledged if those signals that initiated the setting are no longer present.
	»LED active color«	The LED lights up in this color if the state of the OR-assignment of the signals is true.
	»LED inactive color«	The LED lights up in this color if the state of the OR-assignment of the signals is untrue.
	»Assignment 1«	Assignment
	»Assignment 2«	Assignment
	»Assignment 3«	Assignment
	»Assignment 4«	Assignment
	»Assignment 5«	Assignment
	»Inverting 1«	Inverting of the state of the assigned signal.
	»Inverting 2«	Inverting of the state of the assigned signal.
	»Inverting 3«	Inverting of the state of the assigned signal.
	»Inverting 4«	Inverting of the state of the assigned signal.
	»Inverting 5«	Inverting of the state of the assigned signal.

3.3.5 Device Para / Acknowledge

	»Ack via »C« key«	Select which acknowledgeable elements can be reset via pressing the »C« key.
	»Remote Reset«	Enables or disables the option to acknowledge from external/remote via signals (assignments) and SCADA.
	»Ack LED«	All acknowledgeable LEDs will be acknowledged if the state of the assigned signal becomes true.
	»Ack BO«	All acknowledgeable binary output relays will be acknowledged if the state of the assigned signal becomes true.
	»Ack Scada«	Latched SCADA signals are acknowledged if the state of the assigned signal becomes true.

3.3.6 Device Para / Statistics

3.3.6.1 Device Para / Statistics / Min / Max

	»ResFc Max«	Resetting of all Maximum values
	»ResFc Min«	Resetting of all Minimum values

3.3.6.2 Device Para / Statistics / Vavg

	»Start Vavg via:«	Statistics: Start sliding supervision of the average voltage by the set trigger.
	»Start Vavg Fc«	Start of the calculation, if the assigned signal becomes true.
	»ResFc Vavg«	Resetting of the sliding average calculation.
	»Duration Vavg«	Recording time
	»Window Vavg«	Window configuration

3.3.7 Device Para / HMI

	»Contrast«	Contrast
	»Display Off«	The display back light will be turned off when this timer has expired.
	»Menu language«	Selection of the language
	»Display ANSI Device No.«	Display ANSI Device Numbers

3.3.8 Device Para / Security

	»Password«	Changing the password
	»Access Level«	Access Level

3.3.8.1 Device Para / Security / General Settings

	»t-max Edit/Access«	If no other key(s) is pressed at the panel, after expiration of this time, all cached (changed) parameters are canceled. The device access will be locked by falling back into Read-only level Lv0.
	»Conf. Dev. Reset«	If the »C« key is pressed while the device is performing a cold restart a general Reset Dialog appears on the screen. Select which options shall be available with this dialog.

3.3.8.2 Device Para / Security / Communication

	»Smart view via USB«	Activate (allow) or inactivate (disallow) the Smart view access via the USB interface.
	»Smart view via Eth«	Activate (allow) or inactivate (disallow) the Smart view access via the Ethernet interface.
	»Smart view via Modbus«	Activate (allow) or inactivate (disallow) the Smart view access via the Modbus tunnel.

3.3.8.3 Device Para / Security / Syslog

	»Function«	Permanent activation or deactivation of module/stage.
	»IP port number«	IP port number. This is the port on which the Syslog server computer listens and receives log messages. (Since the default, port 514, is a general protocol standard it is recommended to keep this default, unless there are network-related or security-related reasons against it.)
	»IP address, part 1«	IP address (IPv4) of the Syslog server computer, that receives the log messages. IP1.IP2.IP3.IP4
	»IP address, part 2«	IP address (IPv4) of the Syslog server computer, that receives the log messages. IP1.IP2.IP3.IP4
	»IP address, part 3«	IP address (IPv4) of the Syslog server computer, that receives the log messages. IP1.IP2.IP3.IP4
	»IP address, part 4«	IP address (IPv4) of the Syslog server computer, that receives the log messages. IP1.IP2.IP3.IP4

3.3.9 Device Para / Recorders

3.3.9.1 Device Para / Recorders / Disturb rec

	»Start: 1«	Start recording if the assigned signal is true.
	»Start: 2«	Start recording if the assigned signal is true.
	»Start: 3«	Start recording if the assigned signal is true.
	»Start: 4«	Start recording if the assigned signal is true.
	»Start: 5«	Start recording if the assigned signal is true.
	»Start: 6«	Start recording if the assigned signal is true.
	»Start: 7«	Start recording if the assigned signal is true.
	»Start: 8«	Start recording if the assigned signal is true.
	»Auto overwriting«	If there is no more free memory capacity left, the oldest file will be overwritten.
	»Pre-trigger time«	The pre trigger time is set in percent of the »Max file size« value. It corresponds to the part of recording before the onset of the trigger event.
	»Post-trigger time«	The post trigger time is set in percent of the »Max file size« value. It is the remaining time of the »Max file size«, depending on the »Pre-trigger time« setting and the duration of the trigger event, but at maximum the »Post-trigger time« set here.
	»Max file size«	The maximum storage capacity per record, including pre-trigger and post-trigger time. The amount of records depends on the size of each record, on the max. file size (set here), and on the total storage capacity.

3.3.9.2 Device Para / Recorders / Fault rec

	»Record-Mode«	Recorder Mode (Set the behaviour of the recorder)
	»t-meas-delay«	After the Trip, the measurement will be delayed for this time.

3.3.9.3 Device Para / Recorders / Trend rec

	»Resolution«	Resolution (recording frequency)
	»Trend1«	Observed Value1
	»Trend2«	Observed Value2
	»Trend3«	Observed Value3
	»Trend4«	Observed Value4
	»Trend5«	Observed Value5
	»Trend6«	Observed Value6
	»Trend7«	Observed Value7
	»Trend8«	Observed Value8
	»Trend9«	Observed Value9
	»Trend10«	Observed Value10

3.3.10 Device Para / TCP/IP

	»TCP/IP config«	configuration of the TCP/IP protocol

3.3.10.1 Device Para / TCP/IP / Red.Ethernet

	»Supervision PRP«	Supervision PRP
	»superv.Int.PRP«	Interval for supervision messages: PRP
	»Supervision HSR«	Supervision HSR
	»superv.Int.HSR«	Interval for supervision messages: HSR

3.3.10.2 Device Para / TCP/IP / Advanced Settings

	»Keep Alive Time«	Keep Alive Time is the duration between two keep alive transmissions in idle condition
	»Keep Alive Interval«	Keep Alive Interval is the duration between two successive keep alive retransmissions, if the acknowledgement to the previous keepalive transmission was not received.
	»Keep Alive Retry«	Keep alive retry is the number of retransmissions to be carried out before declaring that the remote end is not available.

3.3.11 Device Para / IEC 61850

3.3.11.1 Device Para / IEC 61850 / Communication

	»Function«	Permanent activation or deactivation of module/stage.
	»Deadb integr time«	Deadband integration time.
	»Simulation Mode«	Direct Command to activate the IEC61850 Simulation Mode, so that the “test” flag is set in all GOOSE messages that the device transmits. Moreover, the device reacts in Simulation Mode to only those messages that have this “test” flag set.

3.3.11.2 Device Para / IEC 61850 / Virtual Outputs 1

	»COUTGGIO1.Ind1.stVal« ... »COUTGGIO1.Ind32.stVal«	Virtual Output. This signal can be assigned or visualized via the SCD file to other devices within the IEC61850 substation.

3.3.11.3 Device Para / IEC 61850 / Virtual Outputs 2

	»COUTGGIO2.Ind1.stVal« ... »COUTGGIO2.Ind32.stVal«	Virtual Output. This signal can be assigned or visualized via the SCD file to other devices within the IEC61850 substation.

3.3.12 Device Para / DNP3

3.3.12.1 Device Para / DNP3 / Communication

	»Function«	Permanent activation or deactivation of module/stage.
	»IP Port Number«	IP Port Number. In general it is recommended to keep the default value. If this is not possible then select a number out of the private range 49152-52151 or 52164-65535 that is not yet in use within your network.
	»Baud rate«	Baud rate for communication

	»Frame Layout«	Frame Layout
	»Optical rest position«	Optical rest position
	»Slave Id«	SlaveId defines the DNP3 address of this device (Outstation)
	»Master Id«	MasterId defines the DNP3 address of master (SCADA)
	»SelfAddress«	Support of self (automatic) addresses
	»DataLink confirm«	Enables or disables the data layer confirmation (ack).
	»t-DataLink confirm«	Data layer confirmation timeout
	»DataLink num retries«	Number of repetition of data link packet sending after failing
	»Direction Bit«	Enables Direction Bit functionality. The Direction Bit is 0 for SlaveStation and 1 for MasterStation
	»Max Frame Size«	This value is used to limit the net Frame Size
	»Test Link Period«	This value specifies the time period when to send a Test Link-Frame
	»AppLink confirm«	Determines if the device will request that the Application Layer response be confirmed or not
	»t-AppLink confirm«	Application layer response timeout
	»AppLink num retries«	The number of times the device will retransmit an Application Layer fragment
	»Unsol Reporting«	Enables unsolicited reporting. This is available only for DNP3 TCP connections, and for DNP3 RTU in case of a peer-to-peer connection.
	»Unsol Reporting Timeout«	Set the amount of time that the outstation will wait for an Application Layer confirmation back from the master indicating that the master received the unsolicited response message.
	»Unsol Reporting Retry«	Set the number of retries that an outstation transmits in each unsolicited response series if it does not receive confirmation back from the master.
	»TestSeqNo«	Test if sequence number of request is incremented. If it is not correctly incremented the request will be ignored. It is recommended to have it inactive but some older DNP implementations need it activated.
	»TestSBO«	It enables a stricter comparing of SBO and operate command. For older DNP versions it is recommanded to deactivated it.
	»Timeout SBO«	DNP Outputs can be controlled in a two stage procedure (SBO: Select Before Operate). These outputs are to be selected first by a Select command. After this the bit is reserved for this Operate request. This setting defines the timer for this reservation: After the timer has elapsed the bit is released.
	»ColdRestart«	Enables support for Cold Restart function.
	»Deadb integr time«	Deadband integration time.

3.3.12.2 Device Para / DNP3 / Point map

3.3.12.2.1 Device Para / DNP3 / Point map / Binary Inputs

	»BinaryInput 0« ...	Virtual Digital Input (DNP). This corresponds to a virtual binary output of the protective device.

	»BinaryInput 63«	

3.3.12.2.2 Device Para / DNP3 / Point map / Double Bit Inputs

	»DoubleBitInput 0«	Double Bit Digital Input (DNP). This corresponds to a double bit binary output of the protective device.
	»DoubleBitInput 1«	Double Bit Digital Input (DNP). This corresponds to a double bit binary output of the protective device.
	»DoubleBitInput 2«	Double Bit Digital Input (DNP). This corresponds to a double bit binary output of the protective device.
	»DoubleBitInput 3«	Double Bit Digital Input (DNP). This corresponds to a double bit binary output of the protective device.
	»DoubleBitInput 4«	Double Bit Digital Input (DNP). This corresponds to a double bit binary output of the protective device.
	»DoubleBitInput 5«	Double Bit Digital Input (DNP). This corresponds to a double bit binary output of the protective device.

3.3.12.2.3 Device Para / DNP3 / Point map / BinaryCounter

	»BinaryCounter 0«	Counter can be used to report counter values to the DNP master.
	»BinaryCounter 1«	Counter can be used to report counter values to the DNP master.
	»BinaryCounter 2«	Counter can be used to report counter values to the DNP master.
	»BinaryCounter 3«	Counter can be used to report counter values to the DNP master.
	»BinaryCounter 4«	Counter can be used to report counter values to the DNP master.
	»BinaryCounter 5«	Counter can be used to report counter values to the DNP master.
	»BinaryCounter 6«	Counter can be used to report counter values to the DNP master.
	»BinaryCounter 7«	Counter can be used to report counter values to the DNP master.

3.3.12.2.4 Device Para / DNP3 / Point map / Analog Input

	»Analog value 0« ... »Analog value 31«	Analog value can be used to report values to the master (DNP)
	»Scale Factor 0« ... »Scale Factor 31«	The scale factor is used to convert the measured value in an integer format
	»Dead Band 0« ...	If a change of measured value is greater than the deadband value it will be reported to the master.

	»Dead Band 31«	

3.3.13 Device Para / Modbus

3.3.13.1 Device Para / Modbus / Communication

3.3.13.1.1 Device Para / Modbus / Communication / General Settings

	»t-call«	If there is no request telegram sent from Scada to the device after expiry of this time - the device concludes a communication failure within the Scada system.
	»Scada CmdBlo«	Activating (allowing)/ Deactivating (disallowing) the blocking of the Scada Commands
	»Disable Latching«	Disable Latching: If this parameter is active (true), none of the Modbus states will be latched. That means that trip signals wont be latched by Modbus.
	»AllowGap«	If this parameter is active (True), the user can request a set of modbus register without getting an exception, because of invalid address in the requested array. The invalid addresses have a special value 0xFAFA, but the user is responsible for ignoring invalid addresses. Attention: This special value can be valid, if address is valid.
	»Optical rest position«	Optical rest position

3.3.13.1.2 Device Para / Modbus / Communication / TCP

	»Unit ID«	The Unit Identifier is used for routing. This parameter is to be set, if a Modbus RTU and a Modbus TCP network should be coupled.
	»TCP Port Config«	TCP Port Configuration. This parameter needs to be set to “Private” only if another TCP Port than the default one shall be used.
	»Port«	IP Port Number. In general it is recommended to keep the default value. if this is not possible then select a number out of the private range 49152-52151 or 52164-65535 that is not yet in use within your network.

3.3.13.1.3 Device Para / Modbus / Communication / RTU

	»Slave ID«	Device address (Slave ID) within the bus system. Each device address has to be unique within a bus system.
	»t-timeout«	Maximum time that is available to the device for sending an answer to the SCADA system. If the device detects that this time has elapsed (i.e. it failed to send its answer within this time) then it cancels the answer. The time set here must not be longer than the corresponding timeout set for the SCADA system.
	»Baud rate«	Baud rate
	»Physical Settings«	Digit 1: Number of bits. Digit 2: E=even parity, O=odd parity, N=no parity. Digit 3: Number of stop bits. More information on the parity: It is possible that the last data bit is followed by a parity bit which is used for recognition of communication errors. The parity bit ensures that with even parity ("EVEN") always an even number of bits with valence "1" or with odd parity ("ODD") an odd number of "1" valence bits are transmitted. But it is also possible to transmit no parity bits (here the setting is "Parity = None"). More information on the stop-bits: The end of a data byte is terminated by the stop-bits.

3.3.13.2 Device Para / Modbus / Configb Registers

3.3.13.2.1 Device Para / Modbus / Configb Registers / States

	»Config Bin Inp1« ... »Config Bin Inp32«	Virtual Digital Input. This corresponds to a virtual binary output of the protective device.
	»Latched Config Bin Inp1« ... »Latched Config Bin Inp32«	Latched Configurable Binary Input

3.3.13.2.2 Device Para / Modbus / Configb Registers / Measured Values

	»Mapped Meas 1«	Mapped Measured Values. They can be used to provide measured values to the Modbus Master.
	»Mapped Meas 2«	Mapped Measured Values. They can be used to provide measured values to the Modbus Master.
	»Mapped Meas 3«	Mapped Measured Values. They can be used to provide measured values to the Modbus Master.
	»Mapped Meas 4«	Mapped Measured Values. They can be used to provide measured values to the Modbus Master.
	»Mapped Meas 5«	Mapped Measured Values. They can be used to provide measured values to the Modbus Master.
	»Mapped Meas 6«	Mapped Measured Values. They can be used to provide measured values to the Modbus Master.
	»Mapped Meas 7«	Mapped Measured Values. They can be used to provide measured values to the Modbus Master.
	»Mapped Meas 8«	Mapped Measured Values. They can be used to provide measured values to the Modbus Master.
	»Mapped Meas 9«	Mapped Measured Values. They can be used to provide measured values to the Modbus Master.
	»Mapped Meas 10«	Mapped Measured Values. They can be used to provide measured values to the Modbus Master.
	»Mapped Meas 11«	Mapped Measured Values. They can be used to provide measured values to the Modbus Master.
	»Mapped Meas 12«	Mapped Measured Values. They can be used to provide measured values to the Modbus Master.
	»Mapped Meas 13«	Mapped Measured Values. They can be used to provide measured values to the Modbus Master.
	»Mapped Meas 14«	Mapped Measured Values. They can be used to provide measured values to the Modbus Master.
	»Mapped Meas 15«	Mapped Measured Values. They can be used to provide measured values to the Modbus Master.
	»Mapped Meas 16«	Mapped Measured Values. They can be used to provide measured values to the Modbus Master.

3.3.13.3 Device Para / Modbus / Config. Data Obj.

	»Type of SCADA mapping«	This setting decides whether the communication protocol shall use the default mapping of data objects, or some user-defined mapping that has been loaded from a *.HptSMap file.
	»Config info«	Configuration comment (entered by the user during SCADA configuration)
	»Config version«	Version of the user-defined SCADA configuration
	»Config status«	Status of the user-defined SCADA configuration. Possible values: - New SCADA configuration is being loaded, but not active yet. - The SCADA configuration is active. - The user-defined SCADA configuration is not available (e.g. has not been loaded into the device). - Unexpected error. Please contact our service-team.

3.3.14 Device Para / IEC103

3.3.14.1 Device Para / IEC103 / General Settings

	»Function«	Activation or deactivation of the IEC103 communication.
	»Slave ID«	Device address (Slave ID) within the bus system. Each device address has to be unique within a bus system.
	»Baud rate«	Baud rate
	»Physical Settings«	Digit 1: Number of bits. Digit 2: E=even parity, O=odd parity, N=no parity. Digit 3: Number of stop bits. More information on the parity: It is possible that the last data bit is followed by a parity bit which is used for recognition of communication errors. The parity bit ensures that with even parity ("EVEN") always an even number of bits with valence "1" or with odd parity ("ODD") an odd number of "1" valence bits are transmitted. But it is also possible to transmit no parity bits (here the setting is "Parity = None"). More information on the stop-bits: The end of a data byte is terminated by the stop-bits.
	»Timezone«	Selection whether the timestamps in IEC103 messages shall be given as UTC or local time. (“Local time” always includes the actual daylight saving settings.)
	»Transfer Disturb Rec«	Activates the transmission of disturbance records
	»Energy Pulse Rate«	The energy values are always transmitted as counter values (i.e. as integer numbers). This setting defines the unit: If “1” is set then each counter increment is 1 kWh, if “2” is set then each counter increment is 2 kWh,etc. The setting “0” has the effect that no energy values are transmitted.
	»t-call«	If there is no request telegram sent from Scada to the device after expiry of this time - the device concludes a communication failure within the Scada system.
	»DFC-Compat.«	This setting is only required for certain substation implementations. If there should be communication problems related to the Command Response Queue this setting switches the device over to a different behavior.

3.3.14.2 Device Para / IEC103 / Config. Data Obj.

	»Type of SCADA mapping«	This setting decides whether the communication protocol shall use the default mapping of data objects, or some user-defined mapping that has been loaded from a *.HptSMap file.
	»Config info«	Configuration comment (entered by the user during SCADA configuration)
	»Config version«	Version of the user-defined SCADA configuration
	»Config status«	Status of the user-defined SCADA configuration. Possible values: - Changing: New SCADA configuration is being loaded, but not active yet. - OK: The SCADA configuration is active. - Config. not avail.: The user-defined SCADA configuration is not available (e.g. has not been loaded into the device). - Error: Unexpected error. Please contact our service-team.

3.3.15 Device Para / IEC104

3.3.15.1 Device Para / IEC104 / General Settings

	»Function«	Activation or deactivation of the IEC104 communication.
	»TCP Port Config«	TCP Port Configuration. This parameter needs to be set to “Private” only if another TCP Port than the default one shall be used.
	»Port«	IP Port Number. In general it is recommended to keep the default value. if this is not possible then select a number out of the private range 49152-52151 or 52164-65535 that is not yet in use within your network.
	»Common address«	Common Address of the ASDU
	»Timezone«	Selection whether the timestamps in the transmitted communication telegrams shall be given as UTC or local time. (“Local time” always includes the actual daylight saving settings.)
	»Deadb integr time«	Deadband integration time.
	»Timeout SBE«	The communication outputs can be controlled in a two-stage procedure (SBE: Select Before Execute). These outputs have to be selected first by a Select command. After this the bit is reserved for this Execute request. This setting defines the timer for this reservation: After the timer has elapsed the bit is released.

3.3.15.2 Device Para / IEC104 / Advanced

	»Timeout t0«	Timeout of connection establishment
	»Timeout t1«	Timeout of send or test APDUs
	»Timeout t2«	Timeout for acknowledges in case of no data messages
	»Timeout t3«	Timeout for sending test frames in case of a long idle state
	»Param k«	Protocol parameter k
	»Param w«	Protocol parameter w
	»Length of address«	Number of bytes of the Common Address of the ASDU
	»Length of CoT«	Number of bytes of the Cause of Transmission
	»Length of Inf Obj addr«	Number of bytes of the address of the Information Object
	»Update time«	This setting specifies the time after which measurement values are refreshed. If cyclic transmission is selected new values are reported after this time has elapsed.
	»Transmit Int. State«	If this parameter is set to “active” (default) then the intermediate position of a switchgear, too, is transmitted. This needs to be changed to “inactive” only in the rare case that the substation communication does not support the reporting of intermediate positions.
	»Trans. Cmd. State«	_ If false it suppress change events for command states (Same address as cmd)

3.3.15.3 Device Para / IEC104 / Config. Data Obj.

	»Type of SCADA mapping«	This setting decides whether the communication protocol shall use the default mapping of data objects, or some user-defined mapping that has been loaded from a *.HptSMap file.
	»Config info«	Configuration comment (entered by the user during SCADA configuration)
	»Config version«	Version of the user-defined SCADA configuration
	»Config status«	Status of the user-defined SCADA configuration. Possible values: - Changing: New SCADA configuration is being loaded, but not active yet. - OK: The SCADA configuration is active. - Config. not avail.: The user-defined SCADA configuration is not available (e.g. has not been loaded into the device). - Error: Unexpected error. Please contact our service-team.

3.3.16 Device Para / Profibus

3.3.16.1 Device Para / Profibus / Bus parameters

	»Slave ID«	Device address (Slave ID) within the bus system. Each device address has to be unique within a bus system.
	»Little Endian«	If this setting is “active” all numbers are transmitted with the byte order Little Endian, otherwise the byte order Big Endian is used. (If all numbers received by your SCADA system should be completely wrong, changing this setting might help.)

3.3.16.2 Device Para / Profibus / ConfigBinInp 1-16

	»ConfigBinInp 1« ... »ConfigBinInp 16«	Virtual Digital Input. This corresponds to a virtual binary output of the protective device.
	»Latched 1« ... »Latched 16«	Defines whether the Input is latched.

3.3.16.3 Device Para / Profibus / ConfigBinInp 17-32

	»ConfigBinInp 17« ... »ConfigBinInp 32«	Virtual Digital Input. This corresponds to a virtual binary output of the protective device.
	»Latched 17« ... »Latched 32«	Defines whether the Input is latched.

3.3.16.4 Device Para / Profibus / Config. Data Obj.

	»Type of SCADA mapping«	This setting decides whether the communication protocol shall use the default mapping of data objects, or some user-defined mapping that has been loaded from a *.HptSMap file.
	»Config info«	Configuration comment (entered by the user during SCADA configuration)
	»Config version«	Version of the user-defined SCADA configuration
	»Config status«	Status of the user-defined SCADA configuration. Possible values:

3.3.17 Device Para / Time

	»Date and Time«	(Re-)setting Date and Time

3.3.17.1 Device Para / Time / Timezone

	»Time Zones«	Time Zones
	»DST offset«	Difference to wintertime
	»DST manual«	Manual setting of the Daylight Saving Time
	»Summertime«	Daylight Saving Time
	»Summertime m«	Month of clock change summertime
	»Summertime d«	Day of clock change summertime
	»Summertime w«	Place of selected day in month (for clock change summertime)
	»Summertime h«	Hour of clock change summertime
	»Summertime min«	Minute of clock change summertime
	»Wintertime m«	Month of clock change wintertime
	»Wintertime d«	Day of clock change wintertime
	»Wintertime w«	Place of selected day in month (for clock change wintertime)
	»Wintertime h«	Hour of clock change wintertime
	»Wintertime min«	Minute of clock change wintertime

3.3.17.2 Device Para / Time / TimeSync

3.3.17.2.1 Device Para / Time / TimeSync / TimeSync

	»TimeSync«	Time synchronisation

3.3.17.2.2 Device Para / Time / TimeSync / PTP

	»Net.Trans.Prot.«	PTP Network Transport Protocol (IEEE 802.3 or UDP IPv4)
	»Domain«	Domain number. Im Fall Power Profile IEEE C37.238 empfohlener Wert ist 254 und für IEC61850-9-3 ist 254.
	»PathDelay Intv.«	PathDelay Intv.
	»PeerPathDelay Intv.«	PeerPathDelay Intv.
	»Vlan act.«	Vlan activation
	»Vlan ID«	Vlan ID
	»Vlan prio«	PTP VLAN priority.

3.3.17.2.3 Device Para / Time / TimeSync / IRIG-B

	»Function«	Permanent activation or deactivation of module/stage.
	»IRIG-B00X«	Determination of the Type: IRIG-B00X. IRIG-B types differ in types of included “Coded Expressions” (year, control-functions, straight-binary-seconds).

3.3.17.2.4 Device Para / Time / TimeSync / SNTP

	»Server1«	Server 1
	»IP Byte1«	IP1.IP2.IP3.IP4
	»IP Byte2«	IP1.IP2.IP3.IP4
	»IP Byte3«	IP1.IP2.IP3.IP4
	»IP Byte4«	IP1.IP2.IP3.IP4
	»Server2«	Server 2
	»IP Byte1«	IP1.IP2.IP3.IP4
	»IP Byte2«	IP1.IP2.IP3.IP4
	»IP Byte3«	IP1.IP2.IP3.IP4
	»IP Byte4«	IP1.IP2.IP3.IP4

3.3.18 Device Para / Version

	»DM version«	Version of the device model
	»SW version«	Version of the device firmware
	»Build«	Build Number
	»CAT No«	»CAT No.«, Order Code as printed on the nameplate of the device.
	»REV.«	Revision (as printed on the nameplate of the device).
	»S/N«	The serial number of the device.
	»Bootloader Build«	Build number of the bootloader

3.4 Field Para

3.4.1 Field Para / General Settings

	»Phase Sequence«	Phase Sequence
	»f«	Nominal frequency
	»Setting Lock«	No parameters can be changed as long as this input is true. The parameter settings are locked.
	»Setting Lock Bypass«	Short-period unlock of the Setting Lock

3.4.2 Field Para / VT

	»VT pri«	Nominal voltage of the Voltage Transformers at the primary side. Note that always the phase-to-phase voltage must be entered here.
	»VT sec«	Nominal voltage of the Voltage Transformers at the secondary side. Note that always the phase-to-phase voltage must be entered here.
	»VT con«	This parameter has to be set in order to ensure the correct assignment of the voltage measurement channels in the device.
	»EVT pri«	Primary nominal voltage of the e-n winding of the voltage transformers, which is only taken into account in the direct measurement of the residual voltage (GVT con=measured/broken delta).
	»EVT sec«	Secondary nominal voltage of the e-n winding of the voltage transformers, which is only taken into account in the direct measurement of the residual voltage.
	»V Sync«	The fourth measuring input of the voltage measuring card measures the voltage that is to be synchronized.

3.4.3 Field Para / Frequency

	»V Block f«	Threshold for the release of the frequency stages: Frequency-based protection functions are blocked if the voltage drops below this setting. This is necessary to avoid an undesired response of the frequency-based protection functions in case of a voltage disturbance caused by a fault. For example, faults with an arc flash generate a high proportion of harmonics in the voltage. Such disturbances will interfere with accurate frequency detection.
	»delta phi - Mode«	The delta phi element (vector surge) trips, if the permissable voltage angle shift (delta phi) of the three measured voltages (phase-ground or phase-phase) in: one phase, two phases or within all phases is exceeded.
	»Stab. window f«	Stabilizing window, for stabilizing the frequency values against momentary fluctuations. The setting value is in cycles at the rated frequency. Set to "0" for VDE AR-N 4110:2023-9 / 4120:2018-11.
	»Stab. window f for df/dt«	Stabilizing window, for stabilizing the frequency values that are used as input for df/dt calculation against momentary fluctuations. The setting value is in cycles at the rated frequency.
	»Window df/dt«	Window for the determination of df/dt (ROCOF). The setting value is in cycles at the rated frequency.
	»Stab. window df/dt«	Stabilizing window, for stabilizing the df/dt (ROCOF) values against momentary fluctuations. The setting value is in cycles at the rated frequency.

3.5 Protection Para

3.5.1 Protection Para / Global Prot Para

3.5.1.1 Protection Para / Global Prot Para / Prot

	»Function«	Permanent activation or deactivation of module/stage.
	»ExBlo Fc«	Activate (allow) the external blocking of the global protection functionality of the device.
	»ExBlo1«	If external blocking of this module is activated (allowed), the global protection functionality of the device will be blocked if the state of the assigned signal becomes true.
	»ExBlo2«	If external blocking of this module is activated (allowed), the global protection functionality of the device will be blocked if the state of the assigned signal becomes true.
	»Blo TripCmd«	Permanent blocking of the Trip Command of the entire Protection.
	»ExBlo TripCmd Fc«	Activate (allow) the external blocking of the trip command of the entire device.
	»ExBlo TripCmd«	If external blocking of the tripping command is activated (allowed), the tripping command of the entire device will be blocked if the state of the assigned signal becomes true.

3.5.1.2 Protection Para / Global Prot Para / Intercon-Prot

3.5.1.2.1 Protection Para / Global Prot Para / Intercon-Prot / Mains Decouplg

3.5.1.2.1.1 Protection Para / Global Prot Para / Intercon-Prot / Mains Decouplg / df/dt

	»ExBlo1«	External blocking of the module, if blocking is activated (allowed) within a parameter set and if the state of the assigned signal is true.
	»ExBlo2«	External blocking of the module, if blocking is activated (allowed) within a parameter set and if the state of the assigned signal is true.
	»ExBlo TripCmd«	External blocking of the Trip Command of the module/the stage, if blocking is activated (allowed) within a parameter set and if the state of the assigned signal is true.

3.5.1.2.1.2 Protection Para / Global Prot Para / Intercon-Prot / Mains Decouplg / delta phi

	»ExBlo1«	External blocking of the module, if blocking is activated (allowed) within a parameter set and if the state of the assigned signal is true.
	»ExBlo2«	External blocking of the module, if blocking is activated (allowed) within a parameter set and if the state of the assigned signal is true.
	»ExBlo TripCmd«	External blocking of the Trip Command of the module/the stage, if blocking is activated (allowed) within a parameter set and if the state of the assigned signal is true.

3.5.1.2.1.3 Protection Para / Global Prot Para / Intercon-Prot / Mains Decouplg / Intertripping

	»ExBlo1«	External blocking of the module, if blocking is activated (allowed) within a parameter set and if the state of the assigned signal is true.
	»ExBlo2«	External blocking of the module, if blocking is activated (allowed) within a parameter set and if the state of the assigned signal is true.
	»ExBlo TripCmd«	External blocking of the Trip Command of the module/the stage, if blocking is activated (allowed) within a parameter set and if the state of the assigned signal is true.
	»Alarm«	Assignment for External Alarm
	»Trip«	External trip of the CB if the state of the assigned signal is true.

3.5.1.2.2 Protection Para / Global Prot Para / Intercon-Prot / LVRT[1]

	»ExBlo1«	External blocking of the module, if blocking is activated (allowed) within a parameter set and if the state of the assigned signal is true.
	»ExBlo2«	External blocking of the module, if blocking is activated (allowed) within a parameter set and if the state of the assigned signal is true.
	»ExBlo TripCmd«	External blocking of the Trip Command of the module/the stage, if blocking is activated (allowed) within a parameter set and if the state of the assigned signal is true.

3.5.1.2.3 Protection Para / Global Prot Para / Intercon-Prot / LVRT[2]

	»ExBlo1«	External blocking of the module, if blocking is activated (allowed) within a parameter set and if the state of the assigned signal is true.
	»ExBlo2«	External blocking of the module, if blocking is activated (allowed) within a parameter set and if the state of the assigned signal is true.
	»ExBlo TripCmd«	External blocking of the Trip Command of the module/the stage, if blocking is activated (allowed) within a parameter set and if the state of the assigned signal is true.

3.5.1.2.4 Protection Para / Global Prot Para / Intercon-Prot / ReCon[1]

3.5.1.2.4.1 Protection Para / Global Prot Para / Intercon-Prot / ReCon[1] / General Settings

	»ExBlo1«	External blocking of the module, if blocking is activated (allowed) within a parameter set and if the state of the assigned signal is true.
	»ExBlo2«	External blocking of the module, if blocking is activated (allowed) within a parameter set and if the state of the assigned signal is true.
	»V Ext Release PCC«	Release Signal by the Point of Common Coupling. The line-to-line voltage is greater than 95% of VN.
	»PCC Fuse Fail VT«	Blocking if the fuse of a voltage transformer has tripped at the PCC.
	»reconnected«	This signal indicates the state "reconnected" (mains parallel).

3.5.1.2.4.2 Protection Para / Global Prot Para / Intercon-Prot / ReCon[1] / Decoupling

	»Decoupling1«	Decoupling function, that triggers the reconnection.
	»Decoupling2«	Decoupling function, that triggers the reconnection.
	»Decoupling3«	Decoupling function, that triggers the reconnection.
	»Decoupling4«	Decoupling function, that triggers the reconnection.
	»Decoupling5«	Decoupling function, that triggers the reconnection.
	»Decoupling6«	Decoupling function, that triggers the reconnection.

3.5.1.2.5 Protection Para / Global Prot Para / Intercon-Prot / ReCon[2]

3.5.1.2.5.1 Protection Para / Global Prot Para / Intercon-Prot / ReCon[2] / General Settings

	»ExBlo1«	External blocking of the module, if blocking is activated (allowed) within a parameter set and if the state of the assigned signal is true.
	»ExBlo2«	External blocking of the module, if blocking is activated (allowed) within a parameter set and if the state of the assigned signal is true.
	»V Ext Release PCC«	Release Signal by the Point of Common Coupling. The line-to-line voltage is greater than 95% of VN.
	»PCC Fuse Fail VT«	Blocking if the fuse of a voltage transformer has tripped at the PCC.
	»reconnected«	This signal indicates the state "reconnected" (mains parallel).

3.5.1.2.5.2 Protection Para / Global Prot Para / Intercon-Prot / ReCon[2] / Decoupling

	»Decoupling1«	Decoupling function, that triggers the reconnection.
	»Decoupling2«	Decoupling function, that triggers the reconnection.
	»Decoupling3«	Decoupling function, that triggers the reconnection.
	»Decoupling4«	Decoupling function, that triggers the reconnection.
	»Decoupling5«	Decoupling function, that triggers the reconnection.
	»Decoupling6«	Decoupling function, that triggers the reconnection.

3.5.1.2.6 Protection Para / Global Prot Para / Intercon-Prot / Sync

	»ExBlo1«	External blocking of the module, if blocking is activated (allowed) within a parameter set and if the state of the assigned signal is true.
	»ExBlo2«	External blocking of the module, if blocking is activated (allowed) within a parameter set and if the state of the assigned signal is true.
	»Bypass«	The Synchrocheck will be bypassed if the state of the assigned signal (logic input) becomes true.
	»CB Pos Detect«	Criterion by which the Circuit Breaker Switch Position is to be detected.
	»CBCloseInitiate«	Breaker Close Initiate with synchronism check from any control sources (e.g. HMI / SCADA). If the state of the assigned signal becomes true, a Breaker Close will be initiated (Trigger Source).
	»Transformer-Mode«	Activate transformer mode to enable phase and angle corrections for this function.
	»V Line / V Bus«	Ratio of the voltage amplitudes between the line and bus side when using transformer mode.
	»Angle Correction«	Correction angle resulting from the difference in angle between the line and bus side when using transformer mode.

3.5.1.3 Protection Para / Global Prot Para / V-Prot

3.5.1.3.1 Protection Para / Global Prot Para / V-Prot / V[1]

	»ExBlo1«	External blocking of the module, if blocking is activated (allowed) within a parameter set and if the state of the assigned signal is true.
	»ExBlo2«	External blocking of the module, if blocking is activated (allowed) within a parameter set and if the state of the assigned signal is true.
	»ExBlo TripCmd«	External blocking of the Trip Command of the module/the stage, if blocking is activated (allowed) within a parameter set and if the state of the assigned signal is true.

3.5.1.3.2 Protection Para / Global Prot Para / V-Prot / V[2]

	»ExBlo1«	External blocking of the module, if blocking is activated (allowed) within a parameter set and if the state of the assigned signal is true.
	»ExBlo2«	External blocking of the module, if blocking is activated (allowed) within a parameter set and if the state of the assigned signal is true.
	»ExBlo TripCmd«	External blocking of the Trip Command of the module/the stage, if blocking is activated (allowed) within a parameter set and if the state of the assigned signal is true.

3.5.1.3.3 Protection Para / Global Prot Para / V-Prot / V[3]

	»ExBlo1«	External blocking of the module, if blocking is activated (allowed) within a parameter set and if the state of the assigned signal is true.
	»ExBlo2«	External blocking of the module, if blocking is activated (allowed) within a parameter set and if the state of the assigned signal is true.
	»ExBlo TripCmd«	External blocking of the Trip Command of the module/the stage, if blocking is activated (allowed) within a parameter set and if the state of the assigned signal is true.

3.5.1.3.4 Protection Para / Global Prot Para / V-Prot / V[4]

	»ExBlo1«	External blocking of the module, if blocking is activated (allowed) within a parameter set and if the state of the assigned signal is true.
	»ExBlo2«	External blocking of the module, if blocking is activated (allowed) within a parameter set and if the state of the assigned signal is true.
	»ExBlo TripCmd«	External blocking of the Trip Command of the module/the stage, if blocking is activated (allowed) within a parameter set and if the state of the assigned signal is true.

3.5.1.3.5 Protection Para / Global Prot Para / V-Prot / V[5]

	»ExBlo1«	External blocking of the module, if blocking is activated (allowed) within a parameter set and if the state of the assigned signal is true.
	»ExBlo2«	External blocking of the module, if blocking is activated (allowed) within a parameter set and if the state of the assigned signal is true.
	»ExBlo TripCmd«	External blocking of the Trip Command of the module/the stage, if blocking is activated (allowed) within a parameter set and if the state of the assigned signal is true.

3.5.1.3.6 Protection Para / Global Prot Para / V-Prot / V[6]

	»ExBlo1«	External blocking of the module, if blocking is activated (allowed) within a parameter set and if the state of the assigned signal is true.
	»ExBlo2«	External blocking of the module, if blocking is activated (allowed) within a parameter set and if the state of the assigned signal is true.
	»ExBlo TripCmd«	External blocking of the Trip Command of the module/the stage, if blocking is activated (allowed) within a parameter set and if the state of the assigned signal is true.

3.5.1.3.7 Protection Para / Global Prot Para / V-Prot / VG[1]

	»ExBlo1«	External blocking of the module, if blocking is activated (allowed) within a parameter set and if the state of the assigned signal is true.
	»ExBlo2«	External blocking of the module, if blocking is activated (allowed) within a parameter set and if the state of the assigned signal is true.
	»ExBlo TripCmd«	External blocking of the Trip Command of the module/the stage, if blocking is activated (allowed) within a parameter set and if the state of the assigned signal is true.

3.5.1.3.8 Protection Para / Global Prot Para / V-Prot / VG[2]

	»ExBlo1«	External blocking of the module, if blocking is activated (allowed) within a parameter set and if the state of the assigned signal is true.
	»ExBlo2«	External blocking of the module, if blocking is activated (allowed) within a parameter set and if the state of the assigned signal is true.
	»ExBlo TripCmd«	External blocking of the Trip Command of the module/the stage, if blocking is activated (allowed) within a parameter set and if the state of the assigned signal is true.

3.5.1.3.9 Protection Para / Global Prot Para / V-Prot / V012[1]

	»ExBlo1«	External blocking of the module, if blocking is activated (allowed) within a parameter set and if the state of the assigned signal is true.1
	»ExBlo2«	External blocking of the module, if blocking is activated (allowed) within a parameter set and if the state of the assigned signal is true.2
	»ExBlo TripCmd«	External blocking of the Trip Command of the module/the stage, if blocking is activated (allowed) within a parameter set and if the state of the assigned signal is true.

3.5.1.3.10 Protection Para / Global Prot Para / V-Prot / V012[2]

	»ExBlo1«	External blocking of the module, if blocking is activated (allowed) within a parameter set and if the state of the assigned signal is true.1
	»ExBlo2«	External blocking of the module, if blocking is activated (allowed) within a parameter set and if the state of the assigned signal is true.2
	»ExBlo TripCmd«	External blocking of the Trip Command of the module/the stage, if blocking is activated (allowed) within a parameter set and if the state of the assigned signal is true.

3.5.1.3.11 Protection Para / Global Prot Para / V-Prot / V012[3]

	»ExBlo1«	External blocking of the module, if blocking is activated (allowed) within a parameter set and if the state of the assigned signal is true.1
	»ExBlo2«	External blocking of the module, if blocking is activated (allowed) within a parameter set and if the state of the assigned signal is true.2
	»ExBlo TripCmd«	External blocking of the Trip Command of the module/the stage, if blocking is activated (allowed) within a parameter set and if the state of the assigned signal is true.

3.5.1.3.12 Protection Para / Global Prot Para / V-Prot / V012[4]

	»ExBlo1«	External blocking of the module, if blocking is activated (allowed) within a parameter set and if the state of the assigned signal is true.1
	»ExBlo2«	External blocking of the module, if blocking is activated (allowed) within a parameter set and if the state of the assigned signal is true.2
	»ExBlo TripCmd«	External blocking of the Trip Command of the module/the stage, if blocking is activated (allowed) within a parameter set and if the state of the assigned signal is true.

3.5.1.3.13 Protection Para / Global Prot Para / V-Prot / V012[5]

	»ExBlo1«	External blocking of the module, if blocking is activated (allowed) within a parameter set and if the state of the assigned signal is true.1
	»ExBlo2«	External blocking of the module, if blocking is activated (allowed) within a parameter set and if the state of the assigned signal is true.2
	»ExBlo TripCmd«	External blocking of the Trip Command of the module/the stage, if blocking is activated (allowed) within a parameter set and if the state of the assigned signal is true.

3.5.1.3.14 Protection Para / Global Prot Para / V-Prot / V012[6]

	»ExBlo1«	External blocking of the module, if blocking is activated (allowed) within a parameter set and if the state of the assigned signal is true.1
	»ExBlo2«	External blocking of the module, if blocking is activated (allowed) within a parameter set and if the state of the assigned signal is true.2
	»ExBlo TripCmd«	External blocking of the Trip Command of the module/the stage, if blocking is activated (allowed) within a parameter set and if the state of the assigned signal is true.

3.5.1.4 Protection Para / Global Prot Para / f-Prot

3.5.1.4.1 Protection Para / Global Prot Para / f-Prot / f[1]

	»ExBlo1«	External blocking of the module, if blocking is activated (allowed) within a parameter set and if the state of the assigned signal is true.
	»ExBlo2«	External blocking of the module, if blocking is activated (allowed) within a parameter set and if the state of the assigned signal is true.
	»ExBlo TripCmd«	External blocking of the Trip Command of the module/the stage, if blocking is activated (allowed) within a parameter set and if the state of the assigned signal is true.

3.5.1.4.2 Protection Para / Global Prot Para / f-Prot / f[2]

	»ExBlo1«	External blocking of the module, if blocking is activated (allowed) within a parameter set and if the state of the assigned signal is true.
	»ExBlo2«	External blocking of the module, if blocking is activated (allowed) within a parameter set and if the state of the assigned signal is true.
	»ExBlo TripCmd«	External blocking of the Trip Command of the module/the stage, if blocking is activated (allowed) within a parameter set and if the state of the assigned signal is true.

3.5.1.4.3 Protection Para / Global Prot Para / f-Prot / f[3]

	»ExBlo1«	External blocking of the module, if blocking is activated (allowed) within a parameter set and if the state of the assigned signal is true.
	»ExBlo2«	External blocking of the module, if blocking is activated (allowed) within a parameter set and if the state of the assigned signal is true.
	»ExBlo TripCmd«	External blocking of the Trip Command of the module/the stage, if blocking is activated (allowed) within a parameter set and if the state of the assigned signal is true.

3.5.1.4.4 Protection Para / Global Prot Para / f-Prot / f[4]

	»ExBlo1«	External blocking of the module, if blocking is activated (allowed) within a parameter set and if the state of the assigned signal is true.
	»ExBlo2«	External blocking of the module, if blocking is activated (allowed) within a parameter set and if the state of the assigned signal is true.
	»ExBlo TripCmd«	External blocking of the Trip Command of the module/the stage, if blocking is activated (allowed) within a parameter set and if the state of the assigned signal is true.

3.5.1.4.5 Protection Para / Global Prot Para / f-Prot / f[5]

	»ExBlo1«	External blocking of the module, if blocking is activated (allowed) within a parameter set and if the state of the assigned signal is true.
	»ExBlo2«	External blocking of the module, if blocking is activated (allowed) within a parameter set and if the state of the assigned signal is true.
	»ExBlo TripCmd«	External blocking of the Trip Command of the module/the stage, if blocking is activated (allowed) within a parameter set and if the state of the assigned signal is true.

3.5.1.4.6 Protection Para / Global Prot Para / f-Prot / f[6]

	»ExBlo1«	External blocking of the module, if blocking is activated (allowed) within a parameter set and if the state of the assigned signal is true.
	»ExBlo2«	External blocking of the module, if blocking is activated (allowed) within a parameter set and if the state of the assigned signal is true.
	»ExBlo TripCmd«	External blocking of the Trip Command of the module/the stage, if blocking is activated (allowed) within a parameter set and if the state of the assigned signal is true.

3.5.1.5 Protection Para / Global Prot Para / ExP

3.5.1.5.1 Protection Para / Global Prot Para / ExP / ExP[1]

	»ExBlo1«	External blocking of the module, if blocking is activated (allowed) within a parameter set and if the state of the assigned signal is true.
	»ExBlo2«	External blocking of the module, if blocking is activated (allowed) within a parameter set and if the state of the assigned signal is true.
	»ExBlo TripCmd«	External blocking of the Trip Command of the module/the stage, if blocking is activated (allowed) within a parameter set and if the state of the assigned signal is true.
	»Alarm«	Assignment for External Alarm
	»Trip«	External trip of the CB if the state of the assigned signal is true.

3.5.1.5.2 Protection Para / Global Prot Para / ExP / ExP[2]

	»ExBlo1«	External blocking of the module, if blocking is activated (allowed) within a parameter set and if the state of the assigned signal is true.
	»ExBlo2«	External blocking of the module, if blocking is activated (allowed) within a parameter set and if the state of the assigned signal is true.
	»ExBlo TripCmd«	External blocking of the Trip Command of the module/the stage, if blocking is activated (allowed) within a parameter set and if the state of the assigned signal is true.
	»Alarm«	Assignment for External Alarm
	»Trip«	External trip of the CB if the state of the assigned signal is true.

3.5.1.5.3 Protection Para / Global Prot Para / ExP / ExP[3]

	»ExBlo1«	External blocking of the module, if blocking is activated (allowed) within a parameter set and if the state of the assigned signal is true.
	»ExBlo2«	External blocking of the module, if blocking is activated (allowed) within a parameter set and if the state of the assigned signal is true.
	»ExBlo TripCmd«	External blocking of the Trip Command of the module/the stage, if blocking is activated (allowed) within a parameter set and if the state of the assigned signal is true.
	»Alarm«	Assignment for External Alarm
	»Trip«	External trip of the CB if the state of the assigned signal is true.

3.5.1.5.4 Protection Para / Global Prot Para / ExP / ExP[4]

	»ExBlo1«	External blocking of the module, if blocking is activated (allowed) within a parameter set and if the state of the assigned signal is true.
	»ExBlo2«	External blocking of the module, if blocking is activated (allowed) within a parameter set and if the state of the assigned signal is true.
	»ExBlo TripCmd«	External blocking of the Trip Command of the module/the stage, if blocking is activated (allowed) within a parameter set and if the state of the assigned signal is true.
	»Alarm«	Assignment for External Alarm
	»Trip«	External trip of the CB if the state of the assigned signal is true.

3.5.1.6 Protection Para / Global Prot Para / Supervision

3.5.1.6.1 Protection Para / Global Prot Para / Supervision / CBF

	»ExBlo1«	External blocking of the module, if blocking is activated (allowed) within a parameter set and if the state of the assigned signal is true.
	»ExBlo2«	External blocking of the module, if blocking is activated (allowed) within a parameter set and if the state of the assigned signal is true.
	»Trigger«	Determining the trigger mode for the Breaker Failure.
	»Trigger1«	Trigger that will start the CBF
	»Trigger2«	Trigger that will start the CBF
	»Trigger3«	Trigger that will start the CBF

3.5.1.6.2 Protection Para / Global Prot Para / Supervision / TCS

	»Mode«	Select if trip circuit is going to be monitored when the breaker is closed or when the breaker is either open or close.
	»Input 1«	Select the input configured to monitor the trip coil when the breaker is closed.
	»Input 2«	Select the input configured to monitor the trip coil when the breaker is open. Only available if Mode set to “Either”.
	»ExBlo1«	External blocking of the module, if blocking is activated (allowed) within a parameter set and if the state of the assigned signal is true.
	»ExBlo2«	External blocking of the module, if blocking is activated (allowed) within a parameter set and if the state of the assigned signal is true.

3.5.1.6.3 Protection Para / Global Prot Para / Supervision / VTS

	»ExBlo1«	External blocking of the module, if blocking is activated (allowed) within a parameter set and if the state of the assigned signal is true.
	»ExBlo2«	External blocking of the module, if blocking is activated (allowed) within a parameter set and if the state of the assigned signal is true.
	»Ex FF VT-I«	State of the module input: Alarm Fuse Failure Voltage Transformers
	»Ex FF EVT-I«	State of the module input: Alarm Fuse Failure Earth Voltage Transformers

3.5.2 Protection Para / PSet-Switch

	»Act Set«	Signal: Active Parameter Set
	»PSet-Switch«	Switching Parameter Set
	»PS1: activated by«	This Setting Group will be the active one if: The Parameter Setting Group Switch is set to "Switch via Input" and the other three input functions are inactive at the same time. In case that there is more than one input function active, no Parameter Setting Group Switch will be executed. In case all input functions are inactive, the device will keep working with the Setting Group that was activated lastly.
	»PS2: activated by«	This Setting Group will be the active one if: The Parameter Setting Group Switch is set to "Switch via Input" and the other three input functions are inactive at the same time. In case that there is more than one input function active, no Parameter Setting Group Switch will be executed. In case all input functions are inactive, the device will keep working with the Setting Group that was activated lastly.
	»PS3: activated by«	This Setting Group will be the active one if: The Parameter Setting Group Switch is set to "Switch via Input" and the other three input functions are inactive at the same time. In case that there is more than one input function active, no Parameter Setting Group Switch will be executed. In case all input functions are inactive, the device will keep working with the Setting Group that was activated lastly.
	»PS4: activated by«	This Setting Group will be the active one if: The Parameter Setting Group Switch is set to "Switch via Input" and the other three input functions are inactive at the same time. In case that there is more than one input function active, no Parameter Setting Group Switch will be executed. In case all input functions are inactive, the device will keep working with the Setting Group that was activated lastly.

3.5.3 Protection Para / Set 1 ... 4

3.5.3.1 Protection Para / Set 1 ... 4 / Intercon-Prot

3.5.3.1.1 Protection Para / Set 1 ... 4 / Intercon-Prot / Mains Decouplg

3.5.3.1.1.1 Protection Para / Set 1 ... 4 / Intercon-Prot / Mains Decouplg / df/dt

	»Function«	Permanent activation or deactivation of module/stage.
	»ExBlo Fc«	Activate (allow) or inactivate (disallow) blocking of the module/stage. This parameter is only effective if a signal is assigned to the corresponding global protection parameter. If the signal becomes true, those modules/stages are blocked that are parameterized "ExBlo Fc=active".
	»Blo TripCmd«	Permanent blocking of the Trip Command of the module/stage.
	»ExBlo TripCmd Fc«	Activate (allow) or inactivate (disallow) blocking of the module/stage. This parameter is only effective if a signal is assigned to the corresponding global protection parameter. If the signal becomes true, those modules/stages are blocked that are parameterized "ExBlo TripCmd Fc=active".
	»df/dt«	Measured value (calculated): Rate-of-frequency-change.
	»t-df/dt«	Trip delay df/dt
	»df/dt mode«	df/dt mode

3.5.3.1.1.2 Protection Para / Set 1 ... 4 / Intercon-Prot / Mains Decouplg / delta phi

	»Function«	Permanent activation or deactivation of module/stage.
	»ExBlo Fc«	Activate (allow) or inactivate (disallow) blocking of the module/stage. This parameter is only effective if a signal is assigned to the corresponding global protection parameter. If the signal becomes true, those modules/stages are blocked that are parameterized "ExBlo Fc=active".
	»Blo TripCmd«	Permanent blocking of the Trip Command of the module/stage.
	»ExBlo TripCmd Fc«	Activate (allow) or inactivate (disallow) blocking of the module/stage. This parameter is only effective if a signal is assigned to the corresponding global protection parameter. If the signal becomes true, those modules/stages are blocked that are parameterized "ExBlo TripCmd Fc=active".
	»delta phi«	Measured value (calculated): Vector surge

3.5.3.1.1.3 Protection Para / Set 1 ... 4 / Intercon-Prot / Mains Decouplg / Intertripping

	»Function«	Permanent activation or deactivation of module/stage.
	»ExBlo Fc«	Activate (allow) or inactivate (disallow) blocking of the module/stage. This parameter is only effective if a signal is assigned to the corresponding global protection parameter. If the signal becomes true, those modules/stages are blocked that are parameterized "ExBlo Fc=active".
	»Blo TripCmd«	Permanent blocking of the Trip Command of the module/stage.
	»ExBlo TripCmd Fc«	Activate (allow) or inactivate (disallow) blocking of the module/stage. This parameter is only effective if a signal is assigned to the corresponding global protection parameter. If the signal becomes true, those modules/stages are blocked that are parameterized "ExBlo TripCmd Fc=active".

3.5.3.1.2 Protection Para / Set 1 ... 4 / Intercon-Prot / LVRT[1]

3.5.3.1.2.1 Protection Para / Set 1 ... 4 / Intercon-Prot / LVRT[1] / General Settings

	»Function«	Permanent activation or deactivation of module/stage.
	»ExBlo Fc«	Activate (allow) or inactivate (disallow) blocking of the module/stage. This parameter is only effective if a signal is assigned to the corresponding global protection parameter. If the signal becomes true, those modules/stages are blocked that are parameterized "ExBlo Fc=active".
	»Blo TripCmd«	Permanent blocking of the Trip Command of the module/stage.
	»ExBlo TripCmd Fc«	Activate (allow) or inactivate (disallow) blocking of the module/stage. This parameter is only effective if a signal is assigned to the corresponding global protection parameter. If the signal becomes true, those modules/stages are blocked that are parameterized "ExBlo TripCmd Fc=active".
	»Measuring Mode«	Measuring/Supervision Mode: Determines if the phase-to-phase or phase-to-earth voltages are to be supervised
	»Measuring method«	Measuring method: fundamental or rms or 3rd harmonic (only generator protection relays)
	»Alarm Mode«	Alarm criterion for the voltage protection stage.
	»Meas Circuit Superv«	Activates the use of the measuring circuit supervision. In this case the module will be blocked if a measuring circuit supervision module (e.g. LOP, VTS) signals a disturbed measuring circuit (e.g. caused by a fuse failure).
	»AR controlled LVRT«	Activates the supervision of the number of voltage dips during a defined time (t-LVRT).
	»Number of V dips to trip«	Number of voltage dips until the disconnection signal (trip) will be issued.
	»t-LVRT«	This timer defines the supervision interval (window/period) for counting the number of voltage dips to trip (“No of V dips to trip”). The first voltage dip will start the timer. The counted number of voltage dips will be reset if the timer is expired. The timer will also be reset if the maximum “No of V dips to trip” is reached.

3.5.3.1.2.2 Protection Para / Set 1 ... 4 / Intercon-Prot / LVRT[1] / LVRT Profile

	»Vstart<«	A voltage dip is detected if the measured voltage falls below this threshold.
	»Vrecover>«	The voltage is recovered if the measured voltage raises above this threshold.
	»V(t1)« ... »V(t10)«	Voltage value of a point V(t(n)). These points define the LVRT profile.
	»t1« ... »t10«	Point in time for the corresponding voltage value V(t(n)). These points define the LVRT profile.

3.5.3.1.3 Protection Para / Set 1 ... 4 / Intercon-Prot / LVRT[2]

3.5.3.1.3.1 Protection Para / Set 1 ... 4 / Intercon-Prot / LVRT[2] / General Settings

	»Function«	Permanent activation or deactivation of module/stage.
	»ExBlo Fc«	Activate (allow) or inactivate (disallow) blocking of the module/stage. This parameter is only effective if a signal is assigned to the corresponding global protection parameter. If the signal becomes true, those modules/stages are blocked that are parameterized "ExBlo Fc=active".
	»Blo TripCmd«	Permanent blocking of the Trip Command of the module/stage.
	»ExBlo TripCmd Fc«	Activate (allow) or inactivate (disallow) blocking of the module/stage. This parameter is only effective if a signal is assigned to the corresponding global protection parameter. If the signal becomes true, those modules/stages are blocked that are parameterized "ExBlo TripCmd Fc=active".
	»Measuring Mode«	Measuring/Supervision Mode: Determines if the phase-to-phase or phase-to-earth voltages are to be supervised
	»Measuring method«	Measuring method: fundamental or rms or 3rd harmonic (only generator protection relays)
	»Alarm Mode«	Alarm criterion for the voltage protection stage.
	»Meas Circuit Superv«	Activates the use of the measuring circuit supervision. In this case the module will be blocked if a measuring circuit supervision module (e.g. LOP, VTS) signals a disturbed measuring circuit (e.g. caused by a fuse failure).
	»AR controlled LVRT«	Activates the supervision of the number of voltage dips during a defined time (t-LVRT).
	»Number of V dips to trip«	Number of voltage dips until the disconnection signal (trip) will be issued.
	»t-LVRT«	This timer defines the supervision interval (window/period) for counting the number of voltage dips to trip (“No of V dips to trip”). The first voltage dip will start the timer. The counted number of voltage dips will be reset if the timer is expired. The timer will also be reset if the maximum “No of V dips to trip” is reached.

3.5.3.1.3.2 Protection Para / Set 1 ... 4 / Intercon-Prot / LVRT[2] / LVRT Profile

	»Vstart<«	A voltage dip is detected if the measured voltage falls below this threshold.
	»Vrecover>«	The voltage is recovered if the measured voltage raises above this threshold.
	»V(t1)« ... »V(t10)«	Voltage value of a point V(t(n)). These points define the LVRT profile.
	»t1« ... »t10«	Point in time for the corresponding voltage value V(t(n)). These points define the LVRT profile.

3.5.3.1.4 Protection Para / Set 1 ... 4 / Intercon-Prot / ReCon[1]

3.5.3.1.4.1 Protection Para / Set 1 ... 4 / Intercon-Prot / ReCon[1] / General Settings

	»Function«	Permanent activation or deactivation of module/stage.
	»ExBlo Fc«	Activate (allow) or inactivate (disallow) blocking of the module/stage. This parameter is only effective if a signal is assigned to the corresponding global protection parameter. If the signal becomes true, those modules/stages are blocked that are parameterized "ExBlo Fc=active".
	»Meas Circuit Superv«	Activates the use of the measuring circuit supervision. In this case the module will be blocked if a measuring circuit supervision module (e.g. LOP, VTS) signals a disturbed measuring circuit (e.g. caused by a fuse failure).
	»V Ext Release PCC Fc«	Activate the release signal of the Point of Common Coupling. The line-to-line voltage is greater than 95% of VN.

3.5.3.1.4.2 Protection Para / Set 1 ... 4 / Intercon-Prot / ReCon[1] / Release Para

	»Reconnect. Release Cond«	This parameter ensures that the mains voltage is recovered.
	»PCC Fuse Fail VT Fk«	Blocking if the fuse of a voltage transformer has tripped at the PCC.
	»Measuring method«	Measuring method: fundamental or rms or "sliding average supervision"
	»VLL max Release«	Maximum voltage (line-to-line) for reclosure (Restoration Voltage)
	»VLL min Release«	Minimum voltage (line-to-line) for reclosure (Restoration Voltage)
	»f max Release«	Upper frequency limit for the reclosure
	»f min Release«	Lower frequency limit for the reclosure (Restoration Voltage)
	»t-Release Blo«	Time stage (delay) for the reclosure of the energy resources. The Mains seddle time takes based on exirience approx. 10 - 15 minutes.

3.5.3.1.5 Protection Para / Set 1 ... 4 / Intercon-Prot / ReCon[2]

3.5.3.1.5.1 Protection Para / Set 1 ... 4 / Intercon-Prot / ReCon[2] / General Settings

	»Function«	Permanent activation or deactivation of module/stage.
	»ExBlo Fc«	Activate (allow) or inactivate (disallow) blocking of the module/stage. This parameter is only effective if a signal is assigned to the corresponding global protection parameter. If the signal becomes true, those modules/stages are blocked that are parameterized "ExBlo Fc=active".
	»Meas Circuit Superv«	Activates the use of the measuring circuit supervision. In this case the module will be blocked if a measuring circuit supervision module (e.g. LOP, VTS) signals a disturbed measuring circuit (e.g. caused by a fuse failure).
	»V Ext Release PCC Fc«	Activate the release signal of the Point of Common Coupling. The line-to-line voltage is greater than 95% of VN.

3.5.3.1.5.2 Protection Para / Set 1 ... 4 / Intercon-Prot / ReCon[2] / Release Para

	»Reconnect. Release Cond«	This parameter ensures that the mains voltage is recovered.
	»PCC Fuse Fail VT Fk«	Blocking if the fuse of a voltage transformer has tripped at the PCC.
	»Measuring method«	Measuring method: fundamental or rms or "sliding average supervision"
	»VLL max Release«	Maximum voltage (line-to-line) for reclosure (Restoration Voltage)
	»VLL min Release«	Minimum voltage (line-to-line) for reclosure (Restoration Voltage)
	»f max Release«	Upper frequency limit for the reclosure
	»f min Release«	Lower frequency limit for the reclosure (Restoration Voltage)
	»t-Release Blo«	Time stage (delay) for the reclosure of the energy resources. The Mains seddle time takes based on exirience approx. 10 - 15 minutes.

3.5.3.1.6 Protection Para / Set 1 ... 4 / Intercon-Prot / Sync

3.5.3.1.6.1 Protection Para / Set 1 ... 4 / Intercon-Prot / Sync / General Settings

	»Function«	Permanent activation or deactivation of module/stage.
	»ExBlo Fc«	Activate (allow) or inactivate (disallow) blocking of the module/stage. This parameter is only effective if a signal is assigned to the corresponding global protection parameter. If the signal becomes true, those modules/stages are blocked that are parameterized "ExBlo Fc=active".
	»Bypass Fc«	Allowing to bypass the Synchrocheck, if the state signal that is assigned to the parameter with the same name within the Global Parameters (logic input) becomes true.

3.5.3.1.6.2 Protection Para / Set 1 ... 4 / Intercon-Prot / Sync / Mode / Times

	»SyncMode«	Synchrocheck mode: GENERATOR2SYSTEM = Synchronizing generator to system (breaker close initiate needed). SYSTEM2SYSTEM = SynchronCheck between two systems (Stand-Alone, no breaker info needed)
	»t-MaxCBCloseDelay«	Maximum circuit breaker close time delay (Only used for GENERATOR-SYSTEM working mode and is critical for a correct synchronized switching)
	»t-MaxSyncSuperv«	Synchron-Run timer: Max. time allowed for synchronizing process after a close initiate. Only used for GENERATOR2SYSTEM working mode.

3.5.3.1.6.3 Protection Para / Set 1 ... 4 / Intercon-Prot / Sync / DeadLiveVLevels

	»MinLiveBusVoltage«	Minimum Live Bus voltage (Live bus detected, when all three phase bus voltages are above this limit).
	»MaxDeadBusVoltage«	Maximum Dead Bus voltage (Dead bus detected, when all three phase bus voltages are below this limit).
	»MinLiveLineVoltage«	Minimum Live Line voltage (Live line detected, when line voltage above this limit).
	»MaxDeadLineVoltage«	Maximum Dead Line voltage (Dead Line detected, when line voltage below this limit).
	»t-VoltDead«	Voltage dead time (A Dead Bus/Line condition will be accepted only if the voltage falls below the set dead voltage levels longer than this time setting).

3.5.3.1.6.4 Protection Para / Set 1 ... 4 / Intercon-Prot / Sync / Conditions

	»MaxVoltageDiff«	Maximum voltage difference between bus and line voltage phasors (Delta V)for synchronism (Related to bus voltage secondary rating)
	»MaxSlipFrequency«	Maximum frequency difference (Slip: Delta f) between bus and line voltage allowed for synchronism
	»MaxAngleDiff«	Maximum phase angle difference (Delta-Phi in degree) between bus and line voltages allowed for synchronism

3.5.3.1.6.5 Protection Para / Set 1 ... 4 / Intercon-Prot / Sync / Override

	»DBDL«	Enable/disable Dead-Bus AND Dead-Line synchronism overriding
	»DBLL«	Enable/disable Dead-Bus AND Live-Line synchronism overriding
	»LBDL«	Enable/disable Live-Bus AND Dead-Line synchronism overriding

3.5.3.2 Protection Para / Set 1 ... 4 / V-Prot

3.5.3.2.1 Protection Para / Set 1 ... 4 / V-Prot / V[1]

	»Function«	Permanent activation or deactivation of module/stage.
	»ExBlo Fc«	Activate (allow) or inactivate (disallow) blocking of the module/stage. This parameter is only effective if a signal is assigned to the corresponding global protection parameter. If the signal becomes true, those modules/stages are blocked that are parameterized "ExBlo Fc=active".
	»Blo TripCmd«	Permanent blocking of the Trip Command of the module/stage.
	»ExBlo TripCmd Fc«	Activate (allow) or inactivate (disallow) blocking of the module/stage. This parameter is only effective if a signal is assigned to the corresponding global protection parameter. If the signal becomes true, those modules/stages are blocked that are parameterized "ExBlo TripCmd Fc=active".
	»Measuring Mode«	Measuring/Supervision Mode: Determines if the phase-to-phase or phase-to-earth voltages are to be supervised
	»Measuring method«	Measuring method: fundamental or rms or "sliding average supervision"
	»Alarm Mode«	Alarm criterion for the voltage protection stage.
	»V>«	If the pickup value is exceeded, the module/element will be started. If the pickup value is exceeded, the module/element will be started. The definition of Vn is dependent on both the Field Parameter »VT con« and the Setting Group Parameter »Measuring Mode«: If the measuring inputs of the voltage measuring card are fed with phase-to-ground voltages (»VT con« = "Phase-to-Ground") then the setting »Measuring Mode« = "Phase-to-Ground" means that Vn=VTsec/√3, and »Measuring Mode« = "Phase-to-Phase" means that Vn=VTsec. if the measuring inputs of the voltage measuring card are fed with phase-to-phase voltages (»VT con« = "Phase-to-Phase") then only following setting is possible: »Measuring Mode« = "Phase-to-Phase" means that Vn=VTsec.
	»V> Reset«	Drop Out (is in percent of setting)
	»V<«	If the pickup value is exceeded, the module/element will be started. If the pickup value is exceeded, the module/element will be started. The definition of Vn is dependent on both the Field Parameter »VT con« and the Setting Group Parameter »Measuring Mode«: If the measuring inputs of the voltage measuring card are fed with phase-to-ground voltages (»VT con« = "Phase-to-Ground") then the setting »Measuring Mode« = "Phase-to-Ground" means that Vn=VTsec/√3, and »Measuring Mode« = "Phase-to-Phase" means that Vn=VTsec. if the measuring inputs of the voltage measuring card are fed with phase-to-phase voltages (»VT con« = "Phase-to-Phase") then only following setting is possible: »Measuring Mode« = "Phase-to-Phase" means that Vn=VTsec.
	»V< Reset«	Drop Out (is in percent of setting)
	»t«	Tripping delay
	»Meas Circuit Superv«	Activates the use of the measuring circuit supervision. In this case the module will be blocked if a measuring circuit supervision module (e.g. LOP, VTS) signals a disturbed measuring circuit (e.g. caused by a fuse failure).

3.5.3.2.2 Protection Para / Set 1 ... 4 / V-Prot / V[2]

	»Function«	Permanent activation or deactivation of module/stage.
	»ExBlo Fc«	Activate (allow) or inactivate (disallow) blocking of the module/stage. This parameter is only effective if a signal is assigned to the corresponding global protection parameter. If the signal becomes true, those modules/stages are blocked that are parameterized "ExBlo Fc=active".
	»Blo TripCmd«	Permanent blocking of the Trip Command of the module/stage.
	»ExBlo TripCmd Fc«	Activate (allow) or inactivate (disallow) blocking of the module/stage. This parameter is only effective if a signal is assigned to the corresponding global protection parameter. If the signal becomes true, those modules/stages are blocked that are parameterized "ExBlo TripCmd Fc=active".
	»Measuring Mode«	Measuring/Supervision Mode: Determines if the phase-to-phase or phase-to-earth voltages are to be supervised
	»Measuring method«	Measuring method: fundamental or rms or "sliding average supervision"
	»Alarm Mode«	Alarm criterion for the voltage protection stage.
	»V>«	If the pickup value is exceeded, the module/element will be started. If the pickup value is exceeded, the module/element will be started. The definition of Vn is dependent on both the Field Parameter »VT con« and the Setting Group Parameter »Measuring Mode«: If the measuring inputs of the voltage measuring card are fed with phase-to-ground voltages (»VT con« = "Phase-to-Ground") then the setting »Measuring Mode« = "Phase-to-Ground" means that Vn=VTsec/√3, and »Measuring Mode« = "Phase-to-Phase" means that Vn=VTsec. if the measuring inputs of the voltage measuring card are fed with phase-to-phase voltages (»VT con« = "Phase-to-Phase") then only following setting is possible: »Measuring Mode« = "Phase-to-Phase" means that Vn=VTsec.
	»V> Reset«	Drop Out (is in percent of setting)
	»V<«	If the pickup value is exceeded, the module/element will be started. If the pickup value is exceeded, the module/element will be started. The definition of Vn is dependent on both the Field Parameter »VT con« and the Setting Group Parameter »Measuring Mode«: If the measuring inputs of the voltage measuring card are fed with phase-to-ground voltages (»VT con« = "Phase-to-Ground") then the setting »Measuring Mode« = "Phase-to-Ground" means that Vn=VTsec/√3, and »Measuring Mode« = "Phase-to-Phase" means that Vn=VTsec. if the measuring inputs of the voltage measuring card are fed with phase-to-phase voltages (»VT con« = "Phase-to-Phase") then only following setting is possible: »Measuring Mode« = "Phase-to-Phase" means that Vn=VTsec.
	»V< Reset«	Drop Out (is in percent of setting)
	»t«	Tripping delay
	»Meas Circuit Superv«	Activates the use of the measuring circuit supervision. In this case the module will be blocked if a measuring circuit supervision module (e.g. LOP, VTS) signals a disturbed measuring circuit (e.g. caused by a fuse failure).

3.5.3.2.3 Protection Para / Set 1 ... 4 / V-Prot / V[3]

	»Function«	Permanent activation or deactivation of module/stage.
	»ExBlo Fc«	Activate (allow) or inactivate (disallow) blocking of the module/stage. This parameter is only effective if a signal is assigned to the corresponding global protection parameter. If the signal becomes true, those modules/stages are blocked that are parameterized "ExBlo Fc=active".
	»Blo TripCmd«	Permanent blocking of the Trip Command of the module/stage.
	»ExBlo TripCmd Fc«	Activate (allow) or inactivate (disallow) blocking of the module/stage. This parameter is only effective if a signal is assigned to the corresponding global protection parameter. If the signal becomes true, those modules/stages are blocked that are parameterized "ExBlo TripCmd Fc=active".
	»Measuring Mode«	Measuring/Supervision Mode: Determines if the phase-to-phase or phase-to-earth voltages are to be supervised
	»Measuring method«	Measuring method: fundamental or rms or "sliding average supervision"
	»Alarm Mode«	Alarm criterion for the voltage protection stage.
	»V>«	If the pickup value is exceeded, the module/element will be started. If the pickup value is exceeded, the module/element will be started. The definition of Vn is dependent on both the Field Parameter »VT con« and the Setting Group Parameter »Measuring Mode«: If the measuring inputs of the voltage measuring card are fed with phase-to-ground voltages (»VT con« = "Phase-to-Ground") then the setting »Measuring Mode« = "Phase-to-Ground" means that Vn=VTsec/√3, and »Measuring Mode« = "Phase-to-Phase" means that Vn=VTsec. if the measuring inputs of the voltage measuring card are fed with phase-to-phase voltages (»VT con« = "Phase-to-Phase") then only following setting is possible: »Measuring Mode« = "Phase-to-Phase" means that Vn=VTsec.
	»V> Reset«	Drop Out (is in percent of setting)
	»V<«	If the pickup value is exceeded, the module/element will be started. If the pickup value is exceeded, the module/element will be started. The definition of Vn is dependent on both the Field Parameter »VT con« and the Setting Group Parameter »Measuring Mode«: If the measuring inputs of the voltage measuring card are fed with phase-to-ground voltages (»VT con« = "Phase-to-Ground") then the setting »Measuring Mode« = "Phase-to-Ground" means that Vn=VTsec/√3, and »Measuring Mode« = "Phase-to-Phase" means that Vn=VTsec. if the measuring inputs of the voltage measuring card are fed with phase-to-phase voltages (»VT con« = "Phase-to-Phase") then only following setting is possible: »Measuring Mode« = "Phase-to-Phase" means that Vn=VTsec.
	»V< Reset«	Drop Out (is in percent of setting)
	»t«	Tripping delay
	»Meas Circuit Superv«	Activates the use of the measuring circuit supervision. In this case the module will be blocked if a measuring circuit supervision module (e.g. LOP, VTS) signals a disturbed measuring circuit (e.g. caused by a fuse failure).

3.5.3.2.4 Protection Para / Set 1 ... 4 / V-Prot / V[4]

	»Function«	Permanent activation or deactivation of module/stage.
	»ExBlo Fc«	Activate (allow) or inactivate (disallow) blocking of the module/stage. This parameter is only effective if a signal is assigned to the corresponding global protection parameter. If the signal becomes true, those modules/stages are blocked that are parameterized "ExBlo Fc=active".
	»Blo TripCmd«	Permanent blocking of the Trip Command of the module/stage.
	»ExBlo TripCmd Fc«	Activate (allow) or inactivate (disallow) blocking of the module/stage. This parameter is only effective if a signal is assigned to the corresponding global protection parameter. If the signal becomes true, those modules/stages are blocked that are parameterized "ExBlo TripCmd Fc=active".
	»Measuring Mode«	Measuring/Supervision Mode: Determines if the phase-to-phase or phase-to-earth voltages are to be supervised
	»Measuring method«	Measuring method: fundamental or rms or "sliding average supervision"
	»Alarm Mode«	Alarm criterion for the voltage protection stage.
	»V>«	If the pickup value is exceeded, the module/element will be started. If the pickup value is exceeded, the module/element will be started. The definition of Vn is dependent on both the Field Parameter »VT con« and the Setting Group Parameter »Measuring Mode«: If the measuring inputs of the voltage measuring card are fed with phase-to-ground voltages (»VT con« = "Phase-to-Ground") then the setting »Measuring Mode« = "Phase-to-Ground" means that Vn=VTsec/√3, and »Measuring Mode« = "Phase-to-Phase" means that Vn=VTsec. if the measuring inputs of the voltage measuring card are fed with phase-to-phase voltages (»VT con« = "Phase-to-Phase") then only following setting is possible: »Measuring Mode« = "Phase-to-Phase" means that Vn=VTsec.
	»V> Reset«	Drop Out (is in percent of setting)
	»V<«	If the pickup value is exceeded, the module/element will be started. If the pickup value is exceeded, the module/element will be started. The definition of Vn is dependent on both the Field Parameter »VT con« and the Setting Group Parameter »Measuring Mode«: If the measuring inputs of the voltage measuring card are fed with phase-to-ground voltages (»VT con« = "Phase-to-Ground") then the setting »Measuring Mode« = "Phase-to-Ground" means that Vn=VTsec/√3, and »Measuring Mode« = "Phase-to-Phase" means that Vn=VTsec. if the measuring inputs of the voltage measuring card are fed with phase-to-phase voltages (»VT con« = "Phase-to-Phase") then only following setting is possible: »Measuring Mode« = "Phase-to-Phase" means that Vn=VTsec.
	»V< Reset«	Drop Out (is in percent of setting)
	»t«	Tripping delay
	»Meas Circuit Superv«	Activates the use of the measuring circuit supervision. In this case the module will be blocked if a measuring circuit supervision module (e.g. LOP, VTS) signals a disturbed measuring circuit (e.g. caused by a fuse failure).

3.5.3.2.5 Protection Para / Set 1 ... 4 / V-Prot / V[5]

	»Function«	Permanent activation or deactivation of module/stage.
	»ExBlo Fc«	Activate (allow) or inactivate (disallow) blocking of the module/stage. This parameter is only effective if a signal is assigned to the corresponding global protection parameter. If the signal becomes true, those modules/stages are blocked that are parameterized "ExBlo Fc=active".
	»Blo TripCmd«	Permanent blocking of the Trip Command of the module/stage.
	»ExBlo TripCmd Fc«	Activate (allow) or inactivate (disallow) blocking of the module/stage. This parameter is only effective if a signal is assigned to the corresponding global protection parameter. If the signal becomes true, those modules/stages are blocked that are parameterized "ExBlo TripCmd Fc=active".
	»Measuring Mode«	Measuring/Supervision Mode: Determines if the phase-to-phase or phase-to-earth voltages are to be supervised
	»Measuring method«	Measuring method: fundamental or rms or "sliding average supervision"
	»Alarm Mode«	Alarm criterion for the voltage protection stage.
	»V>«	If the pickup value is exceeded, the module/element will be started. If the pickup value is exceeded, the module/element will be started. The definition of Vn is dependent on both the Field Parameter »VT con« and the Setting Group Parameter »Measuring Mode«: If the measuring inputs of the voltage measuring card are fed with phase-to-ground voltages (»VT con« = "Phase-to-Ground") then the setting »Measuring Mode« = "Phase-to-Ground" means that Vn=VTsec/√3, and »Measuring Mode« = "Phase-to-Phase" means that Vn=VTsec. if the measuring inputs of the voltage measuring card are fed with phase-to-phase voltages (»VT con« = "Phase-to-Phase") then only following setting is possible: »Measuring Mode« = "Phase-to-Phase" means that Vn=VTsec.
	»V> Reset«	Drop Out (is in percent of setting)
	»V<«	If the pickup value is exceeded, the module/element will be started. If the pickup value is exceeded, the module/element will be started. The definition of Vn is dependent on both the Field Parameter »VT con« and the Setting Group Parameter »Measuring Mode«: If the measuring inputs of the voltage measuring card are fed with phase-to-ground voltages (»VT con« = "Phase-to-Ground") then the setting »Measuring Mode« = "Phase-to-Ground" means that Vn=VTsec/√3, and »Measuring Mode« = "Phase-to-Phase" means that Vn=VTsec. if the measuring inputs of the voltage measuring card are fed with phase-to-phase voltages (»VT con« = "Phase-to-Phase") then only following setting is possible: »Measuring Mode« = "Phase-to-Phase" means that Vn=VTsec.
	»V< Reset«	Drop Out (is in percent of setting)
	»t«	Tripping delay
	»Meas Circuit Superv«	Activates the use of the measuring circuit supervision. In this case the module will be blocked if a measuring circuit supervision module (e.g. LOP, VTS) signals a disturbed measuring circuit (e.g. caused by a fuse failure).

3.5.3.2.6 Protection Para / Set 1 ... 4 / V-Prot / V[6]

	»Function«	Permanent activation or deactivation of module/stage.
	»ExBlo Fc«	Activate (allow) or inactivate (disallow) blocking of the module/stage. This parameter is only effective if a signal is assigned to the corresponding global protection parameter. If the signal becomes true, those modules/stages are blocked that are parameterized "ExBlo Fc=active".
	»Blo TripCmd«	Permanent blocking of the Trip Command of the module/stage.
	»ExBlo TripCmd Fc«	Activate (allow) or inactivate (disallow) blocking of the module/stage. This parameter is only effective if a signal is assigned to the corresponding global protection parameter. If the signal becomes true, those modules/stages are blocked that are parameterized "ExBlo TripCmd Fc=active".
	»Measuring Mode«	Measuring/Supervision Mode: Determines if the phase-to-phase or phase-to-earth voltages are to be supervised
	»Measuring method«	Measuring method: fundamental or rms or "sliding average supervision"
	»Alarm Mode«	Alarm criterion for the voltage protection stage.
	»V>«	If the pickup value is exceeded, the module/element will be started. If the pickup value is exceeded, the module/element will be started. The definition of Vn is dependent on both the Field Parameter »VT con« and the Setting Group Parameter »Measuring Mode«: If the measuring inputs of the voltage measuring card are fed with phase-to-ground voltages (»VT con« = "Phase-to-Ground") then the setting »Measuring Mode« = "Phase-to-Ground" means that Vn=VTsec/√3, and »Measuring Mode« = "Phase-to-Phase" means that Vn=VTsec. if the measuring inputs of the voltage measuring card are fed with phase-to-phase voltages (»VT con« = "Phase-to-Phase") then only following setting is possible: »Measuring Mode« = "Phase-to-Phase" means that Vn=VTsec.
	»V> Reset«	Drop Out (is in percent of setting)
	»V<«	If the pickup value is exceeded, the module/element will be started. If the pickup value is exceeded, the module/element will be started. The definition of Vn is dependent on both the Field Parameter »VT con« and the Setting Group Parameter »Measuring Mode«: If the measuring inputs of the voltage measuring card are fed with phase-to-ground voltages (»VT con« = "Phase-to-Ground") then the setting »Measuring Mode« = "Phase-to-Ground" means that Vn=VTsec/√3, and »Measuring Mode« = "Phase-to-Phase" means that Vn=VTsec. if the measuring inputs of the voltage measuring card are fed with phase-to-phase voltages (»VT con« = "Phase-to-Phase") then only following setting is possible: »Measuring Mode« = "Phase-to-Phase" means that Vn=VTsec.
	»V< Reset«	Drop Out (is in percent of setting)
	»t«	Tripping delay
	»Meas Circuit Superv«	Activates the use of the measuring circuit supervision. In this case the module will be blocked if a measuring circuit supervision module (e.g. LOP, VTS) signals a disturbed measuring circuit (e.g. caused by a fuse failure).

3.5.3.2.7 Protection Para / Set 1 ... 4 / V-Prot / VG[1]

	»Function«	Permanent activation or deactivation of module/stage.
	»ExBlo Fc«	Activate (allow) or inactivate (disallow) blocking of the module/stage. This parameter is only effective if a signal is assigned to the corresponding global protection parameter. If the signal becomes true, those modules/stages are blocked that are parameterized "ExBlo Fc=active".
	»Blo TripCmd«	Permanent blocking of the Trip Command of the module/stage.
	»ExBlo TripCmd Fc«	Activate (allow) or inactivate (disallow) blocking of the module/stage. This parameter is only effective if a signal is assigned to the corresponding global protection parameter. If the signal becomes true, those modules/stages are blocked that are parameterized "ExBlo TripCmd Fc=active".
	»VG Source«	Selection if VG is measured or calculated (neutral voltage or residual voltage)
	»Measuring method«	Measuring method: fundamental or rms or 3rd harmonic (only generator protection relays)
	»VG>«	If the pickup value is exceeded, the module/stage will be started.
	»VG> Reset«	Drop Out (is in percent of setting)
	»VG<«	Undervoltage Threshold
	»VG< Reset«	Drop Out (is in percent of setting)
	»t«	Tripping delay
	»Meas Circuit Superv«	Activates the use of the measuring circuit supervision. In this case the module will be blocked if a measuring circuit supervision module (e.g. LOP, VTS) signals a disturbed measuring circuit (e.g. caused by a fuse failure).

3.5.3.2.8 Protection Para / Set 1 ... 4 / V-Prot / VG[2]

	»Function«	Permanent activation or deactivation of module/stage.
	»ExBlo Fc«	Activate (allow) or inactivate (disallow) blocking of the module/stage. This parameter is only effective if a signal is assigned to the corresponding global protection parameter. If the signal becomes true, those modules/stages are blocked that are parameterized "ExBlo Fc=active".
	»Blo TripCmd«	Permanent blocking of the Trip Command of the module/stage.
	»ExBlo TripCmd Fc«	Activate (allow) or inactivate (disallow) blocking of the module/stage. This parameter is only effective if a signal is assigned to the corresponding global protection parameter. If the signal becomes true, those modules/stages are blocked that are parameterized "ExBlo TripCmd Fc=active".
	»VG Source«	Selection if VG is measured or calculated (neutral voltage or residual voltage)
	»Measuring method«	Measuring method: fundamental or rms or 3rd harmonic (only generator protection relays)
	»VG>«	If the pickup value is exceeded, the module/stage will be started.
	»VG> Reset«	Drop Out (is in percent of setting)
	»VG<«	Undervoltage Threshold
	»VG< Reset«	Drop Out (is in percent of setting)
	»t«	Tripping delay
	»Meas Circuit Superv«	Activates the use of the measuring circuit supervision. In this case the module will be blocked if a measuring circuit supervision module (e.g. LOP, VTS) signals a disturbed measuring circuit (e.g. caused by a fuse failure).

3.5.3.2.9 Protection Para / Set 1 ... 4 / V-Prot / V012[1]

	»Function«	Permanent activation or deactivation of module/stage.
	»ExBlo Fc«	Activate (allow) or inactivate (disallow) blocking of the module/stage. This parameter is only effective if a signal is assigned to the corresponding global protection parameter. If the signal becomes true, those modules/stages are blocked that are parameterized "ExBlo Fc=active".
	»Blo TripCmd«	Permanent blocking of the Trip Command of the module/stage.
	»ExBlo TripCmd Fc«	Activate (allow) or inactivate (disallow) blocking of the module/stage. This parameter is only effective if a signal is assigned to the corresponding global protection parameter. If the signal becomes true, those modules/stages are blocked that are parameterized "ExBlo TripCmd Fc=active".
	»V1>«	Positive Phase Sequence Overvoltage
	»V1> Reset«	Drop Out (is in percent of setting)
	»V1<«	Positive Phase Sequence Undervoltage
	»V1< Reset«	Drop Out (is in percent of setting)
	»V2>«	Negative Phase Sequence Overvoltage
	»V2> Reset«	Drop Out (is in percent of setting)
	»%(V2/V1)«	The %(V2/V1) setting is the unbalance trip pickup setting. It is defined by the ratio of negative sequence voltage to positive sequence voltage (% Unbalance=V2/V1). Phase sequence will be taken into account automatically.
	»%(V2/V1)«	The %(V2/V1) setting is the unbalance trip pickup setting. It is defined by the ratio of negative sequence voltage to positive sequence voltage (% Unbalance=V2/V1). Phase sequence will be taken into account automatically.
	»t«	Tripping delay
	»Meas Circuit Superv«	Activates the use of the measuring circuit supervision. In this case the module will be blocked if a measuring circuit supervision module (e.g. LOP, VTS) signals a disturbed measuring circuit (e.g. caused by a fuse failure).

3.5.3.2.10 Protection Para / Set 1 ... 4 / V-Prot / V012[2]

	»Function«	Permanent activation or deactivation of module/stage.
	»ExBlo Fc«	Activate (allow) or inactivate (disallow) blocking of the module/stage. This parameter is only effective if a signal is assigned to the corresponding global protection parameter. If the signal becomes true, those modules/stages are blocked that are parameterized "ExBlo Fc=active".
	»Blo TripCmd«	Permanent blocking of the Trip Command of the module/stage.
	»ExBlo TripCmd Fc«	Activate (allow) or inactivate (disallow) blocking of the module/stage. This parameter is only effective if a signal is assigned to the corresponding global protection parameter. If the signal becomes true, those modules/stages are blocked that are parameterized "ExBlo TripCmd Fc=active".
	»V1>«	Positive Phase Sequence Overvoltage
	»V1> Reset«	Drop Out (is in percent of setting)
	»V1<«	Positive Phase Sequence Undervoltage
	»V1< Reset«	Drop Out (is in percent of setting)
	»V2>«	Negative Phase Sequence Overvoltage
	»V2> Reset«	Drop Out (is in percent of setting)
	»%(V2/V1)«	The %(V2/V1) setting is the unbalance trip pickup setting. It is defined by the ratio of negative sequence voltage to positive sequence voltage (% Unbalance=V2/V1). Phase sequence will be taken into account automatically.
	»%(V2/V1)«	The %(V2/V1) setting is the unbalance trip pickup setting. It is defined by the ratio of negative sequence voltage to positive sequence voltage (% Unbalance=V2/V1). Phase sequence will be taken into account automatically.
	»t«	Tripping delay
	»Meas Circuit Superv«	Activates the use of the measuring circuit supervision. In this case the module will be blocked if a measuring circuit supervision module (e.g. LOP, VTS) signals a disturbed measuring circuit (e.g. caused by a fuse failure).

3.5.3.2.11 Protection Para / Set 1 ... 4 / V-Prot / V012[3]

	»Function«	Permanent activation or deactivation of module/stage.
	»ExBlo Fc«	Activate (allow) or inactivate (disallow) blocking of the module/stage. This parameter is only effective if a signal is assigned to the corresponding global protection parameter. If the signal becomes true, those modules/stages are blocked that are parameterized "ExBlo Fc=active".
	»Blo TripCmd«	Permanent blocking of the Trip Command of the module/stage.
	»ExBlo TripCmd Fc«	Activate (allow) or inactivate (disallow) blocking of the module/stage. This parameter is only effective if a signal is assigned to the corresponding global protection parameter. If the signal becomes true, those modules/stages are blocked that are parameterized "ExBlo TripCmd Fc=active".
	»V1>«	Positive Phase Sequence Overvoltage
	»V1> Reset«	Drop Out (is in percent of setting)
	»V1<«	Positive Phase Sequence Undervoltage
	»V1< Reset«	Drop Out (is in percent of setting)
	»V2>«	Negative Phase Sequence Overvoltage
	»V2> Reset«	Drop Out (is in percent of setting)
	»%(V2/V1)«	The %(V2/V1) setting is the unbalance trip pickup setting. It is defined by the ratio of negative sequence voltage to positive sequence voltage (% Unbalance=V2/V1). Phase sequence will be taken into account automatically.
	»%(V2/V1)«	The %(V2/V1) setting is the unbalance trip pickup setting. It is defined by the ratio of negative sequence voltage to positive sequence voltage (% Unbalance=V2/V1). Phase sequence will be taken into account automatically.
	»t«	Tripping delay
	»Meas Circuit Superv«	Activates the use of the measuring circuit supervision. In this case the module will be blocked if a measuring circuit supervision module (e.g. LOP, VTS) signals a disturbed measuring circuit (e.g. caused by a fuse failure).

3.5.3.2.12 Protection Para / Set 1 ... 4 / V-Prot / V012[4]

	»Function«	Permanent activation or deactivation of module/stage.
	»ExBlo Fc«	Activate (allow) or inactivate (disallow) blocking of the module/stage. This parameter is only effective if a signal is assigned to the corresponding global protection parameter. If the signal becomes true, those modules/stages are blocked that are parameterized "ExBlo Fc=active".
	»Blo TripCmd«	Permanent blocking of the Trip Command of the module/stage.
	»ExBlo TripCmd Fc«	Activate (allow) or inactivate (disallow) blocking of the module/stage. This parameter is only effective if a signal is assigned to the corresponding global protection parameter. If the signal becomes true, those modules/stages are blocked that are parameterized "ExBlo TripCmd Fc=active".
	»V1>«	Positive Phase Sequence Overvoltage
	»V1> Reset«	Drop Out (is in percent of setting)
	»V1<«	Positive Phase Sequence Undervoltage
	»V1< Reset«	Drop Out (is in percent of setting)
	»V2>«	Negative Phase Sequence Overvoltage
	»V2> Reset«	Drop Out (is in percent of setting)
	»%(V2/V1)«	The %(V2/V1) setting is the unbalance trip pickup setting. It is defined by the ratio of negative sequence voltage to positive sequence voltage (% Unbalance=V2/V1). Phase sequence will be taken into account automatically.
	»%(V2/V1)«	The %(V2/V1) setting is the unbalance trip pickup setting. It is defined by the ratio of negative sequence voltage to positive sequence voltage (% Unbalance=V2/V1). Phase sequence will be taken into account automatically.
	»t«	Tripping delay
	»Meas Circuit Superv«	Activates the use of the measuring circuit supervision. In this case the module will be blocked if a measuring circuit supervision module (e.g. LOP, VTS) signals a disturbed measuring circuit (e.g. caused by a fuse failure).

3.5.3.2.13 Protection Para / Set 1 ... 4 / V-Prot / V012[5]

	»Function«	Permanent activation or deactivation of module/stage.
	»ExBlo Fc«	Activate (allow) or inactivate (disallow) blocking of the module/stage. This parameter is only effective if a signal is assigned to the corresponding global protection parameter. If the signal becomes true, those modules/stages are blocked that are parameterized "ExBlo Fc=active".
	»Blo TripCmd«	Permanent blocking of the Trip Command of the module/stage.
	»ExBlo TripCmd Fc«	Activate (allow) or inactivate (disallow) blocking of the module/stage. This parameter is only effective if a signal is assigned to the corresponding global protection parameter. If the signal becomes true, those modules/stages are blocked that are parameterized "ExBlo TripCmd Fc=active".
	»V1>«	Positive Phase Sequence Overvoltage
	»V1> Reset«	Drop Out (is in percent of setting)
	»V1<«	Positive Phase Sequence Undervoltage
	»V1< Reset«	Drop Out (is in percent of setting)
	»V2>«	Negative Phase Sequence Overvoltage
	»V2> Reset«	Drop Out (is in percent of setting)
	»%(V2/V1)«	The %(V2/V1) setting is the unbalance trip pickup setting. It is defined by the ratio of negative sequence voltage to positive sequence voltage (% Unbalance=V2/V1). Phase sequence will be taken into account automatically.
	»%(V2/V1)«	The %(V2/V1) setting is the unbalance trip pickup setting. It is defined by the ratio of negative sequence voltage to positive sequence voltage (% Unbalance=V2/V1). Phase sequence will be taken into account automatically.
	»t«	Tripping delay
	»Meas Circuit Superv«	Activates the use of the measuring circuit supervision. In this case the module will be blocked if a measuring circuit supervision module (e.g. LOP, VTS) signals a disturbed measuring circuit (e.g. caused by a fuse failure).

3.5.3.2.14 Protection Para / Set 1 ... 4 / V-Prot / V012[6]

	»Function«	Permanent activation or deactivation of module/stage.
	»ExBlo Fc«	Activate (allow) or inactivate (disallow) blocking of the module/stage. This parameter is only effective if a signal is assigned to the corresponding global protection parameter. If the signal becomes true, those modules/stages are blocked that are parameterized "ExBlo Fc=active".
	»Blo TripCmd«	Permanent blocking of the Trip Command of the module/stage.
	»ExBlo TripCmd Fc«	Activate (allow) or inactivate (disallow) blocking of the module/stage. This parameter is only effective if a signal is assigned to the corresponding global protection parameter. If the signal becomes true, those modules/stages are blocked that are parameterized "ExBlo TripCmd Fc=active".
	»V1>«	Positive Phase Sequence Overvoltage
	»V1> Reset«	Drop Out (is in percent of setting)
	»V1<«	Positive Phase Sequence Undervoltage
	»V1< Reset«	Drop Out (is in percent of setting)
	»V2>«	Negative Phase Sequence Overvoltage
	»V2> Reset«	Drop Out (is in percent of setting)
	»%(V2/V1)«	The %(V2/V1) setting is the unbalance trip pickup setting. It is defined by the ratio of negative sequence voltage to positive sequence voltage (% Unbalance=V2/V1). Phase sequence will be taken into account automatically.
	»%(V2/V1)«	The %(V2/V1) setting is the unbalance trip pickup setting. It is defined by the ratio of negative sequence voltage to positive sequence voltage (% Unbalance=V2/V1). Phase sequence will be taken into account automatically.
	»t«	Tripping delay
	»Meas Circuit Superv«	Activates the use of the measuring circuit supervision. In this case the module will be blocked if a measuring circuit supervision module (e.g. LOP, VTS) signals a disturbed measuring circuit (e.g. caused by a fuse failure).

3.5.3.3 Protection Para / Set 1 … 4 / f-Prot

3.5.3.3.1 Protection Para / Set 1 … 4 / f-Prot / f[1]

	»Function«	Permanent activation or deactivation of module/stage.
	»ExBlo Fc«	Activate (allow) or inactivate (disallow) blocking of the module/stage. This parameter is only effective if a signal is assigned to the corresponding global protection parameter. If the signal becomes true, those modules/stages are blocked that are parameterized "ExBlo Fc=active".
	»Blo TripCmd«	Permanent blocking of the Trip Command of the module/stage.
	»ExBlo TripCmd Fc«	Activate (allow) or inactivate (disallow) blocking of the module/stage. This parameter is only effective if a signal is assigned to the corresponding global protection parameter. If the signal becomes true, those modules/stages are blocked that are parameterized "ExBlo TripCmd Fc=active".
	»f>«	Pickup value for overfrequency.
	»f<«	Pickup value for underfrequency.
	»Freq. drop-off«	Drop-off for the Frequency function. This setting modifies the shape of the hysteresis that is used for the frequency protection.
	»t«	Tripping delay
	»df/dt«	Measured value (calculated): Rate-of-frequency-change.
	»t-df/dt«	Trip delay df/dt
	»DF«	Frequency difference for the maximum admissible variation of the mean of the rate of frequency-change. This function is inactive if DF=0.
	»DT«	Time interval of the maximum admissible rate-of-frequency-change.
	»df/dt mode«	df/dt mode
	»delta phi«	Measured value (calculated): Vector surge

3.5.3.3.2 Protection Para / Set 1 ... 4 / f-Prot / f[2]

	»Function«	Permanent activation or deactivation of module/stage.
	»ExBlo Fc«	Activate (allow) or inactivate (disallow) blocking of the module/stage. This parameter is only effective if a signal is assigned to the corresponding global protection parameter. If the signal becomes true, those modules/stages are blocked that are parameterized "ExBlo Fc=active".
	»Blo TripCmd«	Permanent blocking of the Trip Command of the module/stage.
	»ExBlo TripCmd Fc«	Activate (allow) or inactivate (disallow) blocking of the module/stage. This parameter is only effective if a signal is assigned to the corresponding global protection parameter. If the signal becomes true, those modules/stages are blocked that are parameterized "ExBlo TripCmd Fc=active".
	»f>«	Pickup value for overfrequency.
	»f<«	Pickup value for underfrequency.
	»Freq. drop-off«	Drop-off for the Frequency function. This setting modifies the shape of the hysteresis that is used for the frequency protection.
	»t«	Tripping delay
	»df/dt«	Measured value (calculated): Rate-of-frequency-change.
	»t-df/dt«	Trip delay df/dt
	»DF«	Frequency difference for the maximum admissible variation of the mean of the rate of frequency-change. This function is inactive if DF=0.
	»DT«	Time interval of the maximum admissible rate-of-frequency-change.
	»df/dt mode«	df/dt mode
	»delta phi«	Measured value (calculated): Vector surge

3.5.3.3.3 Protection Para / Set 1 ... 4 / f-Prot / f[3]

	»Function«	Permanent activation or deactivation of module/stage.
	»ExBlo Fc«	Activate (allow) or inactivate (disallow) blocking of the module/stage. This parameter is only effective if a signal is assigned to the corresponding global protection parameter. If the signal becomes true, those modules/stages are blocked that are parameterized "ExBlo Fc=active".
	»Blo TripCmd«	Permanent blocking of the Trip Command of the module/stage.
	»ExBlo TripCmd Fc«	Activate (allow) or inactivate (disallow) blocking of the module/stage. This parameter is only effective if a signal is assigned to the corresponding global protection parameter. If the signal becomes true, those modules/stages are blocked that are parameterized "ExBlo TripCmd Fc=active".
	»f>«	Pickup value for overfrequency.
	»f<«	Pickup value for underfrequency.
	»Freq. drop-off«	Drop-off for the Frequency function. This setting modifies the shape of the hysteresis that is used for the frequency protection.
	»t«	Tripping delay
	»df/dt«	Measured value (calculated): Rate-of-frequency-change.
	»t-df/dt«	Trip delay df/dt
	»DF«	Frequency difference for the maximum admissible variation of the mean of the rate of frequency-change. This function is inactive if DF=0.
	»DT«	Time interval of the maximum admissible rate-of-frequency-change.
	»df/dt mode«	df/dt mode
	»delta phi«	Measured value (calculated): Vector surge

3.5.3.3.4 Protection Para / Set 1 ... 4 / f-Prot / f[4]

	»Function«	Permanent activation or deactivation of module/stage.
	»ExBlo Fc«	Activate (allow) or inactivate (disallow) blocking of the module/stage. This parameter is only effective if a signal is assigned to the corresponding global protection parameter. If the signal becomes true, those modules/stages are blocked that are parameterized "ExBlo Fc=active".
	»Blo TripCmd«	Permanent blocking of the Trip Command of the module/stage.
	»ExBlo TripCmd Fc«	Activate (allow) or inactivate (disallow) blocking of the module/stage. This parameter is only effective if a signal is assigned to the corresponding global protection parameter. If the signal becomes true, those modules/stages are blocked that are parameterized "ExBlo TripCmd Fc=active".
	»f>«	Pickup value for overfrequency.
	»f<«	Pickup value for underfrequency.
	»Freq. drop-off«	Drop-off for the Frequency function. This setting modifies the shape of the hysteresis that is used for the frequency protection.
	»t«	Tripping delay
	»df/dt«	Measured value (calculated): Rate-of-frequency-change.
	»t-df/dt«	Trip delay df/dt
	»DF«	Frequency difference for the maximum admissible variation of the mean of the rate of frequency-change. This function is inactive if DF=0.
	»DT«	Time interval of the maximum admissible rate-of-frequency-change.
	»df/dt mode«	df/dt mode
	»delta phi«	Measured value (calculated): Vector surge

3.5.3.3.5 Protection Para / Set 1 ... 4 / f-Prot / f[5]

	»Function«	Permanent activation or deactivation of module/stage.
	»ExBlo Fc«	Activate (allow) or inactivate (disallow) blocking of the module/stage. This parameter is only effective if a signal is assigned to the corresponding global protection parameter. If the signal becomes true, those modules/stages are blocked that are parameterized "ExBlo Fc=active".
	»Blo TripCmd«	Permanent blocking of the Trip Command of the module/stage.
	»ExBlo TripCmd Fc«	Activate (allow) or inactivate (disallow) blocking of the module/stage. This parameter is only effective if a signal is assigned to the corresponding global protection parameter. If the signal becomes true, those modules/stages are blocked that are parameterized "ExBlo TripCmd Fc=active".
	»f>«	Pickup value for overfrequency.
	»f<«	Pickup value for underfrequency.
	»Freq. drop-off«	Drop-off for the Frequency function. This setting modifies the shape of the hysteresis that is used for the frequency protection.
	»t«	Tripping delay
	»df/dt«	Measured value (calculated): Rate-of-frequency-change.
	»t-df/dt«	Trip delay df/dt
	»DF«	Frequency difference for the maximum admissible variation of the mean of the rate of frequency-change. This function is inactive if DF=0.
	»DT«	Time interval of the maximum admissible rate-of-frequency-change.
	»df/dt mode«	df/dt mode
	»delta phi«	Measured value (calculated): Vector surge

3.5.3.3.6 Protection Para / Set 1 ... 4 / f-Prot / f[6]

	»Function«	Permanent activation or deactivation of module/stage.
	»ExBlo Fc«	Activate (allow) or inactivate (disallow) blocking of the module/stage. This parameter is only effective if a signal is assigned to the corresponding global protection parameter. If the signal becomes true, those modules/stages are blocked that are parameterized "ExBlo Fc=active".
	»Blo TripCmd«	Permanent blocking of the Trip Command of the module/stage.
	»ExBlo TripCmd Fc«	Activate (allow) or inactivate (disallow) blocking of the module/stage. This parameter is only effective if a signal is assigned to the corresponding global protection parameter. If the signal becomes true, those modules/stages are blocked that are parameterized "ExBlo TripCmd Fc=active".
	»f>«	Pickup value for overfrequency.
	»f<«	Pickup value for underfrequency.
	»Freq. drop-off«	Drop-off for the Frequency function. This setting modifies the shape of the hysteresis that is used for the frequency protection.
	»t«	Tripping delay
	»df/dt«	Measured value (calculated): Rate-of-frequency-change.
	»t-df/dt«	Trip delay df/dt
	»DF«	Frequency difference for the maximum admissible variation of the mean of the rate of frequency-change. This function is inactive if DF=0.
	»DT«	Time interval of the maximum admissible rate-of-frequency-change.
	»df/dt mode«	df/dt mode
	»delta phi«	Measured value (calculated): Vector surge

3.5.3.4 Protection Para / Set 1 ... 4 / ExP

3.5.3.4.1 Protection Para / Set 1 ... 4 / ExP / ExP[1]

	»Function«	Permanent activation or deactivation of module/stage.
	»ExBlo Fc«	Activate (allow) or inactivate (disallow) blocking of the module/stage. This parameter is only effective if a signal is assigned to the corresponding global protection parameter. If the signal becomes true, those modules/stages are blocked that are parameterized "ExBlo Fc=active".
	»Blo TripCmd«	Permanent blocking of the Trip Command of the module/stage.
	»ExBlo TripCmd Fc«	Activate (allow) or inactivate (disallow) blocking of the module/stage. This parameter is only effective if a signal is assigned to the corresponding global protection parameter. If the signal becomes true, those modules/stages are blocked that are parameterized "ExBlo TripCmd Fc=active".

3.5.3.4.2 Protection Para / Set 1 ... 4 / ExP / ExP[2]

	»Function«	Permanent activation or deactivation of module/stage.
	»ExBlo Fc«	Activate (allow) or inactivate (disallow) blocking of the module/stage. This parameter is only effective if a signal is assigned to the corresponding global protection parameter. If the signal becomes true, those modules/stages are blocked that are parameterized "ExBlo Fc=active".
	»Blo TripCmd«	Permanent blocking of the Trip Command of the module/stage.
	»ExBlo TripCmd Fc«	Activate (allow) or inactivate (disallow) blocking of the module/stage. This parameter is only effective if a signal is assigned to the corresponding global protection parameter. If the signal becomes true, those modules/stages are blocked that are parameterized "ExBlo TripCmd Fc=active".

3.5.3.4.3 Protection Para / Set 1 ... 4 / ExP / ExP[3]

	»Function«	Permanent activation or deactivation of module/stage.
	»ExBlo Fc«	Activate (allow) or inactivate (disallow) blocking of the module/stage. This parameter is only effective if a signal is assigned to the corresponding global protection parameter. If the signal becomes true, those modules/stages are blocked that are parameterized "ExBlo Fc=active".
	»Blo TripCmd«	Permanent blocking of the Trip Command of the module/stage.
	»ExBlo TripCmd Fc«	Activate (allow) or inactivate (disallow) blocking of the module/stage. This parameter is only effective if a signal is assigned to the corresponding global protection parameter. If the signal becomes true, those modules/stages are blocked that are parameterized "ExBlo TripCmd Fc=active".

3.5.3.4.4 Protection Para / Set 1 ... 4 / ExP / ExP[4]

	»Function«	Permanent activation or deactivation of module/stage.
	»ExBlo Fc«	Activate (allow) or inactivate (disallow) blocking of the module/stage. This parameter is only effective if a signal is assigned to the corresponding global protection parameter. If the signal becomes true, those modules/stages are blocked that are parameterized "ExBlo Fc=active".
	»Blo TripCmd«	Permanent blocking of the Trip Command of the module/stage.
	»ExBlo TripCmd Fc«	Activate (allow) or inactivate (disallow) blocking of the module/stage. This parameter is only effective if a signal is assigned to the corresponding global protection parameter. If the signal becomes true, those modules/stages are blocked that are parameterized "ExBlo TripCmd Fc=active".

3.5.3.5 Protection Para / Set 1 … 4 / Supervision

3.5.3.5.1 Protection Para / Set 1 … 4 / Supervision / CBF

	»Function«	Permanent activation or deactivation of module/stage.
	»ExBlo Fc«	Activate (allow) or inactivate (disallow) blocking of the module/stage. This parameter is only effective if a signal is assigned to the corresponding global protection parameter. If the signal becomes true, those modules/stages are blocked that are parameterized "ExBlo Fc=active".
	»t-CBF«	If the delay time is expired, a CBF alarm is issued.

3.5.3.5.2 Protection Para / Set 1 … 4 / Supervision / TCS

	»Function«	Permanent activation or deactivation of module/stage.
	»ExBlo Fc«	Activate (allow) or inactivate (disallow) blocking of the module/stage. This parameter is only effective if a signal is assigned to the corresponding global protection parameter. If the signal becomes true, those modules/stages are blocked that are parameterized "ExBlo Fc=active".
	»t-TCS«	Delay time of the Trip Circuit Supervision

3.5.3.5.3 Protection Para / Set 1 … 4 / Supervision / VTS

	»Function«	Permanent activation or deactivation of module/stage.
	»ExBlo Fc«	Activate (allow) or inactivate (disallow) blocking of the module/stage. This parameter is only effective if a signal is assigned to the corresponding global protection parameter. If the signal becomes true, those modules/stages are blocked that are parameterized "ExBlo Fc=active".
	»ΔV«	In order to prevent faulty tripping of phase selective protection functions that use the voltage as tripping criterion. If the difference of the residual voltage and the calculated value V0 is higher than the pick up value ΔV, an alarm event effected after the excitation time. In such a case, the existence of a fuse failure, a broken wire or a faulty measuring circuit can be assumed.
	»Alarm delay«	Alarm delay

3.6 SysA

3.6.1 SysA / General Settings

	»Function«	Permanent activation or deactivation of module/stage.
	»ExBlo Fc«	Activate (allow) or inactivate (disallow) blocking of the module/stage. This parameter is only effective if a signal is assigned to the corresponding global protection parameter. If the signal becomes true, those modules/stages are blocked that are parameterized "ExBlo Fc=active".

3.6.2 SysA / THD

3.6.2.1 SysA / THD / V THD

	»Alarm«	Alarm
	»Threshold«	Threshold (to be entered as primary value)
	»t-Delay«	Tripping Delay

3.7 Control

	»Control Page«	Control Page

3.7.1 Control / General Settings

	»Switching Authority«	Switching Authority
	»NonInterl«	DC for Non-Interlocking
	»Res NonIL«	Resetmode Non-Interlocking
	»Timeout NonIL«	Timeout Non-Interlocking
	»NonIL Assign«	Assignment Non-Interlocking

3.7.2 Control / SG

3.7.2.1 Control / SG / SG[1]

3.7.2.1.1 Control / SG / SG[1] / General Settings

	»ON incl Prot ON«	The ON Command includes the ON Command issued by the Protection module.
	»OFF incl TripCmd«	The OFF Command includes the OFF Command issued by the Protection module.
	»t-Move ON«	Time to move to the ON Position
	»t-Move OFF«	Time to move to the OFF Position
	»t-Dwell«	Dwell time
	»Manipulate Position«	WARNING! Fake Position - Manual Position Manipulation

3.7.2.1.2 Control / SG / SG[1] / Trip Manager

	»t-TripCmd«	Minimum hold time of the OFF-command (circuit breaker, load break switch)
	»Latched«	Defines whether the Trip Command is latched.
	»Ack TripCmd«	Ack TripCmd

	»Off Cmd1« ... »Off Cmd30«	Off Command to the Circuit Breaker if the state of the assigned signal becomes true.

3.7.2.1.3 Control / SG / SG[1] / Pos Indicatrs Wirng

	»Aux ON«	The CB is in ON-position if the state of the assigned signal is true (52a).
	»Aux OFF«	The CB is in OFF-position if the state of the assigned signal is true (52b).
	»Ready«	Circuit breaker is ready for operation if the state of the assigned signal is true. This digital input can be used by some protective elements (if they are available within the device) like Auto Reclosure (AR), e.g. as a trigger signal.
	»Removed«	The withdrawable circuit breaker is Removed

3.7.2.1.4 Control / SG / SG[1] / Ex ON/OFF Cmd

	»SCmd ON«	Switching ON Command, e.g. the state of the Logics or the state of the digital input
	»SCmd OFF«	Switching OFF Command, e.g. the state of the Logics or the state of the digital input

3.7.2.1.5 Control / SG / SG[1] / Interlockings

	»Interl ON1«	Interlocking of the ON command
	»Interl ON2«	Interlocking of the ON command
	»Interl ON3«	Interlocking of the ON command
	»Interl OFF1«	Interlocking of the OFF command
	»Interl OFF2«	Interlocking of the OFF command
	»Interl OFF3«	Interlocking of the OFF command

3.7.2.1.6 Control / SG / SG[1] / Synchron Switchg

	»Synchronism«	Synchronism
	»t-MaxSyncSuperv«	Synchron-Run timer: Max. time allowed for synchronizing process after a close initiate. Only used for GENERATOR2SYSTEM working mode.

3.7.2.1.7 Control / SG / SG[1] / SG Wear

	»Operations Alarm«	Maximum number of operations. If the operations counter »TripCmd Cr« exceeds this limit then the signal »Operations Alarm« is set.

3.8 Logics

3.8.1 Logics / LE 1

	»LE1.Gate«	Logic gate
	»LE1.Input1«	Assignment of the Input Signal
	»LE1.Inverting1«	Inverting the input signals.
	»LE1.Input2«	Assignment of the Input Signal
	»LE1.Inverting2«	Inverting the input signals.
	»LE1.Input3«	Assignment of the Input Signal
	»LE1.Inverting3«	Inverting the input signals.
	»LE1.Input4«	Assignment of the Input Signal
	»LE1.Inverting4«	Inverting the input signals.
	»LE1.t-On Delay«	Switch On Delay
	»LE1.t-Off Delay«	Switch Off Delay
	»LE1.Reset Latched«	Reset Signal for the Latching
	»LE1.Inverting Reset«	Inverting Reset Signal for the Latching
	»LE1.Inverting Set«	Inverting the Setting Signal for the Latching

3.8.2 Logics / LE 2

	»LE2.Gate«	Logic gate
	»LE2.Input1«	Assignment of the Input Signal
	»LE2.Inverting1«	Inverting the input signals.
	»LE2.Input2«	Assignment of the Input Signal
	»LE2.Inverting2«	Inverting the input signals.
	»LE2.Input3«	Assignment of the Input Signal
	»LE2.Inverting3«	Inverting the input signals.
	»LE2.Input4«	Assignment of the Input Signal
	»LE2.Inverting4«	Inverting the input signals.
	»LE2.t-On Delay«	Switch On Delay
	»LE2.t-Off Delay«	Switch Off Delay
	»LE2.Reset Latched«	Reset Signal for the Latching
	»LE2.Inverting Reset«	Inverting Reset Signal for the Latching
	»LE2.Inverting Set«	Inverting the Setting Signal for the Latching

3.8.3 Logics / LE 3

	»LE3.Gate«	Logic gate
	»LE3.Input1«	Assignment of the Input Signal
	»LE3.Inverting1«	Inverting the input signals.
	»LE3.Input2«	Assignment of the Input Signal
	»LE3.Inverting2«	Inverting the input signals.
	»LE3.Input3«	Assignment of the Input Signal
	»LE3.Inverting3«	Inverting the input signals.
	»LE3.Input4«	Assignment of the Input Signal
	»LE3.Inverting4«	Inverting the input signals.
	»LE3.t-On Delay«	Switch On Delay
	»LE3.t-Off Delay«	Switch Off Delay
	»LE3.Reset Latched«	Reset Signal for the Latching
	»LE3.Inverting Reset«	Inverting Reset Signal for the Latching
	»LE3.Inverting Set«	Inverting the Setting Signal for the Latching

3.8.4 Logics / LE 4

	»LE4.Gate«	Logic gate
	»LE4.Input1«	Assignment of the Input Signal
	»LE4.Inverting1«	Inverting the input signals.
	»LE4.Input2«	Assignment of the Input Signal
	»LE4.Inverting2«	Inverting the input signals.
	»LE4.Input3«	Assignment of the Input Signal
	»LE4.Inverting3«	Inverting the input signals.
	»LE4.Input4«	Assignment of the Input Signal
	»LE4.Inverting4«	Inverting the input signals.
	»LE4.t-On Delay«	Switch On Delay
	»LE4.t-Off Delay«	Switch Off Delay
	»LE4.Reset Latched«	Reset Signal for the Latching
	»LE4.Inverting Reset«	Inverting Reset Signal for the Latching
	»LE4.Inverting Set«	Inverting the Setting Signal for the Latching

3.8.5 Logics / LE 5

	»LE5.Gate«	Logic gate
	»LE5.Input1«	Assignment of the Input Signal
	»LE5.Inverting1«	Inverting the input signals.
	»LE5.Input2«	Assignment of the Input Signal
	»LE5.Inverting2«	Inverting the input signals.
	»LE5.Input3«	Assignment of the Input Signal
	»LE5.Inverting3«	Inverting the input signals.
	»LE5.Input4«	Assignment of the Input Signal
	»LE5.Inverting4«	Inverting the input signals.
	»LE5.t-On Delay«	Switch On Delay
	»LE5.t-Off Delay«	Switch Off Delay
	»LE5.Reset Latched«	Reset Signal for the Latching
	»LE5.Inverting Reset«	Inverting Reset Signal for the Latching
	»LE5.Inverting Set«	Inverting the Setting Signal for the Latching

3.8.6 Logics / LE 6

	»LE6.Gate«	Logic gate
	»LE6.Input1«	Assignment of the Input Signal
	»LE6.Inverting1«	Inverting the input signals.
	»LE6.Input2«	Assignment of the Input Signal
	»LE6.Inverting2«	Inverting the input signals.
	»LE6.Input3«	Assignment of the Input Signal
	»LE6.Inverting3«	Inverting the input signals.
	»LE6.Input4«	Assignment of the Input Signal
	»LE6.Inverting4«	Inverting the input signals.
	»LE6.t-On Delay«	Switch On Delay
	»LE6.t-Off Delay«	Switch Off Delay
	»LE6.Reset Latched«	Reset Signal for the Latching
	»LE6.Inverting Reset«	Inverting Reset Signal for the Latching
	»LE6.Inverting Set«	Inverting the Setting Signal for the Latching

3.8.7 Logics / LE 7

	»LE7.Gate«	Logic gate
	»LE7.Input1«	Assignment of the Input Signal
	»LE7.Inverting1«	Inverting the input signals.
	»LE7.Input2«	Assignment of the Input Signal
	»LE7.Inverting2«	Inverting the input signals.
	»LE7.Input3«	Assignment of the Input Signal
	»LE7.Inverting3«	Inverting the input signals.
	»LE7.Input4«	Assignment of the Input Signal
	»LE7.Inverting4«	Inverting the input signals.
	»LE7.t-On Delay«	Switch On Delay
	»LE7.t-Off Delay«	Switch Off Delay
	»LE7.Reset Latched«	Reset Signal for the Latching
	»LE7.Inverting Reset«	Inverting Reset Signal for the Latching
	»LE7.Inverting Set«	Inverting the Setting Signal for the Latching

3.8.8 Logics / LE 8

	»LE8.Gate«	Logic gate
	»LE8.Input1«	Assignment of the Input Signal
	»LE8.Inverting1«	Inverting the input signals.
	»LE8.Input2«	Assignment of the Input Signal
	»LE8.Inverting2«	Inverting the input signals.
	»LE8.Input3«	Assignment of the Input Signal
	»LE8.Inverting3«	Inverting the input signals.
	»LE8.Input4«	Assignment of the Input Signal
	»LE8.Inverting4«	Inverting the input signals.
	»LE8.t-On Delay«	Switch On Delay
	»LE8.t-Off Delay«	Switch Off Delay
	»LE8.Reset Latched«	Reset Signal for the Latching
	»LE8.Inverting Reset«	Inverting Reset Signal for the Latching
	»LE8.Inverting Set«	Inverting the Setting Signal for the Latching

3.8.9 Logics / LE 9

	»LE9.Gate«	Logic gate
	»LE9.Input1«	Assignment of the Input Signal
	»LE9.Inverting1«	Inverting the input signals.
	»LE9.Input2«	Assignment of the Input Signal
	»LE9.Inverting2«	Inverting the input signals.
	»LE9.Input3«	Assignment of the Input Signal
	»LE9.Inverting3«	Inverting the input signals.
	»LE9.Input4«	Assignment of the Input Signal
	»LE9.Inverting4«	Inverting the input signals.
	»LE9.t-On Delay«	Switch On Delay
	»LE9.t-Off Delay«	Switch Off Delay
	»LE9.Reset Latched«	Reset Signal for the Latching
	»LE9.Inverting Reset«	Inverting Reset Signal for the Latching
	»LE9.Inverting Set«	Inverting the Setting Signal for the Latching

3.8.10 Logics / LE 10

	»LE10.Gate«	Logic gate
	»LE10.Input1«	Assignment of the Input Signal
	»LE10.Inverting1«	Inverting the input signals.
	»LE10.Input2«	Assignment of the Input Signal
	»LE10.Inverting2«	Inverting the input signals.
	»LE10.Input3«	Assignment of the Input Signal
	»LE10.Inverting3«	Inverting the input signals.
	»LE10.Input4«	Assignment of the Input Signal
	»LE10.Inverting4«	Inverting the input signals.
	»LE10.t-On Delay«	Switch On Delay
	»LE10.t-Off Delay«	Switch Off Delay
	»LE10.Reset Latched«	Reset Signal for the Latching
	»LE10.Inverting Reset«	Inverting Reset Signal for the Latching
	»LE10.Inverting Set«	Inverting the Setting Signal for the Latching

3.8.11 Logics / LE 11

	»LE11.Gate«	Logic gate
	»LE11.Input1«	Assignment of the Input Signal
	»LE11.Inverting1«	Inverting the input signals.
	»LE11.Input2«	Assignment of the Input Signal
	»LE11.Inverting2«	Inverting the input signals.
	»LE11.Input3«	Assignment of the Input Signal
	»LE11.Inverting3«	Inverting the input signals.
	»LE11.Input4«	Assignment of the Input Signal
	»LE11.Inverting4«	Inverting the input signals.
	»LE11.t-On Delay«	Switch On Delay
	»LE11.t-Off Delay«	Switch Off Delay
	»LE11.Reset Latched«	Reset Signal for the Latching
	»LE11.Inverting Reset«	Inverting Reset Signal for the Latching
	»LE11.Inverting Set«	Inverting the Setting Signal for the Latching

3.8.12 Logics / LE 12

	»LE12.Gate«	Logic gate
	»LE12.Input1«	Assignment of the Input Signal
	»LE12.Inverting1«	Inverting the input signals.
	»LE12.Input2«	Assignment of the Input Signal
	»LE12.Inverting2«	Inverting the input signals.
	»LE12.Input3«	Assignment of the Input Signal
	»LE12.Inverting3«	Inverting the input signals.
	»LE12.Input4«	Assignment of the Input Signal
	»LE12.Inverting4«	Inverting the input signals.
	»LE12.t-On Delay«	Switch On Delay
	»LE12.t-Off Delay«	Switch Off Delay
	»LE12.Reset Latched«	Reset Signal for the Latching
	»LE12.Inverting Reset«	Inverting Reset Signal for the Latching
	»LE12.Inverting Set«	Inverting the Setting Signal for the Latching

3.8.13 Logics / LE 13

	»LE13.Gate«	Logic gate
	»LE13.Input1«	Assignment of the Input Signal
	»LE13.Inverting1«	Inverting the input signals.
	»LE13.Input2«	Assignment of the Input Signal
	»LE13.Inverting2«	Inverting the input signals.
	»LE13.Input3«	Assignment of the Input Signal
	»LE13.Inverting3«	Inverting the input signals.
	»LE13.Input4«	Assignment of the Input Signal
	»LE13.Inverting4«	Inverting the input signals.
	»LE13.t-On Delay«	Switch On Delay
	»LE13.t-Off Delay«	Switch Off Delay
	»LE13.Reset Latched«	Reset Signal for the Latching
	»LE13.Inverting Reset«	Inverting Reset Signal for the Latching
	»LE13.Inverting Set«	Inverting the Setting Signal for the Latching

3.8.14 Logics / LE 14

	»LE14.Gate«	Logic gate
	»LE14.Input1«	Assignment of the Input Signal
	»LE14.Inverting1«	Inverting the input signals.
	»LE14.Input2«	Assignment of the Input Signal
	»LE14.Inverting2«	Inverting the input signals.
	»LE14.Input3«	Assignment of the Input Signal
	»LE14.Inverting3«	Inverting the input signals.
	»LE14.Input4«	Assignment of the Input Signal
	»LE14.Inverting4«	Inverting the input signals.
	»LE14.t-On Delay«	Switch On Delay
	»LE14.t-Off Delay«	Switch Off Delay
	»LE14.Reset Latched«	Reset Signal for the Latching
	»LE14.Inverting Reset«	Inverting Reset Signal for the Latching
	»LE14.Inverting Set«	Inverting the Setting Signal for the Latching

3.8.15 Logics / LE 15

	»LE15.Gate«	Logic gate
	»LE15.Input1«	Assignment of the Input Signal
	»LE15.Inverting1«	Inverting the input signals.
	»LE15.Input2«	Assignment of the Input Signal
	»LE15.Inverting2«	Inverting the input signals.
	»LE15.Input3«	Assignment of the Input Signal
	»LE15.Inverting3«	Inverting the input signals.
	»LE15.Input4«	Assignment of the Input Signal
	»LE15.Inverting4«	Inverting the input signals.
	»LE15.t-On Delay«	Switch On Delay
	»LE15.t-Off Delay«	Switch Off Delay
	»LE15.Reset Latched«	Reset Signal for the Latching
	»LE15.Inverting Reset«	Inverting Reset Signal for the Latching
	»LE15.Inverting Set«	Inverting the Setting Signal for the Latching

3.8.16 Logics / LE 16

	»LE16.Gate«	Logic gate
	»LE16.Input1«	Assignment of the Input Signal
	»LE16.Inverting1«	Inverting the input signals.
	»LE16.Input2«	Assignment of the Input Signal
	»LE16.Inverting2«	Inverting the input signals.
	»LE16.Input3«	Assignment of the Input Signal
	»LE16.Inverting3«	Inverting the input signals.
	»LE16.Input4«	Assignment of the Input Signal
	»LE16.Inverting4«	Inverting the input signals.
	»LE16.t-On Delay«	Switch On Delay
	»LE16.t-Off Delay«	Switch Off Delay
	»LE16.Reset Latched«	Reset Signal for the Latching
	»LE16.Inverting Reset«	Inverting Reset Signal for the Latching
	»LE16.Inverting Set«	Inverting the Setting Signal for the Latching

3.8.17 Logics / LE 17

	»LE17.Gate«	Logic gate
	»LE17.Input1«	Assignment of the Input Signal
	»LE17.Inverting1«	Inverting the input signals.
	»LE17.Input2«	Assignment of the Input Signal
	»LE17.Inverting2«	Inverting the input signals.
	»LE17.Input3«	Assignment of the Input Signal
	»LE17.Inverting3«	Inverting the input signals.
	»LE17.Input4«	Assignment of the Input Signal
	»LE17.Inverting4«	Inverting the input signals.
	»LE17.t-On Delay«	Switch On Delay
	»LE17.t-Off Delay«	Switch Off Delay
	»LE17.Reset Latched«	Reset Signal for the Latching
	»LE17.Inverting Reset«	Inverting Reset Signal for the Latching
	»LE17.Inverting Set«	Inverting the Setting Signal for the Latching

3.8.18 Logics / LE 18

	»LE18.Gate«	Logic gate
	»LE18.Input1«	Assignment of the Input Signal
	»LE18.Inverting1«	Inverting the input signals.
	»LE18.Input2«	Assignment of the Input Signal
	»LE18.Inverting2«	Inverting the input signals.
	»LE18.Input3«	Assignment of the Input Signal
	»LE18.Inverting3«	Inverting the input signals.
	»LE18.Input4«	Assignment of the Input Signal
	»LE18.Inverting4«	Inverting the input signals.
	»LE18.t-On Delay«	Switch On Delay
	»LE18.t-Off Delay«	Switch Off Delay
	»LE18.Reset Latched«	Reset Signal for the Latching
	»LE18.Inverting Reset«	Inverting Reset Signal for the Latching
	»LE18.Inverting Set«	Inverting the Setting Signal for the Latching

3.8.19 Logics / LE 19

	»LE19.Gate«	Logic gate
	»LE19.Input1«	Assignment of the Input Signal
	»LE19.Inverting1«	Inverting the input signals.
	»LE19.Input2«	Assignment of the Input Signal
	»LE19.Inverting2«	Inverting the input signals.
	»LE19.Input3«	Assignment of the Input Signal
	»LE19.Inverting3«	Inverting the input signals.
	»LE19.Input4«	Assignment of the Input Signal
	»LE19.Inverting4«	Inverting the input signals.
	»LE19.t-On Delay«	Switch On Delay
	»LE19.t-Off Delay«	Switch Off Delay
	»LE19.Reset Latched«	Reset Signal for the Latching
	»LE19.Inverting Reset«	Inverting Reset Signal for the Latching
	»LE19.Inverting Set«	Inverting the Setting Signal for the Latching

3.8.20 Logics / LE 20

	»LE20.Gate«	Logic gate
	»LE20.Input1«	Assignment of the Input Signal
	»LE20.Inverting1«	Inverting the input signals.
	»LE20.Input2«	Assignment of the Input Signal
	»LE20.Inverting2«	Inverting the input signals.
	»LE20.Input3«	Assignment of the Input Signal
	»LE20.Inverting3«	Inverting the input signals.
	»LE20.Input4«	Assignment of the Input Signal
	»LE20.Inverting4«	Inverting the input signals.
	»LE20.t-On Delay«	Switch On Delay
	»LE20.t-Off Delay«	Switch Off Delay
	»LE20.Reset Latched«	Reset Signal for the Latching
	»LE20.Inverting Reset«	Inverting Reset Signal for the Latching
	»LE20.Inverting Set«	Inverting the Setting Signal for the Latching

3.8.21 Logics / LE 21

	»LE21.Gate«	Logic gate
	»LE21.Input1«	Assignment of the Input Signal
	»LE21.Inverting1«	Inverting the input signals.
	»LE21.Input2«	Assignment of the Input Signal
	»LE21.Inverting2«	Inverting the input signals.
	»LE21.Input3«	Assignment of the Input Signal
	»LE21.Inverting3«	Inverting the input signals.
	»LE21.Input4«	Assignment of the Input Signal
	»LE21.Inverting4«	Inverting the input signals.
	»LE21.t-On Delay«	Switch On Delay
	»LE21.t-Off Delay«	Switch Off Delay
	»LE21.Reset Latched«	Reset Signal for the Latching
	»LE21.Inverting Reset«	Inverting Reset Signal for the Latching
	»LE21.Inverting Set«	Inverting the Setting Signal for the Latching

3.8.22 Logics / LE 22

	»LE22.Gate«	Logic gate
	»LE22.Input1«	Assignment of the Input Signal
	»LE22.Inverting1«	Inverting the input signals.
	»LE22.Input2«	Assignment of the Input Signal
	»LE22.Inverting2«	Inverting the input signals.
	»LE22.Input3«	Assignment of the Input Signal
	»LE22.Inverting3«	Inverting the input signals.
	»LE22.Input4«	Assignment of the Input Signal
	»LE22.Inverting4«	Inverting the input signals.
	»LE22.t-On Delay«	Switch On Delay
	»LE22.t-Off Delay«	Switch Off Delay
	»LE22.Reset Latched«	Reset Signal for the Latching
	»LE22.Inverting Reset«	Inverting Reset Signal for the Latching
	»LE22.Inverting Set«	Inverting the Setting Signal for the Latching

3.8.23 Logics / LE 23

	»LE23.Gate«	Logic gate
	»LE23.Input1«	Assignment of the Input Signal
	»LE23.Inverting1«	Inverting the input signals.
	»LE23.Input2«	Assignment of the Input Signal
	»LE23.Inverting2«	Inverting the input signals.
	»LE23.Input3«	Assignment of the Input Signal
	»LE23.Inverting3«	Inverting the input signals.
	»LE23.Input4«	Assignment of the Input Signal
	»LE23.Inverting4«	Inverting the input signals.
	»LE23.t-On Delay«	Switch On Delay
	»LE23.t-Off Delay«	Switch Off Delay
	»LE23.Reset Latched«	Reset Signal for the Latching
	»LE23.Inverting Reset«	Inverting Reset Signal for the Latching
	»LE23.Inverting Set«	Inverting the Setting Signal for the Latching

3.8.24 Logics / LE 24

	»LE24.Gate«	Logic gate
	»LE24.Input1«	Assignment of the Input Signal
	»LE24.Inverting1«	Inverting the input signals.
	»LE24.Input2«	Assignment of the Input Signal
	»LE24.Inverting2«	Inverting the input signals.
	»LE24.Input3«	Assignment of the Input Signal
	»LE24.Inverting3«	Inverting the input signals.
	»LE24.Input4«	Assignment of the Input Signal
	»LE24.Inverting4«	Inverting the input signals.
	»LE24.t-On Delay«	Switch On Delay
	»LE24.t-Off Delay«	Switch Off Delay
	»LE24.Reset Latched«	Reset Signal for the Latching
	»LE24.Inverting Reset«	Inverting Reset Signal for the Latching
	»LE24.Inverting Set«	Inverting the Setting Signal for the Latching

3.8.25 Logics / LE 25

	»LE25.Gate«	Logic gate
	»LE25.Input1«	Assignment of the Input Signal
	»LE25.Inverting1«	Inverting the input signals.
	»LE25.Input2«	Assignment of the Input Signal
	»LE25.Inverting2«	Inverting the input signals.
	»LE25.Input3«	Assignment of the Input Signal
	»LE25.Inverting3«	Inverting the input signals.
	»LE25.Input4«	Assignment of the Input Signal
	»LE25.Inverting4«	Inverting the input signals.
	»LE25.t-On Delay«	Switch On Delay
	»LE25.t-Off Delay«	Switch Off Delay
	»LE25.Reset Latched«	Reset Signal for the Latching
	»LE25.Inverting Reset«	Inverting Reset Signal for the Latching
	»LE25.Inverting Set«	Inverting the Setting Signal for the Latching

3.8.26 Logics / LE 26

	»LE26.Gate«	Logic gate
	»LE26.Input1«	Assignment of the Input Signal
	»LE26.Inverting1«	Inverting the input signals.
	»LE26.Input2«	Assignment of the Input Signal
	»LE26.Inverting2«	Inverting the input signals.
	»LE26.Input3«	Assignment of the Input Signal
	»LE26.Inverting3«	Inverting the input signals.
	»LE26.Input4«	Assignment of the Input Signal
	»LE26.Inverting4«	Inverting the input signals.
	»LE26.t-On Delay«	Switch On Delay
	»LE26.t-Off Delay«	Switch Off Delay
	»LE26.Reset Latched«	Reset Signal for the Latching
	»LE26.Inverting Reset«	Inverting Reset Signal for the Latching
	»LE26.Inverting Set«	Inverting the Setting Signal for the Latching

3.8.27 Logics / LE 27

	»LE27.Gate«	Logic gate
	»LE27.Input1«	Assignment of the Input Signal
	»LE27.Inverting1«	Inverting the input signals.
	»LE27.Input2«	Assignment of the Input Signal
	»LE27.Inverting2«	Inverting the input signals.
	»LE27.Input3«	Assignment of the Input Signal
	»LE27.Inverting3«	Inverting the input signals.
	»LE27.Input4«	Assignment of the Input Signal
	»LE27.Inverting4«	Inverting the input signals.
	»LE27.t-On Delay«	Switch On Delay
	»LE27.t-Off Delay«	Switch Off Delay
	»LE27.Reset Latched«	Reset Signal for the Latching
	»LE27.Inverting Reset«	Inverting Reset Signal for the Latching
	»LE27.Inverting Set«	Inverting the Setting Signal for the Latching

3.8.28 Logics / LE 28

	»LE28.Gate«	Logic gate
	»LE28.Input1«	Assignment of the Input Signal
	»LE28.Inverting1«	Inverting the input signals.
	»LE28.Input2«	Assignment of the Input Signal
	»LE28.Inverting2«	Inverting the input signals.
	»LE28.Input3«	Assignment of the Input Signal
	»LE28.Inverting3«	Inverting the input signals.
	»LE28.Input4«	Assignment of the Input Signal
	»LE28.Inverting4«	Inverting the input signals.
	»LE28.t-On Delay«	Switch On Delay
	»LE28.t-Off Delay«	Switch Off Delay
	»LE28.Reset Latched«	Reset Signal for the Latching
	»LE28.Inverting Reset«	Inverting Reset Signal for the Latching
	»LE28.Inverting Set«	Inverting the Setting Signal for the Latching

3.8.29 Logics / LE 29

	»LE29.Gate«	Logic gate
	»LE29.Input1«	Assignment of the Input Signal
	»LE29.Inverting1«	Inverting the input signals.
	»LE29.Input2«	Assignment of the Input Signal
	»LE29.Inverting2«	Inverting the input signals.
	»LE29.Input3«	Assignment of the Input Signal
	»LE29.Inverting3«	Inverting the input signals.
	»LE29.Input4«	Assignment of the Input Signal
	»LE29.Inverting4«	Inverting the input signals.
	»LE29.t-On Delay«	Switch On Delay
	»LE29.t-Off Delay«	Switch Off Delay
	»LE29.Reset Latched«	Reset Signal for the Latching
	»LE29.Inverting Reset«	Inverting Reset Signal for the Latching
	»LE29.Inverting Set«	Inverting the Setting Signal for the Latching

3.8.30 Logics / LE 30

	»LE30.Gate«	Logic gate
	»LE30.Input1«	Assignment of the Input Signal
	»LE30.Inverting1«	Inverting the input signals.
	»LE30.Input2«	Assignment of the Input Signal
	»LE30.Inverting2«	Inverting the input signals.
	»LE30.Input3«	Assignment of the Input Signal
	»LE30.Inverting3«	Inverting the input signals.
	»LE30.Input4«	Assignment of the Input Signal
	»LE30.Inverting4«	Inverting the input signals.
	»LE30.t-On Delay«	Switch On Delay
	»LE30.t-Off Delay«	Switch Off Delay
	»LE30.Reset Latched«	Reset Signal for the Latching
	»LE30.Inverting Reset«	Inverting Reset Signal for the Latching
	»LE30.Inverting Set«	Inverting the Setting Signal for the Latching

3.8.31 Logics / LE 31

	»LE31.Gate«	Logic gate
	»LE31.Input1«	Assignment of the Input Signal
	»LE31.Inverting1«	Inverting the input signals.
	»LE31.Input2«	Assignment of the Input Signal
	»LE31.Inverting2«	Inverting the input signals.
	»LE31.Input3«	Assignment of the Input Signal
	»LE31.Inverting3«	Inverting the input signals.
	»LE31.Input4«	Assignment of the Input Signal
	»LE31.Inverting4«	Inverting the input signals.
	»LE31.t-On Delay«	Switch On Delay
	»LE31.t-Off Delay«	Switch Off Delay
	»LE31.Reset Latched«	Reset Signal for the Latching
	»LE31.Inverting Reset«	Inverting Reset Signal for the Latching
	»LE31.Inverting Set«	Inverting the Setting Signal for the Latching

3.8.32 Logics / LE 32

	»LE32.Gate«	Logic gate
	»LE32.Input1«	Assignment of the Input Signal
	»LE32.Inverting1«	Inverting the input signals.
	»LE32.Input2«	Assignment of the Input Signal
	»LE32.Inverting2«	Inverting the input signals.
	»LE32.Input3«	Assignment of the Input Signal
	»LE32.Inverting3«	Inverting the input signals.
	»LE32.Input4«	Assignment of the Input Signal
	»LE32.Inverting4«	Inverting the input signals.
	»LE32.t-On Delay«	Switch On Delay
	»LE32.t-Off Delay«	Switch Off Delay
	»LE32.Reset Latched«	Reset Signal for the Latching
	»LE32.Inverting Reset«	Inverting Reset Signal for the Latching
	»LE32.Inverting Set«	Inverting the Setting Signal for the Latching

3.8.33 Logics / LE 33

	»LE33.Gate«	Logic gate
	»LE33.Input1«	Assignment of the Input Signal
	»LE33.Inverting1«	Inverting the input signals.
	»LE33.Input2«	Assignment of the Input Signal
	»LE33.Inverting2«	Inverting the input signals.
	»LE33.Input3«	Assignment of the Input Signal
	»LE33.Inverting3«	Inverting the input signals.
	»LE33.Input4«	Assignment of the Input Signal
	»LE33.Inverting4«	Inverting the input signals.
	»LE33.t-On Delay«	Switch On Delay
	»LE33.t-Off Delay«	Switch Off Delay
	»LE33.Reset Latched«	Reset Signal for the Latching
	»LE33.Inverting Reset«	Inverting Reset Signal for the Latching
	»LE33.Inverting Set«	Inverting the Setting Signal for the Latching

3.8.34 Logics / LE 34

	»LE34.Gate«	Logic gate
	»LE34.Input1«	Assignment of the Input Signal
	»LE34.Inverting1«	Inverting the input signals.
	»LE34.Input2«	Assignment of the Input Signal
	»LE34.Inverting2«	Inverting the input signals.
	»LE34.Input3«	Assignment of the Input Signal
	»LE34.Inverting3«	Inverting the input signals.
	»LE34.Input4«	Assignment of the Input Signal
	»LE34.Inverting4«	Inverting the input signals.
	»LE34.t-On Delay«	Switch On Delay
	»LE34.t-Off Delay«	Switch Off Delay
	»LE34.Reset Latched«	Reset Signal for the Latching
	»LE34.Inverting Reset«	Inverting Reset Signal for the Latching
	»LE34.Inverting Set«	Inverting the Setting Signal for the Latching

3.8.35 Logics / LE 35

	»LE35.Gate«	Logic gate
	»LE35.Input1«	Assignment of the Input Signal
	»LE35.Inverting1«	Inverting the input signals.
	»LE35.Input2«	Assignment of the Input Signal
	»LE35.Inverting2«	Inverting the input signals.
	»LE35.Input3«	Assignment of the Input Signal
	»LE35.Inverting3«	Inverting the input signals.
	»LE35.Input4«	Assignment of the Input Signal
	»LE35.Inverting4«	Inverting the input signals.
	»LE35.t-On Delay«	Switch On Delay
	»LE35.t-Off Delay«	Switch Off Delay
	»LE35.Reset Latched«	Reset Signal for the Latching
	»LE35.Inverting Reset«	Inverting Reset Signal for the Latching
	»LE35.Inverting Set«	Inverting the Setting Signal for the Latching

3.8.36 Logics / LE 36

	»LE36.Gate«	Logic gate
	»LE36.Input1«	Assignment of the Input Signal
	»LE36.Inverting1«	Inverting the input signals.
	»LE36.Input2«	Assignment of the Input Signal
	»LE36.Inverting2«	Inverting the input signals.
	»LE36.Input3«	Assignment of the Input Signal
	»LE36.Inverting3«	Inverting the input signals.
	»LE36.Input4«	Assignment of the Input Signal
	»LE36.Inverting4«	Inverting the input signals.
	»LE36.t-On Delay«	Switch On Delay
	»LE36.t-Off Delay«	Switch Off Delay
	»LE36.Reset Latched«	Reset Signal for the Latching
	»LE36.Inverting Reset«	Inverting Reset Signal for the Latching
	»LE36.Inverting Set«	Inverting the Setting Signal for the Latching

3.8.37 Logics / LE 37

	»LE37.Gate«	Logic gate
	»LE37.Input1«	Assignment of the Input Signal
	»LE37.Inverting1«	Inverting the input signals.
	»LE37.Input2«	Assignment of the Input Signal
	»LE37.Inverting2«	Inverting the input signals.
	»LE37.Input3«	Assignment of the Input Signal
	»LE37.Inverting3«	Inverting the input signals.
	»LE37.Input4«	Assignment of the Input Signal
	»LE37.Inverting4«	Inverting the input signals.
	»LE37.t-On Delay«	Switch On Delay
	»LE37.t-Off Delay«	Switch Off Delay
	»LE37.Reset Latched«	Reset Signal for the Latching
	»LE37.Inverting Reset«	Inverting Reset Signal for the Latching
	»LE37.Inverting Set«	Inverting the Setting Signal for the Latching

3.8.38 Logics / LE 38

	»LE38.Gate«	Logic gate
	»LE38.Input1«	Assignment of the Input Signal
	»LE38.Inverting1«	Inverting the input signals.
	»LE38.Input2«	Assignment of the Input Signal
	»LE38.Inverting2«	Inverting the input signals.
	»LE38.Input3«	Assignment of the Input Signal
	»LE38.Inverting3«	Inverting the input signals.
	»LE38.Input4«	Assignment of the Input Signal
	»LE38.Inverting4«	Inverting the input signals.
	»LE38.t-On Delay«	Switch On Delay
	»LE38.t-Off Delay«	Switch Off Delay
	»LE38.Reset Latched«	Reset Signal for the Latching
	»LE38.Inverting Reset«	Inverting Reset Signal for the Latching
	»LE38.Inverting Set«	Inverting the Setting Signal for the Latching

3.8.39 Logics / LE 39

	»LE39.Gate«	Logic gate
	»LE39.Input1«	Assignment of the Input Signal
	»LE39.Inverting1«	Inverting the input signals.
	»LE39.Input2«	Assignment of the Input Signal
	»LE39.Inverting2«	Inverting the input signals.
	»LE39.Input3«	Assignment of the Input Signal
	»LE39.Inverting3«	Inverting the input signals.
	»LE39.Input4«	Assignment of the Input Signal
	»LE39.Inverting4«	Inverting the input signals.
	»LE39.t-On Delay«	Switch On Delay
	»LE39.t-Off Delay«	Switch Off Delay
	»LE39.Reset Latched«	Reset Signal for the Latching
	»LE39.Inverting Reset«	Inverting Reset Signal for the Latching
	»LE39.Inverting Set«	Inverting the Setting Signal for the Latching

3.8.40 Logics / LE 40

	»LE40.Gate«	Logic gate
	»LE40.Input1«	Assignment of the Input Signal
	»LE40.Inverting1«	Inverting the input signals.
	»LE40.Input2«	Assignment of the Input Signal
	»LE40.Inverting2«	Inverting the input signals.
	»LE40.Input3«	Assignment of the Input Signal
	»LE40.Inverting3«	Inverting the input signals.
	»LE40.Input4«	Assignment of the Input Signal
	»LE40.Inverting4«	Inverting the input signals.
	»LE40.t-On Delay«	Switch On Delay
	»LE40.t-Off Delay«	Switch Off Delay
	»LE40.Reset Latched«	Reset Signal for the Latching
	»LE40.Inverting Reset«	Inverting Reset Signal for the Latching
	»LE40.Inverting Set«	Inverting the Setting Signal for the Latching

3.8.41 Logics / LE 41

	»LE41.Gate«	Logic gate
	»LE41.Input1«	Assignment of the Input Signal
	»LE41.Inverting1«	Inverting the input signals.
	»LE41.Input2«	Assignment of the Input Signal
	»LE41.Inverting2«	Inverting the input signals.
	»LE41.Input3«	Assignment of the Input Signal
	»LE41.Inverting3«	Inverting the input signals.
	»LE41.Input4«	Assignment of the Input Signal
	»LE41.Inverting4«	Inverting the input signals.
	»LE41.t-On Delay«	Switch On Delay
	»LE41.t-Off Delay«	Switch Off Delay
	»LE41.Reset Latched«	Reset Signal for the Latching
	»LE41.Inverting Reset«	Inverting Reset Signal for the Latching
	»LE41.Inverting Set«	Inverting the Setting Signal for the Latching

3.8.42 Logics / LE 42

	»LE42.Gate«	Logic gate
	»LE42.Input1«	Assignment of the Input Signal
	»LE42.Inverting1«	Inverting the input signals.
	»LE42.Input2«	Assignment of the Input Signal
	»LE42.Inverting2«	Inverting the input signals.
	»LE42.Input3«	Assignment of the Input Signal
	»LE42.Inverting3«	Inverting the input signals.
	»LE42.Input4«	Assignment of the Input Signal
	»LE42.Inverting4«	Inverting the input signals.
	»LE42.t-On Delay«	Switch On Delay
	»LE42.t-Off Delay«	Switch Off Delay
	»LE42.Reset Latched«	Reset Signal for the Latching
	»LE42.Inverting Reset«	Inverting Reset Signal for the Latching
	»LE42.Inverting Set«	Inverting the Setting Signal for the Latching

3.8.43 Logics / LE 43

	»LE43.Gate«	Logic gate
	»LE43.Input1«	Assignment of the Input Signal
	»LE43.Inverting1«	Inverting the input signals.
	»LE43.Input2«	Assignment of the Input Signal
	»LE43.Inverting2«	Inverting the input signals.
	»LE43.Input3«	Assignment of the Input Signal
	»LE43.Inverting3«	Inverting the input signals.
	»LE43.Input4«	Assignment of the Input Signal
	»LE43.Inverting4«	Inverting the input signals.
	»LE43.t-On Delay«	Switch On Delay
	»LE43.t-Off Delay«	Switch Off Delay
	»LE43.Reset Latched«	Reset Signal for the Latching
	»LE43.Inverting Reset«	Inverting Reset Signal for the Latching
	»LE43.Inverting Set«	Inverting the Setting Signal for the Latching

3.8.44 Logics / LE 44

	»LE44.Gate«	Logic gate
	»LE44.Input1«	Assignment of the Input Signal
	»LE44.Inverting1«	Inverting the input signals.
	»LE44.Input2«	Assignment of the Input Signal
	»LE44.Inverting2«	Inverting the input signals.
	»LE44.Input3«	Assignment of the Input Signal
	»LE44.Inverting3«	Inverting the input signals.
	»LE44.Input4«	Assignment of the Input Signal
	»LE44.Inverting4«	Inverting the input signals.
	»LE44.t-On Delay«	Switch On Delay
	»LE44.t-Off Delay«	Switch Off Delay
	»LE44.Reset Latched«	Reset Signal for the Latching
	»LE44.Inverting Reset«	Inverting Reset Signal for the Latching
	»LE44.Inverting Set«	Inverting the Setting Signal for the Latching

3.8.45 Logics / LE 45

	»LE45.Gate«	Logic gate
	»LE45.Input1«	Assignment of the Input Signal
	»LE45.Inverting1«	Inverting the input signals.
	»LE45.Input2«	Assignment of the Input Signal
	»LE45.Inverting2«	Inverting the input signals.
	»LE45.Input3«	Assignment of the Input Signal
	»LE45.Inverting3«	Inverting the input signals.
	»LE45.Input4«	Assignment of the Input Signal
	»LE45.Inverting4«	Inverting the input signals.
	»LE45.t-On Delay«	Switch On Delay
	»LE45.t-Off Delay«	Switch Off Delay
	»LE45.Reset Latched«	Reset Signal for the Latching
	»LE45.Inverting Reset«	Inverting Reset Signal for the Latching
	»LE45.Inverting Set«	Inverting the Setting Signal for the Latching

3.8.46 Logics / LE 46

	»LE46.Gate«	Logic gate
	»LE46.Input1«	Assignment of the Input Signal
	»LE46.Inverting1«	Inverting the input signals.
	»LE46.Input2«	Assignment of the Input Signal
	»LE46.Inverting2«	Inverting the input signals.
	»LE46.Input3«	Assignment of the Input Signal
	»LE46.Inverting3«	Inverting the input signals.
	»LE46.Input4«	Assignment of the Input Signal
	»LE46.Inverting4«	Inverting the input signals.
	»LE46.t-On Delay«	Switch On Delay
	»LE46.t-Off Delay«	Switch Off Delay
	»LE46.Reset Latched«	Reset Signal for the Latching
	»LE46.Inverting Reset«	Inverting Reset Signal for the Latching
	»LE46.Inverting Set«	Inverting the Setting Signal for the Latching

3.8.47 Logics / LE 47

	»LE47.Gate«	Logic gate
	»LE47.Input1«	Assignment of the Input Signal
	»LE47.Inverting1«	Inverting the input signals.
	»LE47.Input2«	Assignment of the Input Signal
	»LE47.Inverting2«	Inverting the input signals.
	»LE47.Input3«	Assignment of the Input Signal
	»LE47.Inverting3«	Inverting the input signals.
	»LE47.Input4«	Assignment of the Input Signal
	»LE47.Inverting4«	Inverting the input signals.
	»LE47.t-On Delay«	Switch On Delay
	»LE47.t-Off Delay«	Switch Off Delay
	»LE47.Reset Latched«	Reset Signal for the Latching
	»LE47.Inverting Reset«	Inverting Reset Signal for the Latching
	»LE47.Inverting Set«	Inverting the Setting Signal for the Latching

3.8.48 Logics / LE 48

	»LE48.Gate«	Logic gate
	»LE48.Input1«	Assignment of the Input Signal
	»LE48.Inverting1«	Inverting the input signals.
	»LE48.Input2«	Assignment of the Input Signal
	»LE48.Inverting2«	Inverting the input signals.
	»LE48.Input3«	Assignment of the Input Signal
	»LE48.Inverting3«	Inverting the input signals.
	»LE48.Input4«	Assignment of the Input Signal
	»LE48.Inverting4«	Inverting the input signals.
	»LE48.t-On Delay«	Switch On Delay
	»LE48.t-Off Delay«	Switch Off Delay
	»LE48.Reset Latched«	Reset Signal for the Latching
	»LE48.Inverting Reset«	Inverting Reset Signal for the Latching
	»LE48.Inverting Set«	Inverting the Setting Signal for the Latching

3.8.49 Logics / LE 49

	»LE49.Gate«	Logic gate
	»LE49.Input1«	Assignment of the Input Signal
	»LE49.Inverting1«	Inverting the input signals.
	»LE49.Input2«	Assignment of the Input Signal
	»LE49.Inverting2«	Inverting the input signals.
	»LE49.Input3«	Assignment of the Input Signal
	»LE49.Inverting3«	Inverting the input signals.
	»LE49.Input4«	Assignment of the Input Signal
	»LE49.Inverting4«	Inverting the input signals.
	»LE49.t-On Delay«	Switch On Delay
	»LE49.t-Off Delay«	Switch Off Delay
	»LE49.Reset Latched«	Reset Signal for the Latching
	»LE49.Inverting Reset«	Inverting Reset Signal for the Latching
	»LE49.Inverting Set«	Inverting the Setting Signal for the Latching

3.8.50 Logics / LE 50

	»LE50.Gate«	Logic gate
	»LE50.Input1«	Assignment of the Input Signal
	»LE50.Inverting1«	Inverting the input signals.
	»LE50.Input2«	Assignment of the Input Signal
	»LE50.Inverting2«	Inverting the input signals.
	»LE50.Input3«	Assignment of the Input Signal
	»LE50.Inverting3«	Inverting the input signals.
	»LE50.Input4«	Assignment of the Input Signal
	»LE50.Inverting4«	Inverting the input signals.
	»LE50.t-On Delay«	Switch On Delay
	»LE50.t-Off Delay«	Switch Off Delay
	»LE50.Reset Latched«	Reset Signal for the Latching
	»LE50.Inverting Reset«	Inverting Reset Signal for the Latching
	»LE50.Inverting Set«	Inverting the Setting Signal for the Latching

3.8.51 Logics / LE 51

	»LE51.Gate«	Logic gate
	»LE51.Input1«	Assignment of the Input Signal
	»LE51.Inverting1«	Inverting the input signals.
	»LE51.Input2«	Assignment of the Input Signal
	»LE51.Inverting2«	Inverting the input signals.
	»LE51.Input3«	Assignment of the Input Signal
	»LE51.Inverting3«	Inverting the input signals.
	»LE51.Input4«	Assignment of the Input Signal
	»LE51.Inverting4«	Inverting the input signals.
	»LE51.t-On Delay«	Switch On Delay
	»LE51.t-Off Delay«	Switch Off Delay
	»LE51.Reset Latched«	Reset Signal for the Latching
	»LE51.Inverting Reset«	Inverting Reset Signal for the Latching
	»LE51.Inverting Set«	Inverting the Setting Signal for the Latching

3.8.52 Logics / LE 52

	»LE52.Gate«	Logic gate
	»LE52.Input1«	Assignment of the Input Signal
	»LE52.Inverting1«	Inverting the input signals.
	»LE52.Input2«	Assignment of the Input Signal
	»LE52.Inverting2«	Inverting the input signals.
	»LE52.Input3«	Assignment of the Input Signal
	»LE52.Inverting3«	Inverting the input signals.
	»LE52.Input4«	Assignment of the Input Signal
	»LE52.Inverting4«	Inverting the input signals.
	»LE52.t-On Delay«	Switch On Delay
	»LE52.t-Off Delay«	Switch Off Delay
	»LE52.Reset Latched«	Reset Signal for the Latching
	»LE52.Inverting Reset«	Inverting Reset Signal for the Latching
	»LE52.Inverting Set«	Inverting the Setting Signal for the Latching

3.8.53 Logics / LE 53

	»LE53.Gate«	Logic gate
	»LE53.Input1«	Assignment of the Input Signal
	»LE53.Inverting1«	Inverting the input signals.
	»LE53.Input2«	Assignment of the Input Signal
	»LE53.Inverting2«	Inverting the input signals.
	»LE53.Input3«	Assignment of the Input Signal
	»LE53.Inverting3«	Inverting the input signals.
	»LE53.Input4«	Assignment of the Input Signal
	»LE53.Inverting4«	Inverting the input signals.
	»LE53.t-On Delay«	Switch On Delay
	»LE53.t-Off Delay«	Switch Off Delay
	»LE53.Reset Latched«	Reset Signal for the Latching
	»LE53.Inverting Reset«	Inverting Reset Signal for the Latching
	»LE53.Inverting Set«	Inverting the Setting Signal for the Latching

3.8.54 Logics / LE 54

	»LE54.Gate«	Logic gate
	»LE54.Input1«	Assignment of the Input Signal
	»LE54.Inverting1«	Inverting the input signals.
	»LE54.Input2«	Assignment of the Input Signal
	»LE54.Inverting2«	Inverting the input signals.
	»LE54.Input3«	Assignment of the Input Signal
	»LE54.Inverting3«	Inverting the input signals.
	»LE54.Input4«	Assignment of the Input Signal
	»LE54.Inverting4«	Inverting the input signals.
	»LE54.t-On Delay«	Switch On Delay
	»LE54.t-Off Delay«	Switch Off Delay
	»LE54.Reset Latched«	Reset Signal for the Latching
	»LE54.Inverting Reset«	Inverting Reset Signal for the Latching
	»LE54.Inverting Set«	Inverting the Setting Signal for the Latching

3.8.55 Logics / LE 55

	»LE55.Gate«	Logic gate
	»LE55.Input1«	Assignment of the Input Signal
	»LE55.Inverting1«	Inverting the input signals.
	»LE55.Input2«	Assignment of the Input Signal
	»LE55.Inverting2«	Inverting the input signals.
	»LE55.Input3«	Assignment of the Input Signal
	»LE55.Inverting3«	Inverting the input signals.
	»LE55.Input4«	Assignment of the Input Signal
	»LE55.Inverting4«	Inverting the input signals.
	»LE55.t-On Delay«	Switch On Delay
	»LE55.t-Off Delay«	Switch Off Delay
	»LE55.Reset Latched«	Reset Signal for the Latching
	»LE55.Inverting Reset«	Inverting Reset Signal for the Latching
	»LE55.Inverting Set«	Inverting the Setting Signal for the Latching

3.8.56 Logics / LE 56

	»LE56.Gate«	Logic gate
	»LE56.Input1«	Assignment of the Input Signal
	»LE56.Inverting1«	Inverting the input signals.
	»LE56.Input2«	Assignment of the Input Signal
	»LE56.Inverting2«	Inverting the input signals.
	»LE56.Input3«	Assignment of the Input Signal
	»LE56.Inverting3«	Inverting the input signals.
	»LE56.Input4«	Assignment of the Input Signal
	»LE56.Inverting4«	Inverting the input signals.
	»LE56.t-On Delay«	Switch On Delay
	»LE56.t-Off Delay«	Switch Off Delay
	»LE56.Reset Latched«	Reset Signal for the Latching
	»LE56.Inverting Reset«	Inverting Reset Signal for the Latching
	»LE56.Inverting Set«	Inverting the Setting Signal for the Latching

3.8.57 Logics / LE 57

	»LE57.Gate«	Logic gate
	»LE57.Input1«	Assignment of the Input Signal
	»LE57.Inverting1«	Inverting the input signals.
	»LE57.Input2«	Assignment of the Input Signal
	»LE57.Inverting2«	Inverting the input signals.
	»LE57.Input3«	Assignment of the Input Signal
	»LE57.Inverting3«	Inverting the input signals.
	»LE57.Input4«	Assignment of the Input Signal
	»LE57.Inverting4«	Inverting the input signals.
	»LE57.t-On Delay«	Switch On Delay
	»LE57.t-Off Delay«	Switch Off Delay
	»LE57.Reset Latched«	Reset Signal for the Latching
	»LE57.Inverting Reset«	Inverting Reset Signal for the Latching
	»LE57.Inverting Set«	Inverting the Setting Signal for the Latching

3.8.58 Logics / LE 58

	»LE58.Gate«	Logic gate
	»LE58.Input1«	Assignment of the Input Signal
	»LE58.Inverting1«	Inverting the input signals.
	»LE58.Input2«	Assignment of the Input Signal
	»LE58.Inverting2«	Inverting the input signals.
	»LE58.Input3«	Assignment of the Input Signal
	»LE58.Inverting3«	Inverting the input signals.
	»LE58.Input4«	Assignment of the Input Signal
	»LE58.Inverting4«	Inverting the input signals.
	»LE58.t-On Delay«	Switch On Delay
	»LE58.t-Off Delay«	Switch Off Delay
	»LE58.Reset Latched«	Reset Signal for the Latching
	»LE58.Inverting Reset«	Inverting Reset Signal for the Latching
	»LE58.Inverting Set«	Inverting the Setting Signal for the Latching

3.8.59 Logics / LE 59

	»LE59.Gate«	Logic gate
	»LE59.Input1«	Assignment of the Input Signal
	»LE59.Inverting1«	Inverting the input signals.
	»LE59.Input2«	Assignment of the Input Signal
	»LE59.Inverting2«	Inverting the input signals.
	»LE59.Input3«	Assignment of the Input Signal
	»LE59.Inverting3«	Inverting the input signals.
	»LE59.Input4«	Assignment of the Input Signal
	»LE59.Inverting4«	Inverting the input signals.
	»LE59.t-On Delay«	Switch On Delay
	»LE59.t-Off Delay«	Switch Off Delay
	»LE59.Reset Latched«	Reset Signal for the Latching
	»LE59.Inverting Reset«	Inverting Reset Signal for the Latching
	»LE59.Inverting Set«	Inverting the Setting Signal for the Latching

3.8.60 Logics / LE 60

	»LE60.Gate«	Logic gate
	»LE60.Input1«	Assignment of the Input Signal
	»LE60.Inverting1«	Inverting the input signals.
	»LE60.Input2«	Assignment of the Input Signal
	»LE60.Inverting2«	Inverting the input signals.
	»LE60.Input3«	Assignment of the Input Signal
	»LE60.Inverting3«	Inverting the input signals.
	»LE60.Input4«	Assignment of the Input Signal
	»LE60.Inverting4«	Inverting the input signals.
	»LE60.t-On Delay«	Switch On Delay
	»LE60.t-Off Delay«	Switch Off Delay
	»LE60.Reset Latched«	Reset Signal for the Latching
	»LE60.Inverting Reset«	Inverting Reset Signal for the Latching
	»LE60.Inverting Set«	Inverting the Setting Signal for the Latching

3.8.61 Logics / LE 61

	»LE61.Gate«	Logic gate
	»LE61.Input1«	Assignment of the Input Signal
	»LE61.Inverting1«	Inverting the input signals.
	»LE61.Input2«	Assignment of the Input Signal
	»LE61.Inverting2«	Inverting the input signals.
	»LE61.Input3«	Assignment of the Input Signal
	»LE61.Inverting3«	Inverting the input signals.
	»LE61.Input4«	Assignment of the Input Signal
	»LE61.Inverting4«	Inverting the input signals.
	»LE61.t-On Delay«	Switch On Delay
	»LE61.t-Off Delay«	Switch Off Delay
	»LE61.Reset Latched«	Reset Signal for the Latching
	»LE61.Inverting Reset«	Inverting Reset Signal for the Latching
	»LE61.Inverting Set«	Inverting the Setting Signal for the Latching

3.8.62 Logics / LE 62

	»LE62.Gate«	Logic gate
	»LE62.Input1«	Assignment of the Input Signal
	»LE62.Inverting1«	Inverting the input signals.
	»LE62.Input2«	Assignment of the Input Signal
	»LE62.Inverting2«	Inverting the input signals.
	»LE62.Input3«	Assignment of the Input Signal
	»LE62.Inverting3«	Inverting the input signals.
	»LE62.Input4«	Assignment of the Input Signal
	»LE62.Inverting4«	Inverting the input signals.
	»LE62.t-On Delay«	Switch On Delay
	»LE62.t-Off Delay«	Switch Off Delay
	»LE62.Reset Latched«	Reset Signal for the Latching
	»LE62.Inverting Reset«	Inverting Reset Signal for the Latching
	»LE62.Inverting Set«	Inverting the Setting Signal for the Latching

3.8.63 Logics / LE 63

	»LE63.Gate«	Logic gate
	»LE63.Input1«	Assignment of the Input Signal
	»LE63.Inverting1«	Inverting the input signals.
	»LE63.Input2«	Assignment of the Input Signal
	»LE63.Inverting2«	Inverting the input signals.
	»LE63.Input3«	Assignment of the Input Signal
	»LE63.Inverting3«	Inverting the input signals.
	»LE63.Input4«	Assignment of the Input Signal
	»LE63.Inverting4«	Inverting the input signals.
	»LE63.t-On Delay«	Switch On Delay
	»LE63.t-Off Delay«	Switch Off Delay
	»LE63.Reset Latched«	Reset Signal for the Latching
	»LE63.Inverting Reset«	Inverting Reset Signal for the Latching
	»LE63.Inverting Set«	Inverting the Setting Signal for the Latching

3.8.64 Logics / LE 64

	»LE64.Gate«	Logic gate
	»LE64.Input1«	Assignment of the Input Signal
	»LE64.Inverting1«	Inverting the input signals.
	»LE64.Input2«	Assignment of the Input Signal
	»LE64.Inverting2«	Inverting the input signals.
	»LE64.Input3«	Assignment of the Input Signal
	»LE64.Inverting3«	Inverting the input signals.
	»LE64.Input4«	Assignment of the Input Signal
	»LE64.Inverting4«	Inverting the input signals.
	»LE64.t-On Delay«	Switch On Delay
	»LE64.t-Off Delay«	Switch Off Delay
	»LE64.Reset Latched«	Reset Signal for the Latching
	»LE64.Inverting Reset«	Inverting Reset Signal for the Latching
	»LE64.Inverting Set«	Inverting the Setting Signal for the Latching

3.8.65 Logics / LE 65

	»LE65.Gate«	Logic gate
	»LE65.Input1«	Assignment of the Input Signal
	»LE65.Inverting1«	Inverting the input signals.
	»LE65.Input2«	Assignment of the Input Signal
	»LE65.Inverting2«	Inverting the input signals.
	»LE65.Input3«	Assignment of the Input Signal
	»LE65.Inverting3«	Inverting the input signals.
	»LE65.Input4«	Assignment of the Input Signal
	»LE65.Inverting4«	Inverting the input signals.
	»LE65.t-On Delay«	Switch On Delay
	»LE65.t-Off Delay«	Switch Off Delay
	»LE65.Reset Latched«	Reset Signal for the Latching
	»LE65.Inverting Reset«	Inverting Reset Signal for the Latching
	»LE65.Inverting Set«	Inverting the Setting Signal for the Latching

3.8.66 Logics / LE 66

	»LE66.Gate«	Logic gate
	»LE66.Input1«	Assignment of the Input Signal
	»LE66.Inverting1«	Inverting the input signals.
	»LE66.Input2«	Assignment of the Input Signal
	»LE66.Inverting2«	Inverting the input signals.
	»LE66.Input3«	Assignment of the Input Signal
	»LE66.Inverting3«	Inverting the input signals.
	»LE66.Input4«	Assignment of the Input Signal
	»LE66.Inverting4«	Inverting the input signals.
	»LE66.t-On Delay«	Switch On Delay
	»LE66.t-Off Delay«	Switch Off Delay
	»LE66.Reset Latched«	Reset Signal for the Latching
	»LE66.Inverting Reset«	Inverting Reset Signal for the Latching
	»LE66.Inverting Set«	Inverting the Setting Signal for the Latching

3.8.67 Logics / LE 67

	»LE67.Gate«	Logic gate
	»LE67.Input1«	Assignment of the Input Signal
	»LE67.Inverting1«	Inverting the input signals.
	»LE67.Input2«	Assignment of the Input Signal
	»LE67.Inverting2«	Inverting the input signals.
	»LE67.Input3«	Assignment of the Input Signal
	»LE67.Inverting3«	Inverting the input signals.
	»LE67.Input4«	Assignment of the Input Signal
	»LE67.Inverting4«	Inverting the input signals.
	»LE67.t-On Delay«	Switch On Delay
	»LE67.t-Off Delay«	Switch Off Delay
	»LE67.Reset Latched«	Reset Signal for the Latching
	»LE67.Inverting Reset«	Inverting Reset Signal for the Latching
	»LE67.Inverting Set«	Inverting the Setting Signal for the Latching

3.8.68 Logics / LE 68

	»LE68.Gate«	Logic gate
	»LE68.Input1«	Assignment of the Input Signal
	»LE68.Inverting1«	Inverting the input signals.
	»LE68.Input2«	Assignment of the Input Signal
	»LE68.Inverting2«	Inverting the input signals.
	»LE68.Input3«	Assignment of the Input Signal
	»LE68.Inverting3«	Inverting the input signals.
	»LE68.Input4«	Assignment of the Input Signal
	»LE68.Inverting4«	Inverting the input signals.
	»LE68.t-On Delay«	Switch On Delay
	»LE68.t-Off Delay«	Switch Off Delay
	»LE68.Reset Latched«	Reset Signal for the Latching
	»LE68.Inverting Reset«	Inverting Reset Signal for the Latching
	»LE68.Inverting Set«	Inverting the Setting Signal for the Latching

3.8.69 Logics / LE 69

	»LE69.Gate«	Logic gate
	»LE69.Input1«	Assignment of the Input Signal
	»LE69.Inverting1«	Inverting the input signals.
	»LE69.Input2«	Assignment of the Input Signal
	»LE69.Inverting2«	Inverting the input signals.
	»LE69.Input3«	Assignment of the Input Signal
	»LE69.Inverting3«	Inverting the input signals.
	»LE69.Input4«	Assignment of the Input Signal
	»LE69.Inverting4«	Inverting the input signals.
	»LE69.t-On Delay«	Switch On Delay
	»LE69.t-Off Delay«	Switch Off Delay
	»LE69.Reset Latched«	Reset Signal for the Latching
	»LE69.Inverting Reset«	Inverting Reset Signal for the Latching
	»LE69.Inverting Set«	Inverting the Setting Signal for the Latching

3.8.70 Logics / LE 70

	»LE70.Gate«	Logic gate
	»LE70.Input1«	Assignment of the Input Signal
	»LE70.Inverting1«	Inverting the input signals.
	»LE70.Input2«	Assignment of the Input Signal
	»LE70.Inverting2«	Inverting the input signals.
	»LE70.Input3«	Assignment of the Input Signal
	»LE70.Inverting3«	Inverting the input signals.
	»LE70.Input4«	Assignment of the Input Signal
	»LE70.Inverting4«	Inverting the input signals.
	»LE70.t-On Delay«	Switch On Delay
	»LE70.t-Off Delay«	Switch Off Delay
	»LE70.Reset Latched«	Reset Signal for the Latching
	»LE70.Inverting Reset«	Inverting Reset Signal for the Latching
	»LE70.Inverting Set«	Inverting the Setting Signal for the Latching

3.8.71 Logics / LE 71

	»LE71.Gate«	Logic gate
	»LE71.Input1«	Assignment of the Input Signal
	»LE71.Inverting1«	Inverting the input signals.
	»LE71.Input2«	Assignment of the Input Signal
	»LE71.Inverting2«	Inverting the input signals.
	»LE71.Input3«	Assignment of the Input Signal
	»LE71.Inverting3«	Inverting the input signals.
	»LE71.Input4«	Assignment of the Input Signal
	»LE71.Inverting4«	Inverting the input signals.
	»LE71.t-On Delay«	Switch On Delay
	»LE71.t-Off Delay«	Switch Off Delay
	»LE71.Reset Latched«	Reset Signal for the Latching
	»LE71.Inverting Reset«	Inverting Reset Signal for the Latching
	»LE71.Inverting Set«	Inverting the Setting Signal for the Latching

3.8.72 Logics / LE 72

	»LE72.Gate«	Logic gate
	»LE72.Input1«	Assignment of the Input Signal
	»LE72.Inverting1«	Inverting the input signals.
	»LE72.Input2«	Assignment of the Input Signal
	»LE72.Inverting2«	Inverting the input signals.
	»LE72.Input3«	Assignment of the Input Signal
	»LE72.Inverting3«	Inverting the input signals.
	»LE72.Input4«	Assignment of the Input Signal
	»LE72.Inverting4«	Inverting the input signals.
	»LE72.t-On Delay«	Switch On Delay
	»LE72.t-Off Delay«	Switch Off Delay
	»LE72.Reset Latched«	Reset Signal for the Latching
	»LE72.Inverting Reset«	Inverting Reset Signal for the Latching
	»LE72.Inverting Set«	Inverting the Setting Signal for the Latching

3.8.73 Logics / LE 73

	»LE73.Gate«	Logic gate
	»LE73.Input1«	Assignment of the Input Signal
	»LE73.Inverting1«	Inverting the input signals.
	»LE73.Input2«	Assignment of the Input Signal
	»LE73.Inverting2«	Inverting the input signals.
	»LE73.Input3«	Assignment of the Input Signal
	»LE73.Inverting3«	Inverting the input signals.
	»LE73.Input4«	Assignment of the Input Signal
	»LE73.Inverting4«	Inverting the input signals.
	»LE73.t-On Delay«	Switch On Delay
	»LE73.t-Off Delay«	Switch Off Delay
	»LE73.Reset Latched«	Reset Signal for the Latching
	»LE73.Inverting Reset«	Inverting Reset Signal for the Latching
	»LE73.Inverting Set«	Inverting the Setting Signal for the Latching

3.8.74 Logics / LE 74

	»LE74.Gate«	Logic gate
	»LE74.Input1«	Assignment of the Input Signal
	»LE74.Inverting1«	Inverting the input signals.
	»LE74.Input2«	Assignment of the Input Signal
	»LE74.Inverting2«	Inverting the input signals.
	»LE74.Input3«	Assignment of the Input Signal
	»LE74.Inverting3«	Inverting the input signals.
	»LE74.Input4«	Assignment of the Input Signal
	»LE74.Inverting4«	Inverting the input signals.
	»LE74.t-On Delay«	Switch On Delay
	»LE74.t-Off Delay«	Switch Off Delay
	»LE74.Reset Latched«	Reset Signal for the Latching
	»LE74.Inverting Reset«	Inverting Reset Signal for the Latching
	»LE74.Inverting Set«	Inverting the Setting Signal for the Latching

3.8.75 Logics / LE 75

	»LE75.Gate«	Logic gate
	»LE75.Input1«	Assignment of the Input Signal
	»LE75.Inverting1«	Inverting the input signals.
	»LE75.Input2«	Assignment of the Input Signal
	»LE75.Inverting2«	Inverting the input signals.
	»LE75.Input3«	Assignment of the Input Signal
	»LE75.Inverting3«	Inverting the input signals.
	»LE75.Input4«	Assignment of the Input Signal
	»LE75.Inverting4«	Inverting the input signals.
	»LE75.t-On Delay«	Switch On Delay
	»LE75.t-Off Delay«	Switch Off Delay
	»LE75.Reset Latched«	Reset Signal for the Latching
	»LE75.Inverting Reset«	Inverting Reset Signal for the Latching
	»LE75.Inverting Set«	Inverting the Setting Signal for the Latching

3.8.76 Logics / LE 76

	»LE76.Gate«	Logic gate
	»LE76.Input1«	Assignment of the Input Signal
	»LE76.Inverting1«	Inverting the input signals.
	»LE76.Input2«	Assignment of the Input Signal
	»LE76.Inverting2«	Inverting the input signals.
	»LE76.Input3«	Assignment of the Input Signal
	»LE76.Inverting3«	Inverting the input signals.
	»LE76.Input4«	Assignment of the Input Signal
	»LE76.Inverting4«	Inverting the input signals.
	»LE76.t-On Delay«	Switch On Delay
	»LE76.t-Off Delay«	Switch Off Delay
	»LE76.Reset Latched«	Reset Signal for the Latching
	»LE76.Inverting Reset«	Inverting Reset Signal for the Latching
	»LE76.Inverting Set«	Inverting the Setting Signal for the Latching

3.8.77 Logics / LE 77

	»LE77.Gate«	Logic gate
	»LE77.Input1«	Assignment of the Input Signal
	»LE77.Inverting1«	Inverting the input signals.
	»LE77.Input2«	Assignment of the Input Signal
	»LE77.Inverting2«	Inverting the input signals.
	»LE77.Input3«	Assignment of the Input Signal
	»LE77.Inverting3«	Inverting the input signals.
	»LE77.Input4«	Assignment of the Input Signal
	»LE77.Inverting4«	Inverting the input signals.
	»LE77.t-On Delay«	Switch On Delay
	»LE77.t-Off Delay«	Switch Off Delay
	»LE77.Reset Latched«	Reset Signal for the Latching
	»LE77.Inverting Reset«	Inverting Reset Signal for the Latching
	»LE77.Inverting Set«	Inverting the Setting Signal for the Latching

3.8.78 Logics / LE 78

	»LE78.Gate«	Logic gate
	»LE78.Input1«	Assignment of the Input Signal
	»LE78.Inverting1«	Inverting the input signals.
	»LE78.Input2«	Assignment of the Input Signal
	»LE78.Inverting2«	Inverting the input signals.
	»LE78.Input3«	Assignment of the Input Signal
	»LE78.Inverting3«	Inverting the input signals.
	»LE78.Input4«	Assignment of the Input Signal
	»LE78.Inverting4«	Inverting the input signals.
	»LE78.t-On Delay«	Switch On Delay
	»LE78.t-Off Delay«	Switch Off Delay
	»LE78.Reset Latched«	Reset Signal for the Latching
	»LE78.Inverting Reset«	Inverting Reset Signal for the Latching
	»LE78.Inverting Set«	Inverting the Setting Signal for the Latching

3.8.79 Logics / LE 79

	»LE79.Gate«	Logic gate
	»LE79.Input1«	Assignment of the Input Signal
	»LE79.Inverting1«	Inverting the input signals.
	»LE79.Input2«	Assignment of the Input Signal
	»LE79.Inverting2«	Inverting the input signals.
	»LE79.Input3«	Assignment of the Input Signal
	»LE79.Inverting3«	Inverting the input signals.
	»LE79.Input4«	Assignment of the Input Signal
	»LE79.Inverting4«	Inverting the input signals.
	»LE79.t-On Delay«	Switch On Delay
	»LE79.t-Off Delay«	Switch Off Delay
	»LE79.Reset Latched«	Reset Signal for the Latching
	»LE79.Inverting Reset«	Inverting Reset Signal for the Latching
	»LE79.Inverting Set«	Inverting the Setting Signal for the Latching

3.8.80 Logics / LE 80

	»LE80.Gate«	Logic gate
	»LE80.Input1«	Assignment of the Input Signal
	»LE80.Inverting1«	Inverting the input signals.
	»LE80.Input2«	Assignment of the Input Signal
	»LE80.Inverting2«	Inverting the input signals.
	»LE80.Input3«	Assignment of the Input Signal
	»LE80.Inverting3«	Inverting the input signals.
	»LE80.Input4«	Assignment of the Input Signal
	»LE80.Inverting4«	Inverting the input signals.
	»LE80.t-On Delay«	Switch On Delay
	»LE80.t-Off Delay«	Switch Off Delay
	»LE80.Reset Latched«	Reset Signal for the Latching
	»LE80.Inverting Reset«	Inverting Reset Signal for the Latching
	»LE80.Inverting Set«	Inverting the Setting Signal for the Latching

3.9 Service

3.9.1 Service / General

◉	»Sys . Reboot«	Rebooting the device.

3.9.2 Service / Maint Mode

🔧	»Maint Mode«	Activation Mode of the Arc Flash Reduction. Switching into another mode is only possible when no Activation Signal is active (pending).
🔧	»Maint Mode Activated by«	Activation Signal for the Arc Flash Reduction Maintenance Switch

3.9.3 Service / Test - Prot inhib.

3.9.3.1 Service / Test - Prot inhib. / DISARMED

3.9.3.1.1 Service / Test - Prot inhib. / DISARMED / BO Slot X2

🔧	»DISARMED Ctrl«	Enables and disables the disarming of the relay outputs. This is the first step of a two step process, to inhibit the operation or the relay outputs. Please refer to "DISARMED" for the second step.
🔧	»Disarm Mode«	CAUTION! RELAYS DISARMED in order to safely perform maintenance while eliminating the risk of taking an entire process off-line. (Note: The Supervision Contact cannot be disarmed). YOU MUST ENSURE that the relays are ARMED AGAIN after maintenance.
🔧	»t-Timeout DISARM«	The relays will be armed again after expiring of this time.
◉	»DISARMED«	This is the second step, after the "DISARMED Ctrl" has been activated, that is required to DISARM the relay outputs. This will DISARM those output relays that are currently not latched and that are not on “hold” by a pending minimum hold time. CAUTION! RELAYS DISARMED in order to safely perform maintenance while eliminating the risk of taking an entire process off-line. (Note: Zone Interlocking and Supervision Contact cannot be disarmed). YOU MUST ENSURE that the relays are ARMED AGAIN after maintenance.

3.9.3.2 Service / Test - Prot inhib. / Scada

3.9.3.2.1 Service / Test - Prot inhib. / Scada / IEC103

	»Activate test mode«	This Direct Control parameter switches the IEC103 communication into Test Mode (or back to nomal mode).
	»Activate Block MD«	This Direct Control parameter activates (or deactivates) the blocking of IEC103 transmission in monitor direction.
	»Ex activate test mode«	The signal assigned to this parameter switches the IEC103 communication into Test Mode.
	»Ex activate Block MD«	The signal assigned to this parameter activates the blocking of IEC103 transmission in monitor direction.

3.9.3.3 Service / Test - Prot inhib. / Force OR

3.9.3.3.1 Service / Test - Prot inhib. / Force OR / BO Slot X2

	»Force Mode«	By means of this function the normal Output Relay States can be overwritten (forced) in case that the Relay is not in a disarmed state. The relays can be set from normal operation (relay works according to the assigned signals) to "force energized" or "force de-energized" state.
	»t-Timeout Force«	The Output State will be set by force for the duration of this time. That means for the duration of this time the Output Relay does not show the state of the signals that are assigned on it.
	»Force all Outs«	By means of this function the normal Output Relay State can be overwritten (forced). The relay can be set from normal operation (relay works according to the assigned signals) to "force energized" or "force de-energized" state. Forcing all outputs relays of an entire assembly group is superior to forcing a single output relay.
	»Force OR1«	By means of this function the normal Output Relay State can be overwritten (forced). The relay can be set from normal operation (relay works according to the assigned signals) to "force energized" or "force de-energized" state.
	»Force OR2«	By means of this function the normal Output Relay State can be overwritten (forced). The relay can be set from normal operation (relay works according to the assigned signals) to "force energized" or "force de-energized" state.
	»Force OR3«	By means of this function the normal Output Relay State can be overwritten (forced). The relay can be set from normal operation (relay works according to the assigned signals) to "force energized" or "force de-energized" state.
	»Force OR4«	By means of this function the normal Output Relay State can be overwritten (forced). The relay can be set from normal operation (relay works according to the assigned signals) to "force energized" or "force de-energized" state.
	»Force OR5«	By means of this function the normal Output Relay State can be overwritten (forced). The relay can be set from normal operation (relay works according to the assigned signals) to "force energized" or "force de-energized" state.

3.9.3.4 Service / Test - Prot inhib. / Force SG

	»SG[1] . Force Trip Cmd«	Direct Command to force the device to issue a trip command (for testing purposes).

3.9.3.5 Service / Test - Prot inhib. / Force SC

	»SSV . Force SC«	Direct Command to force the device to drop SelfSuperVision Contact (SC) for 5 seconds (for testing purposes).

3.9.3.6 Service / Test - Prot inhib. / Sgen

3.9.3.6.1 Service / Test - Prot inhib. / Sgen / State

	»Running«	Signal: Measuring value simulation is running
	»State«	Wave generation states: 0=Off, 1=PreFault, 2=Fault, 3=PostFault, 4=InitReset
	»ExBlo1-I«	Module input state: External blocking1
	»ExBlo2-I«	Module input state: External blocking2
	»Ex ForcePost-I«	State of the module input:Force Post state. Abort simulation.

3.9.3.6.2 Service / Test - Prot inhib. / Sgen / Process

	»Start Simulation«	Start Fault Simulation (Using the test parameters)
	»Stop Simulation«	Stopp Fault Simulation (Using the test parameters)
	»TripCmd Mode«	Trip Command Mode: Select between two operating modes for the Fault Simulator: "cold simulation" (without tripping the circuit breaker), or "hot simulation" (i.e. the simulation is authorized to trip the circuit breaker)
	»Ex Start Simulation«	External Start of Fault Simulation (Using the test parameters)
	»ExBlo1«	External blocking of the module, if blocking is activated (allowed) within a parameter set and if the state of the assigned signal is true.1
	»ExBlo2«	External blocking of the module, if blocking is activated (allowed) within a parameter set and if the state of the assigned signal is true.2
	»Ex ForcePost«	Force Post state. Abort simulation.

3.9.3.6.3 Service / Test - Prot inhib. / Sgen / Configuration

3.9.3.6.3.1 Service / Test - Prot inhib. / Sgen / Configuration / Times

	»PreFault«	Pre Fault Duration
	»FaultSimulation«	Duration of Fault Simulation
	»PostFault«	Post Fault Duration

3.9.3.6.3.2 Service / Test - Prot inhib. / Sgen / Configuration / PreFault

3.9.3.6.3.2.1 Service / Test - Prot inhib. / Sgen / Configuration / PreFault / VT

	»VL1 «	Voltage Fundamental Magnitude in Pre State: phase L1
	»VL2 «	Voltage Fundamental Magnitude in Pre State: phase L2
	»VL3 «	Voltage Fundamental Magnitude in Pre State: phase L3
	»VX «	Voltage Fundamental Magnitude in Pre State: VX
	»phi VL1 «	Start Position respectively Start Angle of the Voltage Phasor during Pre-Phase:phase L1
	»phi VL2 «	Start Position respectively Start Angle of the Voltage Phasor during Pre-Phase:phase L2
	»phi VL3 «	Start Position respectively Start Angle of the Voltage Phasor during Pre-Phase:phase L3
	»phi VX meas «	Start Position respectively Start Angle of the Voltage Phasor during Pre-Phase: VX

3.9.3.6.3.3 Service / Test - Prot inhib. / Sgen / Configuration / FaultSimulation

3.9.3.6.3.3.1 Service / Test - Prot inhib. / Sgen / Configuration / FaultSimulation / VT

	»VL1 «	Voltage Fundamental Magnitude in Fault State: phase L1
	»VL2 «	Voltage Fundamental Magnitude in Fault State: phase L2
	»VL3 «	Voltage Fundamental Magnitude in Fault State: phase L3
	»VX «	Voltage Fundamental Magnitude in Fault State: phase VX
	»phi VL1 «	Start Position respectively Start Angle of the Voltage Phasor during Fault-Phase:phase L1
	»phi VL2 «	Start Position respectively Start Angle of the Voltage Phasor during Fault-Phase:phase L2
	»phi VL3 «	Start Position respectively Start Angle of the Voltage Phasor during Fault-Phase:phase L3
	»phi VX meas «	Start Position respectively Start Angle of the Voltage Phasor during Fault-Phase: VX

3.9.3.6.3.4 Service / Test - Prot inhib. / Sgen / Configuration / PostFault

3.9.3.6.3.4.1 Service / Test - Prot inhib. / Sgen / Configuration / PostFault / VT

	»VL1 «	Voltage Fundamental Magnitude during Post phase: phase L1
	»VL2 «	Voltage Fundamental Magnitude during Post phase: phase L2
	»VL3 «	Voltage Fundamental Magnitude during Post phase: phase L3
	»VX «	Voltage Fundamental Magnitude during Post phase: phase VX
	»phi VL1 «	Start Position respectively Start Angle of the Voltage Phasor during Post phase: phase L1
	»phi VL2 «	Start Position respectively Start Angle of the Voltage Phasor during Post phase: phase L2
	»phi VL3 «	Start Position respectively Start Angle of the Voltage Phasor during Post phase: phase L3
	»phi VX meas «	Start Position respectively Start Angle of the Voltage Phasor during Post phase: phase VX

3.9.4 Service / Diagnostic Data

3.9.4.1 Service / Diagnostic Data / FADC

	»Sys . FADC_TR«	FADC_TR: total (retain)
	»Sys . FADC_LR«	FADC-LR: long (10min, max, retain)
	»Sys . FADC_MR«	FADC-MR: mid (10s, max, retain)
	»Sys . FADC_SR«	FADC-SR: short(0.2s, max, retain)
	»Sys . FADC_LM«	FADC-LM: long (10min, max, since reset
	»Sys . FADC_MM«	FADC-MM: mid (10s, max, since reset
	»Sys . FADC_SM«	FADC-SM: short (0.2s, max, since reset)
	»Sys . FADC_L«	FADC-L: long (10mmin)
	»Sys . FADC_M«	FADC-M: mid (10s)
	»Sys . FADC_S«	FADC-S: short (0.2s)
	»Sys . Reset-FADC«	Reset: FADC-Counter

4 Hardware

4.1 HMI

front-panel

4.1.1 HMI: Global Parameters

t-max Edit/Access	Device Para / Security / General Settings	
180s	20s ... 3600s	*S.3*
If no other key(s) is pressed at the panel, after expiration of this time, all cached (changed) parameters are canceled. The device access will be locked by falling back into Read-only level Lv0.		

Display Off	Device Para / HMI	
180s	20s ... 3600s	*S.3*
The display back light will be turned off when this timer has expired.		

Menu language	Device Para / HMI	
English	English ... Romanian Table	*S.3*
Selection of the language		

Display ANSI Device No.	Device Para / HMI	
Active	Inactive, Active Table	*S.3*
Display ANSI Device Numbers		

4.1.2 HMI: Direct Controls

Contrast	Device Para / HMI	
50%	0% ... 100%	*S.3*
Contrast		

Conf. Dev. Reset	Device Para / Security / General Settings	
"Fact.def.", "PW rst"	"Fact.def.", "PW rst", Only “Fact.defaults”, Reset deact. Table	*S.3*
If the »C« key is pressed while the device is performing a cold restart a general Reset Dialog appears on the screen. Select which options shall be available with this dialog.		

4.1.3 HMI: Values

Conf. Dev. Reset	Operation / Security / Security States
✎	*If the »C« key is pressed while the device is performing a cold restart a general Reset Dialog appears on the screen. Select which options shall be available with this dialog.*

4.2 Digital Inputs

4.2.1 DI Slot X1

4.2.1.1 DI Slot X1: Global Parameters

Nom voltage	Device Para / Digital Inputs / DI Slot X1 / Group 1	
24 VDC	24 VDC, 48 VDC, 60 VDC, 110 VDC, 230 VDC, 110 VAC, 230 VAC Table	*S.3*
Nominal voltage of the digital inputs		

Inverting 1	Device Para / Digital Inputs / DI Slot X1 / Group 1	
Inactive	Inactive, Active Table	*S.3*
Inverting the input signals.		

Debouncing time 1	Device Para / Digital Inputs / DI Slot X1 / Group 1	
no debouncing time	no debouncing time, 20 ms, 50 ms, 100 ms Table	*S.3*
A state change at the input is recognised immediately and simultaneously the debouncing timer is started. The state remains stable while the timer is running. Only after the debouncing time has elapsed is another state change accepted and the timer restarted.		

Nom voltage	Device Para / Digital Inputs / DI Slot X1 / Group 2	
24 VDC	24 VDC, 48 VDC, 60 VDC, 110 VDC, 230 VDC, 110 VAC, 230 VAC Table	*S.3*
Nominal voltage of the digital inputs		

Inverting 2	Device Para / Digital Inputs / DI Slot X1 / Group 2	
Inactive	Inactive, Active Table	*S.3*
Inverting the input signals.		

Debouncing time 2	Device Para / Digital Inputs / DI Slot X1 / Group 2	
no debouncing time	no debouncing time, 20 ms, 50 ms, 100 ms Table	*S.3*
A state change at the input is recognised immediately and simultaneously the debouncing timer is started. The state remains stable while the timer is running. Only after the debouncing time has elapsed is another state change accepted and the timer restarted.		

Nom voltage	Device Para / Digital Inputs / DI Slot X1 / Group 3	
24 VDC	24 VDC, 48 VDC, 60 VDC, 110 VDC, 230 VDC, 110 VAC, 230 VAC Table	*S.3*
Nominal voltage of the digital inputs		

Inverting 3	Device Para / Digital Inputs / DI Slot X1 / Group 3	
Inactive	Inactive, Active Table	*S.3*
Inverting the input signals.		

Debouncing time 3	Device Para / Digital Inputs / DI Slot X1 / Group 3	
no debouncing time	no debouncing time, 20 ms, 50 ms, 100 ms Table	*S.3*
A state change at the input is recognised immediately and simultaneously the debouncing timer is started. The state remains stable while the timer is running. Only after the debouncing time has elapsed is another state change accepted and the timer restarted.		

Inverting 4	Device Para / Digital Inputs / DI Slot X1 / Group 3	
Inactive	Inactive, Active Table	*S.3*
Inverting the input signals.		

Debouncing time 4	Device Para / Digital Inputs / DI Slot X1 / Group 3	
no debouncing time	no debouncing time, 20 ms, 50 ms, 100 ms Table	*S.3*
A state change at the input is recognised immediately and simultaneously the debouncing timer is started. The state remains stable while the timer is running. Only after the debouncing time has elapsed is another state change accepted and the timer restarted.		

Inverting 5	Device Para / Digital Inputs / DI Slot X1 / Group 3	
Inactive	Inactive, Active Table	*S.3*
Inverting the input signals.		

Debouncing time 5	Device Para / Digital Inputs / DI Slot X1 / Group 3	
no debouncing time	no debouncing time, 20 ms, 50 ms, 100 ms Table	*S.3*
A state change at the input is recognised immediately and simultaneously the debouncing timer is started. The state remains stable while the timer is running. Only after the debouncing time has elapsed is another state change accepted and the timer restarted.		

Inverting 6	Device Para / Digital Inputs / DI Slot X1 / Group 3	
Inactive	Inactive, Active Table	*S.3*
Inverting the input signals.		

Debouncing time 6	Device Para / Digital Inputs / DI Slot X1 / Group 3	
no debouncing time	no debouncing time, 20 ms, 50 ms, 100 ms Table	*S.3*
A state change at the input is recognised immediately and simultaneously the debouncing timer is started. The state remains stable while the timer is running. Only after the debouncing time has elapsed is another state change accepted and the timer restarted.		

Inverting 7	Device Para / Digital Inputs / DI Slot X1 / Group 3	
Inactive	Inactive, Active Table	*S.3*
Inverting the input signals.		

Debouncing time 7	Device Para / Digital Inputs / DI Slot X1 / Group 3	
no debouncing time	no debouncing time, 20 ms, 50 ms, 100 ms Table	*S.3*
A state change at the input is recognised immediately and simultaneously the debouncing timer is started. The state remains stable while the timer is running. Only after the debouncing time has elapsed is another state change accepted and the timer restarted.		

Inverting 8	Device Para / Digital Inputs / DI Slot X1 / Group 3	
Inactive	Inactive, Active Table	*S.3*
Inverting the input signals.		

Debouncing time 8	Device Para / Digital Inputs / DI Slot X1 / Group 3	
no debouncing time	no debouncing time, 20 ms, 50 ms, 100 ms Table	*S.3*
A state change at the input is recognised immediately and simultaneously the debouncing timer is started. The state remains stable while the timer is running. Only after the debouncing time has elapsed is another state change accepted and the timer restarted.		

4.2.1.2 DI Slot X1: Signals (Output States)

DI 1 **...** **DI 8**	Operation / Status Display / DI Slot X1
	Signal: Digital Input

4.3 Binary Outputs

4.3.1 BO Slot X2

Binary Output relay - BO2

4.3.1.1 BO Slot X2: Global Parameters

Operating Mode	Device Para / Binary Outputs / BO Slot X2 / BO 1	
Normally open (NO)	Normally open (NO), Normally closed (NC) Table	*S.3*
Operating Mode		

t-hold	Device Para / Binary Outputs / BO Slot X2 / BO 1	
0.00s	0.00s . . . 300.00s	*S.3*
To clearly identify the state transition of a binary output relay, the "new state" is being hold, at least for the duration of the hold time.		

t-Off Delay	Device Para / Binary Outputs / BO Slot X2 / BO 1	
0.00s	0.00s . . . 300.00s	*S.3*
Switch Off Delay		

Latched	Device Para / Binary Outputs / BO Slot X2 / BO 1	
Inactive	Inactive, Active Table	*S.3*
Defines whether the Relay Output will be latched when it picks up.		

Acknowledgement	Device Para / Binary Outputs / BO Slot X2 / BO 1	
• Only available if: Latched = Active -	- . . . Internal test state Table	*S.3*
Acknowledgement Signal - An acknowledgement signal (that acknowledges the corresponding binary output relay) can be assigned to each output relay. The acknowledgement-signal is only effective if the parameter "Latched" is set to active.		

Inverting	Device Para / Binary Outputs / BO Slot X2 / BO 1	
Inactive	Inactive, Active Table	*S.3*
Inverting of the collective signal (OR-gate/disjunction). In combination with inverted input signals an AND-gate can be programmed (Conjunction).		

Assignment 1	Device Para / Binary Outputs / BO Slot X2 / BO 1	
TripCmd	- . . . Internal test state Table	*S.3*
Assignment		

Inverting 1	Device Para / Binary Outputs / BO Slot X2 / BO 1	
Inactive	Inactive, Active Table	*S.3*
Inverting of the state of the assigned signal.		

Assignment 2	Device Para / Binary Outputs / BO Slot X2 / BO 1	
-	- . . . Internal test state Table	*S.3*
Assignment		

Inverting 2	Device Para / Binary Outputs / BO Slot X2 / BO 1	
Inactive	Inactive, Active Table	*S.3*
Inverting of the state of the assigned signal.		

Assignment 3	Device Para / Binary Outputs / BO Slot X2 / BO 1	
-	- . . . Internal test state Table	*S.3*
Assignment		

Inverting 3	Device Para / Binary Outputs / BO Slot X2 / BO 1	
Inactive	Inactive, Active Table	*S.3*
Inverting of the state of the assigned signal.		

Assignment 4	Device Para / Binary Outputs / BO Slot X2 / BO 1	
-	- . . . Internal test state Table	*S.3*
Assignment		

Inverting 4	Device Para / Binary Outputs / BO Slot X2 / BO 1	
Inactive	Inactive, Active Table	*S.3*
Inverting of the state of the assigned signal.		

Assignment 5	Device Para / Binary Outputs / BO Slot X2 / BO 1	
-	- . . . Internal test state Table	*S.3*
Assignment		

Inverting 5	Device Para / Binary Outputs / BO Slot X2 / BO 1	
Inactive	Inactive, Active Table	*S.3*
Inverting of the state of the assigned signal.		

Assignment 6	Device Para / Binary Outputs / BO Slot X2 / BO 1	
-	- . . . Internal test state Table	*S.3*
Assignment		

Inverting 6	Device Para / Binary Outputs / BO Slot X2 / BO 1	
Inactive	Inactive, Active Table	*S.3*
Inverting of the state of the assigned signal.		

Assignment 7	Device Para / Binary Outputs / BO Slot X2 / BO 1	
-	- . . . Internal test state Table	*S.3*
Assignment		

Inverting 7	Device Para / Binary Outputs / BO Slot X2 / BO 1	
Inactive	Inactive, Active Table	*S.3*
Inverting of the state of the assigned signal.		

Operating Mode	Device Para / Binary Outputs / BO Slot X2 / BO 2	
Normally open (NO)	Normally open (NO), Normally closed (NC) Table	*S.3*
Operating Mode		

t-hold	Device Para / Binary Outputs / BO Slot X2 / BO 2	
0.00s	0.00s ... 300.00s	*S.3*
To clearly identify the state transition of a binary output relay, the "new state" is being hold, at least for the duration of the hold time.		

t-Off Delay	Device Para / Binary Outputs / BO Slot X2 / BO 2	
0.00s	0.00s ... 300.00s	*S.3*
Switch Off Delay		

Latched	Device Para / Binary Outputs / BO Slot X2 / BO 2	
Inactive	Inactive, Active Table	*S.3*
Defines whether the Relay Output will be latched when it picks up.		

Acknowledgement	Device Para / Binary Outputs / BO Slot X2 / BO 2	
• Only available if: Latched = Active -	- ... Internal test state Table	*S.3*
Acknowledgement Signal - An acknowledgement signal (that acknowledges the corresponding binary output relay) can be assigned to each output relay. The acknowledgement-signal is only effective if the parameter "Latched" is set to active.		

Inverting	Device Para / Binary Outputs / BO Slot X2 / BO 2	
Inactive	Inactive, Active Table	*S.3*
Inverting of the collective signal (OR-gate/disjunction). In combination with inverted input signals an AND-gate can be programmed (Conjunction).		

Assignment 1	Device Para / Binary Outputs / BO Slot X2 / BO 2	
Alarm	- ... Internal test state Table	*S.3*
Assignment		

Inverting 1	Device Para / Binary Outputs / BO Slot X2 / BO 2	
Inactive	Inactive, Active Table	*S.3*
Inverting of the state of the assigned signal.		

Assignment 2	Device Para / Binary Outputs / BO Slot X2 / BO 2	
-	- . . . Internal test state Table	*S.3*
Assignment		

Inverting 2	Device Para / Binary Outputs / BO Slot X2 / BO 2	
Inactive	Inactive, Active Table	*S.3*
Inverting of the state of the assigned signal.		

Assignment 3	Device Para / Binary Outputs / BO Slot X2 / BO 2	
-	- . . . Internal test state Table	*S.3*
Assignment		

Inverting 3	Device Para / Binary Outputs / BO Slot X2 / BO 2	
Inactive	Inactive, Active Table	*S.3*
Inverting of the state of the assigned signal.		

Assignment 4	Device Para / Binary Outputs / BO Slot X2 / BO 2	
-	- . . . Internal test state Table	*S.3*
Assignment		

Inverting 4	Device Para / Binary Outputs / BO Slot X2 / BO 2	
Inactive	Inactive, Active Table	*S.3*
Inverting of the state of the assigned signal.		

Assignment 5	Device Para / Binary Outputs / BO Slot X2 / BO 2	
-	- . . . Internal test state Table	*S.3*
Assignment		

Inverting 5	Device Para / Binary Outputs / BO Slot X2 / BO 2	
Inactive	Inactive, Active Table	*S.3*
Inverting of the state of the assigned signal.		

Assignment 6	Device Para / Binary Outputs / BO Slot X2 / BO 2	
-	- . . . Internal test state Table	*S.3*
Assignment		

Inverting 6	Device Para / Binary Outputs / BO Slot X2 / BO 2	
Inactive	Inactive, Active Table	*S.3*
Inverting of the state of the assigned signal.		

Assignment 7	Device Para / Binary Outputs / BO Slot X2 / BO 2	
-	- . . . Internal test state Table	*S.3*
Assignment		

Inverting 7	Device Para / Binary Outputs / BO Slot X2 / BO 2	
Inactive	Inactive, Active Table	*S.3*
Inverting of the state of the assigned signal.		

Operating Mode	Device Para / Binary Outputs / BO Slot X2 / BO 3	
Normally open (NO)	Normally open (NO), Normally closed (NC) Table	*S.3*
Operating Mode		

t-hold	Device Para / Binary Outputs / BO Slot X2 / BO 3	
0.00s	0.00s ... 300.00s	*S.3*
To clearly identify the state transition of a binary output relay, the "new state" is being hold, at least for the duration of the hold time.		

t-Off Delay	Device Para / Binary Outputs / BO Slot X2 / BO 3	
0.00s	0.00s ... 300.00s	*S.3*
Switch Off Delay		

Latched	Device Para / Binary Outputs / BO Slot X2 / BO 3	
Inactive	Inactive, Active Table	*S.3*
Defines whether the Relay Output will be latched when it picks up.		

Acknowledgement	Device Para / Binary Outputs / BO Slot X2 / BO 3	
• Only available if: Latched = Active -	- ... Internal test state Table	*S.3*
Acknowledgement Signal - An acknowledgement signal (that acknowledges the corresponding binary output relay) can be assigned to each output relay. The acknowledgement-signal is only effective if the parameter "Latched" is set to active.		

Inverting	Device Para / Binary Outputs / BO Slot X2 / BO 3	
Inactive	Inactive, Active Table	*S.3*
Inverting of the collective signal (OR-gate/disjunction). In combination with inverted input signals an AND-gate can be programmed (Conjunction).		

Assignment 1	Device Para / Binary Outputs / BO Slot X2 / BO 3	
ON Cmd	- ... Internal test state Table	*S.3*
Assignment		

Inverting 1	Device Para / Binary Outputs / BO Slot X2 / BO 3	
Inactive	Inactive, Active Table	*S.3*
Inverting of the state of the assigned signal.		

Assignment 2	Device Para / Binary Outputs / BO Slot X2 / BO 3	
-	- . . . Internal test state Table	*S.3*
Assignment		

Inverting 2	Device Para / Binary Outputs / BO Slot X2 / BO 3	
Inactive	Inactive, Active Table	*S.3*
Inverting of the state of the assigned signal.		

Assignment 3	Device Para / Binary Outputs / BO Slot X2 / BO 3	
-	- . . . Internal test state Table	*S.3*
Assignment		

Inverting 3	Device Para / Binary Outputs / BO Slot X2 / BO 3	
Inactive	Inactive, Active Table	*S.3*
Inverting of the state of the assigned signal.		

Assignment 4	Device Para / Binary Outputs / BO Slot X2 / BO 3	
-	- . . . Internal test state Table	*S.3*
Assignment		

Inverting 4	Device Para / Binary Outputs / BO Slot X2 / BO 3	
Inactive	Inactive, Active Table	*S.3*
Inverting of the state of the assigned signal.		

Assignment 5	Device Para / Binary Outputs / BO Slot X2 / BO 3	
-	- . . . Internal test state Table	*S.3*
Assignment		

Inverting 5	Device Para / Binary Outputs / BO Slot X2 / BO 3	
Inactive	Inactive, Active Table	*S.3*
Inverting of the state of the assigned signal.		

Assignment 6	Device Para / Binary Outputs / BO Slot X2 / BO 3	
-	- ... Internal test state Table	*S.3*
Assignment		

Inverting 6	Device Para / Binary Outputs / BO Slot X2 / BO 3	
Inactive	Inactive, Active Table	*S.3*
Inverting of the state of the assigned signal.		

Assignment 7	Device Para / Binary Outputs / BO Slot X2 / BO 3	
-	- ... Internal test state Table	*S.3*
Assignment		

Inverting 7	Device Para / Binary Outputs / BO Slot X2 / BO 3	
Inactive	Inactive, Active Table	*S.3*
Inverting of the state of the assigned signal.		

Operating Mode	Device Para / Binary Outputs / BO Slot X2 / BO 4	
Normally open (NO)	Normally open (NO), Normally closed (NC) Table	*S.3*
Operating Mode		

t-hold	Device Para / Binary Outputs / BO Slot X2 / BO 4	
0.00s	0.00s ... 300.00s	*S.3*
To clearly identify the state transition of a binary output relay, the "new state" is being hold, at least for the duration of the hold time.		

t-Off Delay	Device Para / Binary Outputs / BO Slot X2 / BO 4	
0.00s	0.00s ... 300.00s	*S.3*
Switch Off Delay		

Latched	Device Para / Binary Outputs / BO Slot X2 / BO 4	
Inactive	Inactive, Active Table	*S.3*
Defines whether the Relay Output will be latched when it picks up.		

Acknowledgement	Device Para / Binary Outputs / BO Slot X2 / BO 4	
• Only available if: Latched = Active -	- ... Internal test state Table	*S.3*
Acknowledgement Signal - An acknowledgement signal (that acknowledges the corresponding binary output relay) can be assigned to each output relay. The acknowledgement-signal is only effective if the parameter "Latched" is set to active.		

Inverting	Device Para / Binary Outputs / BO Slot X2 / BO 4	
Inactive	Inactive, Active Table	*S.3*
Inverting of the collective signal (OR-gate/disjunction). In combination with inverted input signals an AND-gate can be programmed (Conjunction).		

Assignment 1	Device Para / Binary Outputs / BO Slot X2 / BO 4	
OFF Cmd	- ... Internal test state Table	*S.3*
Assignment		

Inverting 1	Device Para / Binary Outputs / BO Slot X2 / BO 4	
Inactive	Inactive, Active Table	*S.3*
Inverting of the state of the assigned signal.		

Assignment 2	Device Para / Binary Outputs / BO Slot X2 / BO 4	
-	- ... Internal test state Table	*S.3*
Assignment		

Inverting 2	Device Para / Binary Outputs / BO Slot X2 / BO 4	
Inactive	Inactive, Active Table	*S.3*
Inverting of the state of the assigned signal.		

Assignment 3	Device Para / Binary Outputs / BO Slot X2 / BO 4	
-	- . . . Internal test state Table	*S.3*
Assignment		

Inverting 3	Device Para / Binary Outputs / BO Slot X2 / BO 4	
Inactive	Inactive, Active Table	*S.3*
Inverting of the state of the assigned signal.		

Assignment 4	Device Para / Binary Outputs / BO Slot X2 / BO 4	
-	- . . . Internal test state Table	*S.3*
Assignment		

Inverting 4	Device Para / Binary Outputs / BO Slot X2 / BO 4	
Inactive	Inactive, Active Table	*S.3*
Inverting of the state of the assigned signal.		

Assignment 5	Device Para / Binary Outputs / BO Slot X2 / BO 4	
-	- . . . Internal test state Table	*S.3*
Assignment		

Inverting 5	Device Para / Binary Outputs / BO Slot X2 / BO 4	
Inactive	Inactive, Active Table	*S.3*
Inverting of the state of the assigned signal.		

Assignment 6	Device Para / Binary Outputs / BO Slot X2 / BO 4	
-	- . . . Internal test state Table	*S.3*
Assignment		

Inverting 6	Device Para / Binary Outputs / BO Slot X2 / BO 4	
Inactive	Inactive, Active Table	*S.3*
Inverting of the state of the assigned signal.		

Assignment 7	Device Para / Binary Outputs / BO Slot X2 / BO 4	
-	- . . . Internal test state Table	*S.3*
Assignment		

Inverting 7	Device Para / Binary Outputs / BO Slot X2 / BO 4	
Inactive	Inactive, Active Table	*S.3*
Inverting of the state of the assigned signal.		

Operating Mode	Device Para / Binary Outputs / BO Slot X2 / BO 5	
Normally open (NO)	Normally open (NO), Normally closed (NC) Table	*S.3*
Operating Mode		

t-hold	Device Para / Binary Outputs / BO Slot X2 / BO 5	
0.00s	0.00s . . . 300.00s	*S.3*
To clearly identify the state transition of a binary output relay, the "new state" is being hold, at least for the duration of the hold time.		

t-Off Delay	Device Para / Binary Outputs / BO Slot X2 / BO 5	
0.00s	0.00s . . . 300.00s	*S.3*
Switch Off Delay		

Latched	Device Para / Binary Outputs / BO Slot X2 / BO 5	
Inactive	Inactive, Active Table	*S.3*
Defines whether the Relay Output will be latched when it picks up.		

Acknowledgement	Device Para / Binary Outputs / BO Slot X2 / BO 5	
• Only available if: Latched = Active -	- . . . Internal test state Table	*S.3*
Acknowledgement Signal - An acknowledgement signal (that acknowledges the corresponding binary output relay) can be assigned to each output relay. The acknowledgement-signal is only effective if the parameter "Latched" is set to active.		

Inverting	Device Para / Binary Outputs / BO Slot X2 / BO 5	
Inactive	Inactive, Active Table	*S.3*
Inverting of the collective signal (OR-gate/disjunction). In combination with inverted input signals an AND-gate can be programmed (Conjunction).		

Assignment 1	Device Para / Binary Outputs / BO Slot X2 / BO 5	
-	- . . . Internal test state Table	*S.3*
Assignment		

Inverting 1	Device Para / Binary Outputs / BO Slot X2 / BO 5	
Inactive	Inactive, Active Table	*S.3*
Inverting of the state of the assigned signal.		

Assignment 2	Device Para / Binary Outputs / BO Slot X2 / BO 5	
-	- . . . Internal test state Table	*S.3*
Assignment		

Inverting 2	Device Para / Binary Outputs / BO Slot X2 / BO 5	
Inactive	Inactive, Active Table	*S.3*
Inverting of the state of the assigned signal.		

Assignment 3	Device Para / Binary Outputs / BO Slot X2 / BO 5	
-	- . . . Internal test state Table	*S.3*
Assignment		

Inverting 3	Device Para / Binary Outputs / BO Slot X2 / BO 5	
Inactive	Inactive, Active Table	*S.3*
Inverting of the state of the assigned signal.		

Assignment 4	Device Para / Binary Outputs / BO Slot X2 / BO 5	
-	- . . . Internal test state Table	*S.3*
Assignment		

Inverting 4	Device Para / Binary Outputs / BO Slot X2 / BO 5	
Inactive	Inactive, Active Table	*S.3*
Inverting of the state of the assigned signal.		

Assignment 5	Device Para / Binary Outputs / BO Slot X2 / BO 5	
-	- . . . Internal test state Table	*S.3*
Assignment		

Inverting 5	Device Para / Binary Outputs / BO Slot X2 / BO 5	
Inactive	Inactive, Active Table	*S.3*
Inverting of the state of the assigned signal.		

Assignment 6	Device Para / Binary Outputs / BO Slot X2 / BO 5	
-	- . . . Internal test state Table	*S.3*
Assignment		

Inverting 6	Device Para / Binary Outputs / BO Slot X2 / BO 5	
Inactive	Inactive, Active Table	*S.3*
Inverting of the state of the assigned signal.		

Assignment 7	Device Para / Binary Outputs / BO Slot X2 / BO 5	
-	- . . . Internal test state Table	*S.3*
Assignment		

Inverting 7	Device Para / Binary Outputs / BO Slot X2 / BO 5	
Inactive	Inactive, Active Table	*S.3*
Inverting of the state of the assigned signal.		

DISARMED Ctrl	Service / Test - Prot inhib. / DISARMED / BO Slot X2	
Inactive	Inactive, Active Table	*S.3*
Enables and disables the disarming of the relay outputs. This is the first step of a two step process, to inhibit the operation or the relay outputs. Please refer to "DISARMED" for the second step.		

Disarm Mode	Service / Test - Prot inhib. / DISARMED / BO Slot X2	
permanent	permanent, timeout Table	*S.3*
CAUTION! RELAYS DISARMED in order to safely perform maintenance while eliminating the risk of taking an entire process off-line. (Note: The Supervision Contact cannot be disarmed). YOU MUST ENSURE that the relays are ARMED AGAIN after maintenance.		

t-Timeout DISARM	Service / Test - Prot inhib. / DISARMED / BO Slot X2	
• Only available if: Disarm Mode = timeout 0.03s	0.00s . . . 300.00s	*S.3*
The relays will be armed again after expiring of this time.		

Force Mode	Service / Test - Prot inhib. / Force OR / BO Slot X2	
permanent	permanent, timeout ↳ Table	*S.3*

By means of this function the normal Output Relay States can be overwritten (forced) in case that the Relay is not in a disarmed state. The relays can be set from normal operation (relay works according to the assigned signals) to "force energized" or "force de-energized" state.

t-Timeout Force	Service / Test - Prot inhib. / Force OR / BO Slot X2	
• Only available if: Force Mode = timeout 0.03s	0.00s . . . 300.00s	*S.3*

The Output State will be set by force for the duration of this time. That means for the duration of this time the Output Relay does not show the state of the signals that are assigned on it.

4.3.1.2 BO Slot X2: Direct Controls

DISARMED	Service / Test - Prot inhib. / DISARMED / BO Slot X2	
Inactive	Inactive, Active ↳ Table	*S.3*

This is the second step, after the "DISARMED Ctrl" has been activated, that is required to DISARM the relay outputs. This will DISARM those output relays that are currently not latched and that are not on “hold” by a pending minimum hold time. CAUTION! RELAYS DISARMED in order to safely perform maintenance while eliminating the risk of taking an entire process off-line. (Note: Zone Interlocking and Supervision Contact cannot be disarmed). YOU MUST ENSURE that the relays are ARMED AGAIN after maintenance.

Force all Outs	Service / Test - Prot inhib. / Force OR / BO Slot X2	
Normal	Normal, De-Energized, Energized ↳ Table	*S.3*

By means of this function the normal Output Relay State can be overwritten (forced). The relay can be set from normal operation (relay works according to the assigned signals) to "force energized" or "force de-energized" state. Forcing all outputs relays of an entire assembly group is superior to forcing a single output relay.

Force OR1 **. . .** **Force OR5**	Service / Test - Prot inhib. / Force OR / BO Slot X2	
Normal	Normal, De-Energized, Energized ↳ Table	*S.3*

By means of this function the normal Output Relay State can be overwritten (forced). The relay can be set from normal operation (relay works according to the assigned signals) to "force energized" or "force de-energized" state.

4.3.1.3 BO Slot X2: Signals (Output States)

BO 1 **...** **BO 5**	Operation / Status Display / BO Slot X2
⇧	*Signal: Binary Output Relay*

DISARMED!	Operation / Status Display / BO Slot X2
⇧	*Signal: CAUTION! RELAYS DISARMED in order to safely perform maintenance while eliminating the risk of taking an entire process off-line. (Note: The Self Supervision Contact cannot be disarmed). YOU MUST ENSURE that the relays are ARMED AGAIN after maintenance*

Outs forced	Operation / Status Display / BO Slot X2
⇧	*Signal: The State of at least one Relay Output has been set by force. That means that the state of at least one Relay is forced and hence does not show the state of the assigned signals.*

4.4 LEDs

4.4.1 LEDs group A

LEDs at the left side of the display

4.4.1.1 LEDs group A: Global Parameters

Latched	Device Para / LEDs / LED 1	
Inactive	Inactive, Active, active, ack. by alarm Table	*S.3*
Defines whether the LED will be latched when it picks up.		

Ack signal	Device Para / LEDs / LED 1	
• Only available if: Latched = Active -	- . . . Internal test state Table	*S.3*
Acknowledgement signal for the LED. If latching is set to active the LED can only be acknowledged if those signals that initiated the setting are no longer present.		

LED active color	Device Para / LEDs / LED 1	
green	green, red, red flash, green flash, - Table	*S.3*
The LED lights up in this color if the state of the OR-assignment of the signals is true.		

LED inactive color	Device Para / LEDs / LED 1	
-	green, red, red flash, green flash, - Table	*S.3*
The LED lights up in this color if the state of the OR-assignment of the signals is untrue.		

Assignment 1	Device Para / LEDs / LED 1	
Active	- . . . Internal test state Table	*S.3*
Assignment		

Inverting 1	Device Para / LEDs / LED 1	
Inactive	Inactive, Active Table	*S.3*
Inverting of the state of the assigned signal.		

Assignment 2	Device Para / LEDs / LED 1	
-	- . . . Internal test state Table	*S.3*
Assignment		

Inverting 2	Device Para / LEDs / LED 1	
Inactive	Inactive, Active Table	*S.3*
Inverting of the state of the assigned signal.		

Assignment 3	Device Para / LEDs / LED 1	
-	- . . . Internal test state Table	*S.3*
Assignment		

Inverting 3	Device Para / LEDs / LED 1	
Inactive	Inactive, Active Table	*S.3*
Inverting of the state of the assigned signal.		

Assignment 4	Device Para / LEDs / LED 1	
-	- . . . Internal test state Table	*S.3*
Assignment		

Inverting 4	Device Para / LEDs / LED 1	
Inactive	Inactive, Active Table	*S.3*
Inverting of the state of the assigned signal.		

Assignment 5	Device Para / LEDs / LED 1	
-	- . . . Internal test state Table	*S.3*
Assignment		

Inverting 5	Device Para / LEDs / LED 1	
Inactive	Inactive, Active Table	*S.3*
Inverting of the state of the assigned signal.		

Latched	Device Para / LEDs / LED 2	
Active	Inactive, Active, active, ack. by alarm Table	*S.3*
Defines whether the LED will be latched when it picks up.		

Ack signal	Device Para / LEDs / LED 2	
• Only available if: Latched = Active -	- . . . Internal test state Table	*S.3*
Acknowledgement signal for the LED. If latching is set to active the LED can only be acknowledged if those signals that initiated the setting are no longer present.		

LED active color	Device Para / LEDs / LED 2	
red	green, red, red flash, green flash, - Table	*S.3*
The LED lights up in this color if the state of the OR-assignment of the signals is true.		

LED inactive color	Device Para / LEDs / LED 2	
-	green, red, red flash, green flash, - Table	*S.3*
The LED lights up in this color if the state of the OR-assignment of the signals is untrue.		

Assignment 1	Device Para / LEDs / LED 2	
TripCmd	- . . . Internal test state Table	*S.3*
Assignment		

Inverting 1	Device Para / LEDs / LED 2	
Inactive	Inactive, Active Table	*S.3*
Inverting of the state of the assigned signal.		

Assignment 2	Device Para / LEDs / LED 2	
-	- . . . Internal test state Table	*S.3*
Assignment		

Inverting 2	Device Para / LEDs / LED 2	
Inactive	Inactive, Active Table	*S.3*
Inverting of the state of the assigned signal.		

Assignment 3	Device Para / LEDs / LED 2	
-	- . . . Internal test state Table	*S.3*
Assignment		

Inverting 3	Device Para / LEDs / LED 2	
Inactive	Inactive, Active Table	*S.3*
Inverting of the state of the assigned signal.		

Assignment 4	Device Para / LEDs / LED 2	
-	- . . . Internal test state Table	*S.3*
Assignment		

Inverting 4	Device Para / LEDs / LED 2	
Inactive	Inactive, Active Table	*S.3*
Inverting of the state of the assigned signal.		

Assignment 5	Device Para / LEDs / LED 2	
-	- . . . Internal test state Table	*S.3*
Assignment		

Inverting 5	Device Para / LEDs / LED 2	
Inactive	Inactive, Active Table	*S.3*
Inverting of the state of the assigned signal.		

Latched	Device Para / LEDs / LED 3	
Inactive	Inactive, Active, active, ack. by alarm Table	*S.3*
Defines whether the LED will be latched when it picks up.		

Ack signal	Device Para / LEDs / LED 3	
• Only available if: Latched = Active -	- . . . Internal test state Table	*S.3*
Acknowledgement signal for the LED. If latching is set to active the LED can only be acknowledged if those signals that initiated the setting are no longer present.		

LED active color	Device Para / LEDs / LED 3	
red flash	green, red, red flash, green flash, - Table	*S.3*
The LED lights up in this color if the state of the OR-assignment of the signals is true.		

LED inactive color	Device Para / LEDs / LED 3	
-	green, red, red flash, green flash, - Table	*S.3*
The LED lights up in this color if the state of the OR-assignment of the signals is untrue.		

Assignment 1	Device Para / LEDs / LED 3	
Alarm	- . . . Internal test state Table	*S.3*
Assignment		

Inverting 1	Device Para / LEDs / LED 3	
Inactive	Inactive, Active Table	*S.3*
Inverting of the state of the assigned signal.		

Assignment 2	Device Para / LEDs / LED 3	
-	- . . . Internal test state Table	*S.3*
Assignment		

Inverting 2	Device Para / LEDs / LED 3	
Inactive	Inactive, Active Table	*S.3*
Inverting of the state of the assigned signal.		

Assignment 3	Device Para / LEDs / LED 3	
-	- . . . Internal test state Table	*S.3*
Assignment		

Inverting 3	Device Para / LEDs / LED 3	
Inactive	Inactive, Active Table	*S.3*
Inverting of the state of the assigned signal.		

Assignment 4	Device Para / LEDs / LED 3	
-	- . . . Internal test state Table	*S.3*
Assignment		

Inverting 4	Device Para / LEDs / LED 3	
Inactive	Inactive, Active Table	*S.3*
Inverting of the state of the assigned signal.		

Assignment 5	Device Para / LEDs / LED 3	
-	- . . . Internal test state Table	*S.3*
Assignment		

Inverting 5	Device Para / LEDs / LED 3	
Inactive	Inactive, Active Table	*S.3*
Inverting of the state of the assigned signal.		

Latched	Device Para / LEDs / LED 4	
Inactive	Inactive, Active, active, ack. by alarm Table	*S.3*
Defines whether the LED will be latched when it picks up.		

Ack signal	Device Para / LEDs / LED 4	
• Only available if: Latched = Active -	- . . . Internal test state Table	*S.3*
Acknowledgement signal for the LED. If latching is set to active the LED can only be acknowledged if those signals that initiated the setting are no longer present.		

LED active color	Device Para / LEDs / LED 4	
red	green, red, red flash, green flash, - Table	*S.3*
The LED lights up in this color if the state of the OR-assignment of the signals is true.		

LED inactive color	Device Para / LEDs / LED 4	
-	green, red, red flash, green flash, - Table	*S.3*
The LED lights up in this color if the state of the OR-assignment of the signals is untrue.		

Assignment 1	Device Para / LEDs / LED 4	
-	- . . . Internal test state Table	*S.3*
Assignment		

Inverting 1	Device Para / LEDs / LED 4	
Inactive	Inactive, Active Table	*S.3*
Inverting of the state of the assigned signal.		

Assignment 2	Device Para / LEDs / LED 4	
-	- . . . Internal test state Table	*S.3*
Assignment		

Inverting 2	Device Para / LEDs / LED 4	
Inactive	Inactive, Active Table	*S.3*
Inverting of the state of the assigned signal.		

Assignment 3	Device Para / LEDs / LED 4	
-	- . . . Internal test state Table	*S.3*
Assignment		

Inverting 3	Device Para / LEDs / LED 4	
Inactive	Inactive, Active Table	*S.3*
Inverting of the state of the assigned signal.		

Assignment 4	Device Para / LEDs / LED 4	
-	- . . . Internal test state Table	*S.3*
Assignment		

Inverting 4	Device Para / LEDs / LED 4	
Inactive	Inactive, Active Table	*S.3*
Inverting of the state of the assigned signal.		

Assignment 5	Device Para / LEDs / LED 4	
-	- . . . Internal test state Table	*S.3*
Assignment		

Inverting 5	Device Para / LEDs / LED 4	
Inactive	Inactive, Active Table	*S.3*
Inverting of the state of the assigned signal.		

Latched	Device Para / LEDs / LED 5	
Inactive	Inactive, Active, active, ack. by alarm Table	*S.3*
Defines whether the LED will be latched when it picks up.		

Ack signal	Device Para / LEDs / LED 5	
• Only available if: Latched = Active -	- . . . Internal test state Table	*S.3*
Acknowledgement signal for the LED. If latching is set to active the LED can only be acknowledged if those signals that initiated the setting are no longer present.		

LED active color	Device Para / LEDs / LED 5	
red	green, red, red flash, green flash, - Table	*S.3*
The LED lights up in this color if the state of the OR-assignment of the signals is true.		

LED inactive color	Device Para / LEDs / LED 5	
-	green, red, red flash, green flash, - Table	*S.3*
The LED lights up in this color if the state of the OR-assignment of the signals is untrue.		

Assignment 1	Device Para / LEDs / LED 5	
-	- . . . Internal test state Table	*S.3*
Assignment		

Inverting 1	Device Para / LEDs / LED 5	
Inactive	Inactive, Active Table	*S.3*
Inverting of the state of the assigned signal.		

Assignment 2	Device Para / LEDs / LED 5	
-	- . . . Internal test state Table	*S.3*
Assignment		

Inverting 2	Device Para / LEDs / LED 5	
Inactive	Inactive, Active Table	*S.3*
Inverting of the state of the assigned signal.		

Assignment 3	Device Para / LEDs / LED 5	
-	- . . . Internal test state Table	*S.3*
Assignment		

Inverting 3	Device Para / LEDs / LED 5	
Inactive	Inactive, Active Table	*S.3*
Inverting of the state of the assigned signal.		

Assignment 4	Device Para / LEDs / LED 5	
-	- . . . Internal test state Table	*S.3*
Assignment		

Inverting 4	Device Para / LEDs / LED 5	
Inactive	Inactive, Active Table	*S.3*
Inverting of the state of the assigned signal.		

Assignment 5	Device Para / LEDs / LED 5	
-	- . . . Internal test state Table	*S.3*
Assignment		

Inverting 5	Device Para / LEDs / LED 5	
Inactive	Inactive, Active Table	*S.3*
Inverting of the state of the assigned signal.		

Latched	Device Para / LEDs / LED 6	
Inactive	Inactive, Active, active, ack. by alarm Table	*S.3*
Defines whether the LED will be latched when it picks up.		

Ack signal	Device Para / LEDs / LED 6	
• Only available if: Latched = Active -	- . . . Internal test state Table	*S.3*
Acknowledgement signal for the LED. If latching is set to active the LED can only be acknowledged if those signals that initiated the setting are no longer present.		

LED active color	Device Para / LEDs / LED 6	
red	green, red, red flash, green flash, - Table	*S.3*
The LED lights up in this color if the state of the OR-assignment of the signals is true.		

LED inactive color	Device Para / LEDs / LED 6	
-	green, red, red flash, green flash, - Table	*S.3*
The LED lights up in this color if the state of the OR-assignment of the signals is untrue.		

Assignment 1	Device Para / LEDs / LED 6	
-	- . . . Internal test state Table	*S.3*
Assignment		

Inverting 1	Device Para / LEDs / LED 6	
Inactive	Inactive, Active Table	*S.3*
Inverting of the state of the assigned signal.		

Assignment 2	Device Para / LEDs / LED 6	
-	- . . . Internal test state Table	*S.3*
Assignment		

Inverting 2	Device Para / LEDs / LED 6	
Inactive	Inactive, Active Table	*S.3*
Inverting of the state of the assigned signal.		

Assignment 3	Device Para / LEDs / LED 6	
-	- . . . Internal test state Table	*S.3*
Assignment		

Inverting 3	Device Para / LEDs / LED 6	
Inactive	Inactive, Active Table	*S.3*
Inverting of the state of the assigned signal.		

Assignment 4	Device Para / LEDs / LED 6	
-	- . . . Internal test state Table	*S.3*
Assignment		

Inverting 4	Device Para / LEDs / LED 6	
Inactive	Inactive, Active Table	*S.3*
Inverting of the state of the assigned signal.		

Assignment 5	Device Para / LEDs / LED 6	
-	- . . . Internal test state Table	*S.3*
Assignment		

Inverting 5	Device Para / LEDs / LED 6	
Inactive	Inactive, Active Table	*S.3*
Inverting of the state of the assigned signal.		

Latched	Device Para / LEDs / LED 7	
Inactive	Inactive, Active, active, ack. by alarm Table	*S.3*
Defines whether the LED will be latched when it picks up.		

Ack signal	Device Para / LEDs / LED 7	
• Only available if: Latched = Active -	- . . . Internal test state Table	*S.3*
Acknowledgement signal for the LED. If latching is set to active the LED can only be acknowledged if those signals that initiated the setting are no longer present.		

LED active color	Device Para / LEDs / LED 7	
red	green, red, red flash, green flash, - Table	*S.3*
The LED lights up in this color if the state of the OR-assignment of the signals is true.		

LED inactive color	Device Para / LEDs / LED 7	
-	green, red, red flash, green flash, - Table	*S.3*
The LED lights up in this color if the state of the OR-assignment of the signals is untrue.		

Assignment 1	Device Para / LEDs / LED 7	
-	- . . . Internal test state Table	*S.3*
Assignment		

Inverting 1	Device Para / LEDs / LED 7	
Inactive	Inactive, Active Table	*S.3*
Inverting of the state of the assigned signal.		

Assignment 2	Device Para / LEDs / LED 7	
-	- . . . Internal test state Table	*S.3*
Assignment		

Inverting 2	Device Para / LEDs / LED 7	
Inactive	Inactive, Active Table	*S.3*
Inverting of the state of the assigned signal.		

Assignment 3	Device Para / LEDs / LED 7	
-	- . . . Internal test state Table	*S.3*
Assignment		

Inverting 3	Device Para / LEDs / LED 7	
Inactive	Inactive, Active Table	*S.3*
Inverting of the state of the assigned signal.		

Assignment 4	Device Para / LEDs / LED 7	
-	- . . . Internal test state Table	*S.3*
Assignment		

Inverting 4	Device Para / LEDs / LED 7	
Inactive	Inactive, Active Table	*S.3*
Inverting of the state of the assigned signal.		

Assignment 5	Device Para / LEDs / LED 7	
-	- . . . Internal test state Table	*S.3*
Assignment		

Inverting 5	Device Para / LEDs / LED 7	
Inactive	Inactive, Active Table	*S.3*
Inverting of the state of the assigned signal.		

5 Security

- Modbus . Smart view via Modbus
- Ctrl . Switching Authority
- HMI . Conf. Dev. Reset
- HMI . t-max Edit/Access
- HMI . Conf. Dev. Reset
- Modbus . Smart view via Modbus

5.1 Syslog

Module for sending (device-internal) log messages to some server computer via network (UDP/IP)

5.1.1 Syslog: Device Planning Parameters

Mode	Device planning / Projected Elements	
-	-, use Table	*S.3*
Syslog [Module for sending (device-internal) log messages to some server computer via network (UDP/IP)], general operation mode		

5.1.2 Syslog: Global Parameters

Function	Device Para / Security / Syslog	
Inactive	Inactive, Active Table	*S.3*
Permanent activation or deactivation of module/stage.		

IP port number	Device Para / Security / Syslog	
514	1 . . . 65535	*S.3*
IP port number. *This is the port on which the Syslog server computer listens and receives log messages. (Since the default, port 514, is a general protocol standard it is recommended to keep this default, unless there are network-related or security-related reasons against it.)*		

IP address, part 1 **. . .** **IP address, part 4**	Device Para / Security / Syslog	
0	0 . . . 255	*S.3*
IP address (IPv4) of the Syslog server computer, that receives the log messages. *IP1.IP2.IP3.IP4*		

5.1.3 Syslog: Signals (Output States)

Active	Operation / Status Display / Syslog
Signal: active	

6 System

System

Messages	
	Internal messages This item represents a special dialog. (See the Technical Manual for details.)

6.1 Sys: Global Parameters

PSet-Switch	Protection Para / PSet-Switch	
PS1	PS1, PS2, PS3, PS4, PSS via Inp fct, PSS via Scada Table	*P.2*
	Switching Parameter Set	

PS1: activated by ... PS4: activated by	Protection Para / PSet-Switch	
• Only available if: PSet-Switch = PSS via Inp fct -	- ... Maint Mode Inactive Table	*P.2*
	This Setting Group will be the active one if: The Parameter Setting Group Switch is set to "Switch via Input" and the other three input functions are inactive at the same time. In case that there is more than one input function active, no Parameter Setting Group Switch will be executed. In case all input functions are inactive, the device will keep working with the Setting Group that was activated lastly.	

Ack via »C« key	Device Para / Acknowledge	
Ack LEDs w/o passw.	Nothing, Ack LEDs w/o passw., Ack LEDs, Ack LEDs and relays, Ack Everything Table	*P.2*
	Select which acknowledgeable elements can be reset via pressing the »C« key.	

Remote Reset	Device Para / Acknowledge	
Active	Inactive, Active Table	*P.2*
	Enables or disables the option to acknowledge from external/remote via signals (assignments) and SCADA.	

Ack LED	Device Para / Acknowledge	
• Only available if: Remote Reset = Active -	- . . . Internal test state Table	*S.3*
All acknowledgeable LEDs will be acknowledged if the state of the assigned signal becomes true.		

Ack BO	Device Para / Acknowledge	
• Only available if: Remote Reset = Active -	- . . . Internal test state Table	*S.3*
All acknowledgeable binary output relays will be acknowledged if the state of the assigned signal becomes true.		

Ack Scada	Device Para / Acknowledge	
• Only available if: Remote Reset = Active -	- . . . Internal test state Table	*S.3*
Latched SCADA signals are acknowledged if the state of the assigned signal becomes true.		

Scaling	Device Para / Measurem Display / General Settings	
Per unit values	Per unit values, Primary values, Secondary values Table	*S.3*
Display of the measured values as primary, secondary or per unit values		

Maint Mode	Service / Maint Mode	
Inactive	Inactive, Activation Manually, Activation via SCADA, Activation via DI Table	*S.3*
Activation Mode of the Arc Flash Reduction. Switching into another mode is only possible when no Activation Signal is active (pending).		

Maint Mode Activated by	Service / Maint Mode	
• Only available if: Maint Mode = Activation via DI -	- . . . LE80.Out inverted Table	*S.3*
Activation Signal for the Arc Flash Reduction Maintenance Switch		

Setting Lock	Field Para / General Settings	
-	- . . . Internal test state Table	*P.2*
No parameters can be changed as long as this input is true. The parameter settings are locked.		

6.2 Sys: Direct Controls

Ack BO LED Scd Trips	Operation / Acknowledge	
Inactive	Inactive, Active Table	*P.1*
Acknowledge (reset) latched binary output relays, LEDs, SCADA and Trips.		

Ack LED	Operation / Acknowledge	
Inactive	Inactive, Active Table	*P.1*
All acknowledgeable LEDs will be acknowledged.		

Ack BO	Operation / Acknowledge	
Inactive	Inactive, Active Table	*P.1*
All acknowledgeable binary output relays are acknowledged.		

Ack Scada	Operation / Acknowledge	
• Only available if: Protocol ≠ - Inactive	Inactive, Active Table	*P.1*
Latched SCADA signals are acknowledged.		

Reboot	Service / General	
no	no, yes Table	*S.3*
Rebooting the device.		

Setting Lock Bypass	Field Para / General Settings	
Inactive	Inactive, Active Table	*P.1*
Short-period unlock of the Setting Lock		

Reset-FADC	Service / Diagnostic Data / FADC	
Inactive	Inactive, Active Table	*P.1*
Reset: FADC-Counter		

6.3 Sys: Input States

Ack LED-I	Operation / Status Display / Sys
Module input state: LEDs acknowledgement by digital input	

Ack BO-I	Operation / Status Display / Sys
Module input state: Acknowledgement of the binary Output Relays	

Ack Scada-I	Operation / Status Display / Sys
• Only available if: Protocol ≠ - *Module input state: Acknowledge latched SCADA signals.*	

PS1-I **...** **PS4-I**	Operation / Status Display / Sys
State of the module input respectively of the signal, that should activate this Parameter Setting Group.	

Setting Lock-I **(Sys . Setting Lock)**	Operation / Status Display / Sys
State of the module input: No parameters can be changed as long as this input is true. The parameter settings are locked.	

Maint Mode-I	Operation / Status Display / Sys
Module Input State: Arc Flash Reduction Maintenance Switch	

6.4 Sys: Signals (Output States)

Reboot	Operation / Status Display / Sys
Signal: Rebooting the device. *Device Start-up Codes: 1=Normal Start-up; 2=Reboot by the Operator; 3=Reboot by means of Super Reset; 4=outdated; 5=outdated; 6=Unknown Error Source; 7=Forced Reboot (initiated by the main processor); 8=Exceeded Time Limit of the Protection Cycle; 9= Forced Reboot (initiated by the digital signal processor); 10=Exceeded Time Limit of the Measured Value Processing; 11=Sags of the Supply Voltage; 12=Illegal Memory Access.*	

Act Set	Operation / Status Display / Sys Protection Para / PSet-Switch
⇧	*Signal: Active Parameter Set*

PS 1	Operation / Status Display / Sys
⇧	*Signal: The currently active Parameter Set is PS 1*

PS 2	Operation / Status Display / Sys
⇧	*Signal: The currently active Parameter Set is PS 2*

PS 3	Operation / Status Display / Sys
⇧	*Signal: The currently active Parameter Set is PS 3*

PS 4	Operation / Status Display / Sys
⇧	*Signal: The currently active Parameter Set is PS 4*

PSS manual	Operation / Status Display / Sys
⇧	*Signal: Manual Switch over of a Parameter Set*

PSS via Scada	Operation / Status Display / Sys
⇧	• Only available if: Protocol ≠ - *Signal: Parameter Set Switch via Scada. Write into this output byte the integer of the parameter set that should become active (e.g. 4 => Switch onto parameter set 4).*

PSS via Inp fct	Operation / Status Display / Sys
⇧	*Signal: Parameter Set Switch via input function*

min 1 param changed	Operation / Status Display / Sys
⇧	*Signal: At least one parameter has been changed*

Setting Lock Bypass	Operation / Status Display / Sys
⇧	*Signal: Short-period unlock of the Setting Lock*

Maint Mode Active	Operation / Status Display / Sys
⇧	*Signal: Arc Flash Reduction Maintenance Active*

Maint Mode Inactive	Operation / Status Display / Sys
⇧	*Signal: Arc Flash Reduction Maintenance Inactive*

MaintMode Manually	Operation / Status Display / Sys
⇧	*Signal: Arc Flash Reduction Maintenance Manual Mode*

Maint Mode SCADA	Operation / Status Display / Sys
⇧	*Signal: Arc Flash Reduction Maintenance SCADA Mode*

Maint Mode DI	Operation / Status Display / Sys
⇧	*Signal: Arc Flash Reduction Maintenance Digital Input Mode*

Ack LED	Operation / Status Display / Sys
⇧	*Signal: LEDs acknowledgement*

Ack BO	Operation / Status Display / Sys
⇧	*Signal: Acknowledgement of the Binary Outputs*

Ack Scada	Operation / Status Display / Sys
⇧	• Only available if: Protocol ≠ - *Signal: Acknowledge latched SCADA signals*

Ack TripCmd	Operation / Status Display / Sys
⇧	*Signal: Reset Trip Command*

Ack LED-HMI	Operation / Status Display / Sys
⇧	*Signal: LEDs acknowledgement, triggered at the HMI*

Ack BO-HMI	Operation / Status Display / Sys
⇧	*Signal: Acknowledgement of the Binary Outputs, triggered at the HMI*

Ack Scada-HMI	Operation / Status Display / Sys
⇧	• Only available if: Protocol ≠ - *Signal: Acknowledge latched SCADA signals, triggered at the HMI*

Ack TripCmd-HMI	Operation / Status Display / Sys
⇧	*Signal: Reset Trip Command, triggered at the HMI*

Ack LED-Sca	Operation / Status Display / Sys

- Only available if: Protocol ≠ -

Signal: LEDs acknowledgement, triggered via SCADA

Ack BO-Sca	Operation / Status Display / Sys

- Only available if: Protocol ≠ -

Signal: Acknowledgement of the Binary Outputs, triggered via SCADA

Ack Counter-Sca	Operation / Status Display / Sys

- Only available if: Protocol ≠ -

Signal: Reset of all Counters, triggered via SCADA

Ack Scada-Sca	Operation / Status Display / Sys

- Only available if: Protocol ≠ -

Signal: Acknowledge latched SCADA signals, triggered via SCADA

Ack TripCmd-Sca	Operation / Status Display / Sys

- Only available if: Protocol ≠ -

Signal: Reset Trip Command, triggered via SCADA

Res OperationsCr	Operation / Status Display / Sys

Signal:: Res OperationsCr

Res AlarmCr	Operation / Status Display / Sys

Signal:: Res AlarmCr

Res TripCmdCr	Operation / Status Display / Sys

Signal:: Res TripCmdCr

Res TotalCr	Operation / Status Display / Sys

Signal:: Res TotalCr

6.5 Sys: Values

Bootloader Build	Device Para / Version
	Build number of the bootloader

Build	Device Para / Version
	Build Number

SW version	Device Para / Version
	Version of the device firmware

CAT No	Device Para / Version
	»CAT No.«, Order Code as printed on the nameplate of the device.

REV.	Device Para / Version
	Revision (as printed on the nameplate of the device).

S/N	Device Para / Version
	The serial number of the device.

DM version	Device Para / Version
	Version of the device model

Operating hours Cr	Operation / Count and RevData / Sys
	Operating hours counter of the protective device

FADC_TR	Service / Diagnostic Data / FADC
	FADC_TR: total (retain)

FADC_LR	Service / Diagnostic Data / FADC
	FADC-LR: long (10min, max, retain)

FADC_MR	Service / Diagnostic Data / FADC
	FADC-MR: mid (10s, max, retain)

FADC_SR	Service / Diagnostic Data / FADC
	FADC-SR: short(0.2s, max, retain)

FADC_LM	Service / Diagnostic Data / FADC
	FADC-LM: long (10min, max, since reset

FADC_MM	Service / Diagnostic Data / FADC
	FADC-MM: mid (10s, max, since reset

FADC_SM	Service / Diagnostic Data / FADC
	FADC-SM: short (0.2s, max, since reset)

FADC_L	Service / Diagnostic Data / FADC
	FADC-L: long (10mmin)

FADC_M	Service / Diagnostic Data / FADC
	FADC-M: mid (10s)

FADC_S	Service / Diagnostic Data / FADC
	FADC-S: short (0.2s)

6.6 Sys

System

Security Logger	
	Security-related messages This item represents a special dialog. (See the Technical Manual for details.)

Password	
	Changing the password This item represents a special dialog. (See the Technical Manual for details.)

Access Level	
	Access Level This item represents a special dialog. (See the Technical Manual for details.)

6.6.1 Sys: Direct Controls

Smart view via USB	Device Para / Security / Communication	
Active	Inactive, Active Table	*S.3*
	Activate (allow) or inactivate (disallow) the Smart view access via the USB interface.	

Smart view via Eth	Device Para / Security / Communication	
Active	Inactive, Active Table	*S.3*
	Activate (allow) or inactivate (disallow) the Smart view access via the Ethernet interface.	

6.6.2 Sys: Values

Smart view via USB	Operation / Security / Security States
	Information whether or not the Smart view access via the USB interface is activated (allowed).

Smart view via Eth	Operation / Security / Security States
	Information whether or not the Smart view access via the Ethernet interface is activated (allowed).

TLS Certificate	Operation / Security / Security States
	Type of certificate that the device uses for the encrypted communication. This value is directly related to the security-level of the communication.

Passw.remote net.conn.	Operation / Security / Security States
	Type / Security-level of the connection password that is used for a Smart view connection via some network interface.

Passw. for USB conn.	Operation / Security / Security States
	Type / Security-level of the connection password that is used for a USB connection.

6.7 TimeSync

Time synchronisation

Date and Time	
	(Re-)setting Date and Time This item represents a special dialog. (See the Technical Manual for details.)

6.7.1 TimeSync: Global Parameters

DST offset	Device Para / Time / Timezone	
60min	-180min ... 180min	*S.3*
	Difference to wintertime	

DST manual	Device Para / Time / Timezone	
Active	Inactive, Active ↳ Table	*S.3*
	Manual setting of the Daylight Saving Time	

Summertime	Device Para / Time / Timezone	
• Only available if: DST manual = Active Inactive	Inactive, Active ↳ Table	*S.3*
	Daylight Saving Time	

Summertime m	Device Para / Time / Timezone	
• Only available if: DST manual = Inactive March	January ... December ↳ Table	*S.3*
	Month of clock change summertime	

Summertime d	Device Para / Time / Timezone	
• Only available if: DST manual = Inactive Sunday	Sunday ... General day ↳ Table	*S.3*
	Day of clock change summertime	

Summertime w	Device Para / Time / Timezone	
• Only available if: DST manual = Inactive Last	First, Second, Third, Fourth, Last Table	*S.3*
Place of selected day in month (for clock change summertime)		

Summertime h	Device Para / Time / Timezone	
• Only available if: DST manual = Inactive 2h	0h ... 23h	*S.3*
Hour of clock change summertime		

Summertime min	Device Para / Time / Timezone	
• Only available if: DST manual = Inactive 0min	0min ... 59min	*S.3*
Minute of clock change summertime		

Wintertime m	Device Para / Time / Timezone	
• Only available if: DST manual = Inactive October	January ... December Table	*S.3*
Month of clock change wintertime		

Wintertime d	Device Para / Time / Timezone	
• Only available if: DST manual = Inactive Sunday	Sunday ... General day Table	*S.3*
Day of clock change wintertime		

Wintertime w	Device Para / Time / Timezone	
• Only available if: DST manual = Inactive Last	First, Second, Third, Fourth, Last Table	*S.3*
Place of selected day in month (for clock change wintertime)		

Wintertime h	Device Para / Time / Timezone	
• Only available if: DST manual = Inactive 3h	0h ... 23h	*S.3*
Hour of clock change wintertime		

Wintertime min	Device Para / Time / Timezone	
• Only available if: DST manual = Inactive 0min	0min ... 59min	*S.3*
Minute of clock change wintertime		

Time Zones	Device Para / Time / Timezone	
UTC+0 London	UTC+14 Kiritimati ... UTC-11 Midway Islands Table	*S.3*
Time Zones		

TimeSync	Device Para / Time / TimeSync / TimeSync	
-	- ... PTP Table	*S.3*
Time synchronisation		

6.7.2 TimeSync: Signals (Output States)

synchronized	Operation / Status Display / TimeSync / TimeSync
Clock is synchronized.	

7 Communication

7.1 Scada: Device Planning Parameters

Protocol	Device planning / Projected Elements	
-	- . . . Profibus Table	*S.3*
Select the SCADA protocol to be used.		

7.2 Scada: Signals (Output States)

SCADA connected	Operation / Status Display / Scada
At least one SCADA System is connected to the device.	

SCADA not connected	Operation / Status Display / Scada
No SCADA System is connected to the device	

7.3 TcpIp

TCP/IP config	
configuration of the TCP/IP protocol This item represents a special dialog. (See the Technical Manual for details.)	

7.3.1 TcpIp: Global Parameters

Keep Alive Time	Device Para / TCP/IP / Advanced Settings	
720s	1s ... 7200s	*S.3*
Keep Alive Time is the duration between two keep alive transmissions in idle condition		

Keep Alive Interval	Device Para / TCP/IP / Advanced Settings	
15s	1s ... 60s	*S.3*
Keep Alive Interval is the duration between two successive keep alive retransmissions, if the acknowledgement to the previous keepalive transmission was not received.		

Keep Alive Retry	Device Para / TCP/IP / Advanced Settings	
3	3 ... 3	*S.3*
Keep alive retry is the number of retransmissions to be carried out before declaring that the remote end is not available.		

7.4 DNP3

Distributed Network Protocol

7.4.1 DNP3: Global Parameters

Function	Device Para / DNP3 / Communication	
Inactive	Inactive, Active Table	*S.3*
Permanent activation or deactivation of module/stage.		

IP Port Number	Device Para / DNP3 / Communication	
Only available if: • Protocol = DNP3 TCP • Protocol = DNP3 UDP 20000	0 ... 65535	*S.3*
IP Port Number. *In general it is recommended to keep the default value. If this is not possible then select a number out of the private range 49152-52151 or 52164-65535 that is not yet in use within your network.*		

Baud rate	Device Para / DNP3 / Communication	
• Only available if: Protocol = DNP3 RTU 19200	1200 ... 115200 Table	*S.3*
Baud rate for communication		

Frame Layout	Device Para / DNP3 / Communication	
• Only available if: Protocol = DNP3 RTU 8E1	8E1, 8O1, 8N1, 8N2 Table	*S.3*
Frame Layout		

Optical rest position	Device Para / DNP3 / Communication	
Light on	Light off, Light on Table	*S.3*
Optical rest position		

SelfAddress	Device Para / DNP3 / Communication	
Inactive	Inactive, Active Table	*S.3*
Support of self (automatic) addresses		

DataLink confirm	Device Para / DNP3 / Communication	
Never	Never, Always, On_Large Table	*S.3*
Enables or disables the data layer confirmation (ack).		

t-DataLink confirm	Device Para / DNP3 / Communication	
1s	0.1s ... 10.0s	*S.3*
Data layer confirmation timeout		

DataLink num retries	Device Para / DNP3 / Communication	
3	0 ... 255	*S.3*
Number of repetition of data link packet sending after failing		

Direction Bit	Device Para / DNP3 / Communication	
Inactive	Inactive, Active Table	*S.3*
Enables Direction Bit functionality. The Direction Bit is 0 for SlaveStation and 1 for MasterStation		

Max Frame Size	Device Para / DNP3 / Communication	
255	64 ... 255	*S.3*
This value is used to limit the net Frame Size		

Test Link Period	Device Para / DNP3 / Communication	
0s	0.0s ... 120.0s	*S.3*
This value specifies the time period when to send a Test Link-Frame		

AppLink confirm	Device Para / DNP3 / Communication	
Always	Never, Always, Event Table	*S.3*
Determines if the device will request that the Application Layer response be confirmed or not		

t-AppLink confirm	Device Para / DNP3 / Communication	
5s	0.1s ... 10.0s	*S.3*
Application layer response timeout		

AppLink num retries	Device Para / DNP3 / Communication	
0	0 ... 255	*S.3*
The number of times the device will retransmit an Application Layer fragment		

Unsol Reporting	Device Para / DNP3 / Communication	
Inactive	Inactive, Active Table	*S.3*
Enables unsolicited reporting. This is available only for DNP3 TCP connections, and for DNP3 RTU in case of a peer-to-peer connection.		

Unsol Reporting Timeout	Device Para / DNP3 / Communication	
• Only available if: Protocol ≠ DNP3 UDP 10s	1.0s ... 60.0s	*S.3*
Set the amount of time that the outstation will wait for an Application Layer confirmation back from the master indicating that the master received the unsolicited response message.		

Unsol Reporting Retry	Device Para / DNP3 / Communication	
• Only available if: Protocol ≠ DNP3 UDP 2	0 ... 255	*S.3*
Set the number of retries that an outstation transmits in each unsolicited response series if it does not receive confirmation back from the master.		

TestSeqNo	Device Para / DNP3 / Communication	
Inactive	Inactive, Active Table	*S.3*
Test if sequence number of request is incremented. If it is not correctly incremented the request will be ignored. It is recommended to have it inactive but some older DNP implementations need it activated.		

TestSBO	Device Para / DNP3 / Communication	
Active	Inactive, Active Table	*S.3*
It enables a stricter comparing of SBO and operate command. For older DNP versions it is recommanded to deactivated it.		

Timeout SBO	Device Para / DNP3 / Communication	
30s	1.0s ... 60.0s	*S.3*
DNP Outputs can be controlled in a two stage procedure (SBO: Select Before Operate). These outputs are to be selected first by a Select command. After this the bit is reserved for this Operate request. This setting defines the timer for this reservation: After the timer has elapsed the bit is released.		

ColdRestart	Device Para / DNP3 / Communication	
Inactive	Inactive, Active Table	*S.3*
Enables support for Cold Restart function.		

Deadb integr time	Device Para / DNP3 / Communication	
1	0 ... 300	*S.3*
Deadband integration time.		

BinaryInput 0 **...** **BinaryInput 63**	Device Para / DNP3 / Point map / Binary Inputs	
-	- ... Internal test state Table	*S.3*
Virtual Digital Input (DNP). This corresponds to a virtual binary output of the protective device.		

DoubleBitInput 0 **...** **DoubleBitInput 5**	Device Para / DNP3 / Point map / Double Bit Inputs	
-	-, Pos Table	*S.3*
Double Bit Digital Input (DNP). This corresponds to a double bit binary output of the protective device.		

BinaryCounter 0 **...** **BinaryCounter 7**	Device Para / DNP3 / Point map / BinaryCounter	
-	- ... Operating hours Cr Table	*S.3*
Counter can be used to report counter values to the DNP master.		

Analog value 0 **...** **Analog value 31**	Device Para / DNP3 / Point map / Analog Input	
-	- ... VL31 THD Table	*S.3*
Analog value can be used to report values to the master (DNP)		

Scale Factor 0 **...** **Scale Factor 31**	Device Para / DNP3 / Point map / Analog Input	
1	0.001 ... 1000000 Table	*S.3*
The scale factor is used to convert the measured value in an integer format		

Dead Band 0 **...** **Dead Band 31**	Device Para / DNP3 / Point map / Analog Input	
1%	0.01% ... 100.00%	*S.3*
If a change of measured value is greater than the deadband value it will be reported to the master.		

7.4.2 DNP3: Direct Controls

Res all Diag Cr	Operation / Count and RevData / DNP3 Operation / Reset	
Inactive	Inactive, Active Table	*S.3*
Reset all diagnosis counters		

Slave Id	Device Para / DNP3 / Communication	
1	0 ... 65519	*S.3*
SlaveId defines the DNP3 address of this device (Outstation)		

Master Id	Device Para / DNP3 / Communication	
65500	0 ... 65519	*S.3*
MasterId defines the DNP3 address of master (SCADA)		

7.4.3 DNP3: Input States

BinaryInput0-I **...** **BinaryInput15-I** **(↳ DNP3 . BinaryInput 0)**	Operation / Status Display / DNP3 / Binary Inputs
⇩	*Virtual Digital Input (DNP). This corresponds to a virtual binary output of the protective device.*

BinaryInput16-I **...** **BinaryInput31-I**	Operation / Status Display / DNP3 / Binary Inputs
⇩	*Virtual Digital Input (DNP). This corresponds to a virtual binary output of the protective device.*

BinaryInput32-I **...** **BinaryInput47-I**	Operation / Status Display / DNP3 / Binary Inputs
⇩	*Virtual Digital Input (DNP). This corresponds to a virtual binary output of the protective device.*

BinaryInput48-I **...** **BinaryInput63-I**	Operation / Status Display / DNP3 / Binary Inputs
⇩	*Virtual Digital Input (DNP). This corresponds to a virtual binary output of the protective device.*

DoubleBitInput0-I **...** **DoubleBitInput5-I** **(↳ DNP3 . DoubleBitInput 0)**	Operation / Status Display / DNP3 / Double Bit Inputs
⇩	*Double Bit Digital Input (DNP). This corresponds to a double bit binary output of the protective device.*

7.4.4 DNP3: Signals (Output States)

busy	Operation / Status Display / DNP3 / State
⇧	*This message is set if the protocol is started. It will be reset if the protocol is shut down.*

ready	Operation / Status Display / DNP3 / State
⇧	*The message will be set if the protocol is successfully started and ready for data exchange.*

Active	Operation / Status Display / DNP3 / State
⇧	*The communication with the Master (SCADA) is active.* *Note that for TCP/UDP, this state is permanently “Low” unless »DataLink confirm« is set to “Always”.*

7.4.5 DNP3: Counters

NReceived	Operation / Count and RevData / DNP3
#	*Diagnostic counter: Number of received characters*

NSent	Operation / Count and RevData / DNP3
#	*Diagnostic counter: Number of sent characters*

NBadFramings	Operation / Count and RevData / DNP3
#	*Diagnostic counter: Number of bad framings. A large number indicates a disturbed serial connection.*

NBadParities	Operation / Count and RevData / DNP3
#	*Diagnostic counter: Number of parity errrors. A large number indicates a disturbed serial connection.*

NBreakSignals	Operation / Count and RevData / DNP3
#	*Diagnostic counter: Number of break signals. A large number indicates a disturbed serial connection.*

NBadChecksum	Operation / Count and RevData / DNP3
#	*Diagnostic counter: Number of frames received with bad checksum.*

7.5 Modbus

7.5.1 Modbus: Global Parameters

TCP Port Config	Device Para / Modbus / Communication / TCP	
Only available if: • Protocol = Modbus TCP • Protocol = Modbus TCP/RTU Default	Default, Private Table	*S.3*
TCP Port Configuration. This parameter needs to be set to “Private” only if another TCP Port than the default one shall be used.		

Port	Device Para / Modbus / Communication / TCP	
Only available if: • Protocol = Modbus TCP • Protocol = Modbus TCP/RTU 502	Adjustable range: • 502 ... 502, If: TCP Port Config = Default • 49152 ... 65535, If: TCP Port Config = Private	*S.3*
IP Port Number. *In general it is recommended to keep the default value. if this is not possible then select a number out of the private range 49152-52151 or 52164-65535 that is not yet in use within your network.*		

t-timeout	Device Para / Modbus / Communication / RTU	
Only available if: • Protocol = Modbus RTU • Protocol = Modbus TCP/RTU 2s	0.01s ... 10.00s	*S.3*
Maximum time that is available to the device for sending an answer to the SCADA system. If the device detects that this time has elapsed (i.e. it failed to send its answer within this time) then it cancels the answer. The time set here must not be longer than the corresponding timeout set for the SCADA system.		

Baud rate	Device Para / Modbus / Communication / RTU	
Only available if: • Protocol = Modbus RTU • Protocol = Modbus TCP/RTU 19200	1200, 2400, 4800, 9600, 19200, 38400 Table	*S.3*
Baud rate		

Physical Settings	Device Para / Modbus / Communication / RTU	
Only available if: • Protocol = Modbus RTU • Protocol = Modbus TCP/RTU 8E1	8E1, 8O1, 8N1, 8N2 Table	*S.3*
Digit 1: Number of bits. Digit 2: E=even parity, O=odd parity, N=no parity. Digit 3: Number of stop bits. More information on the parity: It is possible that the last data bit is followed by a parity bit which is used for recognition of communication errors. The parity bit ensures that with even parity ("EVEN") always an even number of bits with valence "1" or with odd parity ("ODD") an odd number of "1" valence bits are transmitted. But it is also possible to transmit no parity bits (here the setting is "Parity = None"). More information on the stop-bits: The end of a data byte is terminated by the stop-bits.		

t-call	Device Para / Modbus / Communication / General Settings	
10s	1s ... 3600s	*S.3*
If there is no request telegram sent from Scada to the device after expiry of this time - the device concludes a communication failure within the Scada system.		

Scada CmdBlo	Device Para / Modbus / Communication / General Settings	
Inactive	Inactive, Active Table	*S.3*
Activating (allowing)/ Deactivating (disallowing) the blocking of the Scada Commands		

Disable Latching	Device Para / Modbus / Communication / General Settings	
Inactive	Inactive, Active Table	*S.3*
Disable Latching: If this parameter is active (true), none of the Modbus states will be latched. That means that trip signals wont be latched by Modbus.		

AllowGap	Device Para / Modbus / Communication / General Settings	
Inactive	Inactive, Active Table	*S.3*
If this parameter is active (True), the user can request a set of modbus register without getting an exception, because of invalid address in the requested array. The invalid addresses have a special value 0xFAFA, but the user is responsible for ignoring invalid addresses. Attention: This special value can be valid, if address is valid.		

Optical rest position	Device Para / Modbus / Communication / General Settings	
Light on	Light off, Light on Table	*S.3*
Optical rest position		

Config Bin Inp1 ... **Config Bin Inp32**	Device Para / Modbus / Configb Registers / States	
-	- ... Internal test state Table	*S.3*

Virtual Digital Input. This corresponds to a virtual binary output of the protective device.

Latched Config Bin Inp1 ... **Latched Config Bin Inp32**	Device Para / Modbus / Configb Registers / States	
Inactive	Inactive, Active Table	*S.3*

Latched Configurable Binary Input

Mapped Meas 1 ... **Mapped Meas 16**	Device Para / Modbus / Configb Registers / Measured Values	
-	- ... VL31 THD Table	*S.3*

Mapped Measured Values. They can be used to provide measured values to the Modbus Master.

Type of SCADA mapping	Device Para / Modbus / Config. Data Obj.	
Standard	Standard, User-defined Table	*S.3*

*This setting decides whether the communication protocol shall use the default mapping of data objects, or some user-defined mapping that has been loaded from a *.HptSMap file.*

7.5.2 Modbus: Direct Controls

Res Diagn Cr	Operation / Reset	
Inactive	Inactive, Active Table	*P.1*

All Modbus Diagnosis Counters will be reset.

Smart view via Modbus	Device Para / Security / Communication	
Inactive	Inactive, Active Table	*P.1*
Activate (allow) or inactivate (disallow) the Smart view access via the Modbus tunnel.		

Slave ID	Device Para / Modbus / Communication / RTU	
Only available if: • Protocol = Modbus RTU • Protocol = Modbus TCP/RTU 1	1 ... 247	*P.1*
Device address (Slave ID) within the bus system. Each device address has to be unique within a bus system.		

Unit ID	Device Para / Modbus / Communication / TCP	
Only available if: • Protocol = Modbus TCP • Protocol = Modbus TCP/RTU 255	1 ... 255	*P.1*
The Unit Identifier is used for routing. This parameter is to be set, if a Modbus RTU and a Modbus TCP network should be coupled.		

7.5.3 Modbus: Input States

Config Bin Inp1-I ... **Config Bin Inp16-I** (**Modbus . Config Bin Inp1**)	Operation / Status Display / Modbus / Configb Registers
State of the module input: Config Bin Inp	

Config Bin Inp17-I ... **Config Bin Inp32-I**	Operation / Status Display / Modbus / Configb Registers
State of the module input: Config Bin Inp	

7.5.4 Modbus: Signals (Output States)

Transmission RTU	Operation / Status Display / Modbus / State
⇧	Only available if: • Protocol = Modbus RTU • Protocol = Modbus TCP/RTU *Signal: SCADA active*

Transmission TCP	Operation / Status Display / Modbus / State
⇧	Only available if: • Protocol = Modbus TCP • Protocol = Modbus TCP/RTU *Signal: SCADA active*

Scada Cmd 1 ... **Scada Cmd 16**	Operation / Status Display / Modbus / Commands
⇧	*Scada Command*

Device Type	Operation / Status Display / Modbus / State
⇧	*Device type code for relationship between device name and its Modbus code.* *HighPROTEC:* *MRI4 - 1000* *MRU4 - 1001* *MRA4 - 1002* *MCA4 - 1003* *MRDT4 - 1005* *MCDTV4 - 1006* *MCDGV4 - 1007* *MRM4 - 1009* *MRMV4 - 1010* *MCDLV4 - 1011*

Comm Version	Operation / Status Display / Modbus / State
⇧	*Modbus Communication version. This version number changes if something becomes incompatible between different Modbus releases.*

7.5.5 Modbus: Values, Counters

NoOfRequestsTotal	Operation / Count and RevData / Modbus / RTU
#	Only available if: • Protocol = Modbus RTU • Protocol = Modbus TCP/RTU *Total number of requests. Includes requests for other slaves.*

NoOfReqForMe	Operation / Count and RevData / Modbus / RTU
#	Only available if: • Protocol = Modbus RTU • Protocol = Modbus TCP/RTU *Total Number of requests for this slave.*

NoOfResponse	Operation / Count and RevData / Modbus / RTU
#	Only available if: • Protocol = Modbus RTU • Protocol = Modbus TCP/RTU *Total number of requests having been responded.*

NoOfFrameErrors	Operation / Count and RevData / Modbus / RTU
#	Only available if: • Protocol = Modbus RTU • Protocol = Modbus TCP/RTU *Total Number of Frame Errors. Physically corrupted Frame.*

NoOfParityErrors	Operation / Count and RevData / Modbus / RTU
#	Only available if: • Protocol = Modbus RTU • Protocol = Modbus TCP/RTU *Total number of parity errors. Physically corrupted Frame.*

NoOfRespTimeOverruns	Operation / Count and RevData / Modbus / RTU
#	Only available if: • Protocol = Modbus RTU • Protocol = Modbus TCP/RTU *Total number of requests with exceeded response time. Physically corrupted Frame.*

NoOfOverrunErros	Operation / Count and RevData / Modbus / RTU

#

Only available if:

- Protocol = Modbus RTU
- Protocol = Modbus TCP/RTU

Total Number of Overrun Failures. Physically corrupted Frame.

NoOfBreaks	Operation / Count and RevData / Modbus / RTU

#

Only available if:

- Protocol = Modbus RTU
- Protocol = Modbus TCP/RTU

Number of detected communication aborts

NoOfRequestsTotal	Operation / Count and RevData / Modbus / TCP

#

Only available if:

- Protocol = Modbus TCP
- Protocol = Modbus TCP/RTU

Total number of requests. Includes requests for other slaves.

NoOfReqForMe	Operation / Count and RevData / Modbus / TCP

#

Only available if:

- Protocol = Modbus TCP
- Protocol = Modbus TCP/RTU

Total Number of requests for this slave.

NoOfResponse	Operation / Count and RevData / Modbus / TCP

#

Only available if:

- Protocol = Modbus TCP
- Protocol = Modbus TCP/RTU

Total number of requests having been responded.

NoOfQueryInvalid	Operation / Count and RevData / Modbus / TCP

#

Only available if:

- Protocol = Modbus TCP
- Protocol = Modbus TCP/RTU

Total number of Request errors. Request could not be interpreted

NoOfInternalError	Operation / Count and RevData / Modbus / TCP
#	Only available if: • Protocol = Modbus TCP • Protocol = Modbus TCP/RTU *Total Number of Internal errors while interpreting the request.*

Mapped Meas 1 **...** **Mapped Meas 16**	Operation / Count and RevData / Modbus / Measured Values
✎	*Mapped Measured Values. They can be used to provide measured values to the Modbus Master.*

Smart view via Modbus	Operation / Security / Security States
✎	*Activate (allow) or inactivate (disallow) the Smart view access via the Modbus tunnel.*

Config info	Device Para / Modbus / Config. Data Obj.
✎	*Configuration comment (entered by the user during SCADA configuration)*

Config version	Device Para / Modbus / Config. Data Obj.
✎	*Version of the user-defined SCADA configuration*

Config status	Device Para / Modbus / Config. Data Obj.
✎	*Status of the user-defined SCADA configuration.* *Possible values:* *- New SCADA configuration is being loaded, but not active yet.* *- The SCADA configuration is active.* *- The user-defined SCADA configuration is not available (e.g. has not been loaded into the device).* *- Unexpected error. Please contact our service-team.*

7.6 IEC 61850

IEC 61850 communication

7.6.1 IEC 61850: Global Parameters

Function	Device Para / IEC 61850 / Communication	
Inactive	Inactive, Active Table	*S.3*
Permanent activation or deactivation of module/stage.		

Deadb integr time	Device Para / IEC 61850 / Communication	
0	0 ... 300	*S.3*
Deadband integration time.		

7.6.2 IEC 61850: Direct Controls

ResetStatistic	Operation / Reset	
Inactive	Inactive, Active Table	*P.1*
Reset of all IEC61850 diagnostic counters		

Simulation Mode	Device Para / IEC 61850 / Communication	
Inactive	Inactive, Active Table	*P.1*
Direct Command to activate the IEC61850 Simulation Mode, so that the “test” flag is set in all GOOSE messages that the device transmits. Moreover, the device reacts in Simulation Mode to only those messages that have this “test” flag set.		

7.6.3 IEC 61850: Signals (Output States)

MMS Client connected	Operation / Status Display / IEC 61850 / State
At least one MMS client is connected to the device	

All Goose Subscriber active	Operation / Status Display / IEC 61850 / State
All Goose subscriber in the device are working	

GOSINGGIO1.Ind1.stVal **...** **GOSINGGIO1.Ind16.stVal**	Operation / Status Display / IEC 61850 / Virtual Inputs 1
⇧	*Signal: Virtual Input (IEC61850 GGIO Ind): State*

GOSINGGIO1.Ind17.stVal **...** **GOSINGGIO1.Ind32.stVal**	Operation / Status Display / IEC 61850 / Virtual Inputs 1
⇧	*Signal: Virtual Input (IEC61850 GGIO Ind): State*

GOSINGGIO2.Ind1.stVal **...** **GOSINGGIO2.Ind16.stVal**	Operation / Status Display / IEC 61850 / Virtual Inputs 2
⇧	*Signal: Virtual Input (IEC61850 GGIO Ind): State*

GOSINGGIO2.Ind17.stVal **...** **GOSINGGIO2.Ind32.stVal**	Operation / Status Display / IEC 61850 / Virtual Inputs 2
⇧	*Signal: Virtual Input (IEC61850 GGIO Ind): State*

GOSINGGIO1.Ind1.q **...** **GOSINGGIO1.Ind16.q**	Operation / Status Display / IEC 61850 / Virtual Inputs 1
⇧	*Signal: Virtual Input (IEC61850 GGIO Ind): Self-Supervision of the GGIO Input*

GOSINGGIO1.Ind17.q **...** **GOSINGGIO1.Ind32.q**	Operation / Status Display / IEC 61850 / Virtual Inputs 1
⇧	*Signal: Virtual Input (IEC61850 GGIO Ind): Self-Supervision of the GGIO Input*

GOSINGGIO2.Ind1.q **...** **GOSINGGIO2.Ind16.q**	Operation / Status Display / IEC 61850 / Virtual Inputs 2
⇧	*Signal: Virtual Input (IEC61850 GGIO Ind): Self-Supervision of the GGIO Input*

GOSINGGIO2.Ind17.q **...** **GOSINGGIO2.Ind32.q**	Operation / Status Display / IEC 61850 / Virtual Inputs 2
⇧	*Signal: Virtual Input (IEC61850 GGIO Ind): Self-Supervision of the GGIO Input*

CTLGGIO1.SPCSO1.stVal **...** **CTLGGIO1.SPCSO16.stVal**	Operation / Status Display / IEC 61850 / ControlInputs
⇧	*Status bit that can be set by clients like e.g. SCADA (Single Point Controllable Status Output).*

CTLGGIO1.SPCSO17.stVal **...** **CTLGGIO1.SPCSO32.stVal**	Operation / Status Display / IEC 61850 / ControlInputs
⇧	*Status bit that can be set by clients like e.g. SCADA (Single Point Controllable Status Output).*

7.6.4 IEC 61850: Values, Counters

GoosePublisherState	Operation / Status Display / IEC 61850 / State
⟍	*State of the GOOSE Publisher (on or off)*

GooseSubscriberState	Operation / Status Display / IEC 61850 / State
⟍	*State of the GOOSE Subscriber (on or off)*

MmsServerState	Operation / Status Display / IEC 61850 / State
⟍	*State of MMS Server (on or off)*

NoOfGooseRxAll	Operation / Count and RevData / IEC 61850
#	*Total number of received GOOSE messages including messages for other devices (subscribed and not subscribed messages).*

NoOfGooseRxSubscribed	Operation / Count and RevData / IEC 61850
#	*Total Number of subscribed GOOSE messages including messages with incorrect content.*

NoOfGooseRxCorrect	Operation / Count and RevData / IEC 61850
#	*Total Number of subscribed and correctly received GOOSE messages.*

NoOfGooseRxNew	Operation / Count and RevData / IEC 61850
#	*Number of subscribed and correctly received GOOSE messages with new content.*

NoOfGooseTxAll	Operation / Count and RevData / IEC 61850
#	*Total Number of GOOSE messages that have been published by this device.*

NoOfGooseTxNew	Operation / Count and RevData / IEC 61850
#	*Total Number of new GOOSE messages (modified content) that have been published by this device.*

NoOf Srv.Req.All	Operation / Count and RevData / IEC 61850
#	*Total number of MMS Server requests including incorrect requests.*

NoOfDataReadAll	Operation / Count and RevData / IEC 61850
#	*Total Number of values read from this device including incorrect requests.*

NoOfDataReadCorrect	Operation / Count and RevData / IEC 61850
#	*Total Number of correctly read values from this device.*

NoOfDataWrittenAll	Operation / Count and RevData / IEC 61850
#	*Total Number of values written by this device including incorrect ones.*

NoOfDataWrittenCorrect	Operation / Count and RevData / IEC 61850
#	*Total Number of correctly written values by this device.*

NoOfDataChangeNotification	Operation / Count and RevData / IEC 61850
#	*Number of detected changes within the datasets that are published with GOOSE messages.*

No of Client Connections	Operation / Count and RevData / IEC 61850
#	*Number of active MMS client connections*

7.6.5 IEC 61850, IEC 61850

IEC 61850 communication

7.6.5.1 IEC 61850, IEC 61850: Global Parameters

COUTGGIO1.Ind1.stVal **...** **COUTGGIO1.Ind32.stVal**	Device Para / IEC 61850 / Virtual Outputs 1	
-	- ... Internal test state Table	*S.3*
Virtual Output. This signal can be assigned or visualized via the SCD file to other devices within the IEC61850 substation.		

7.6.5.2 IEC 61850, IEC 61850: Input States

COUTGGIO1.Ind1.stVal-I **...** **COUTGGIO1.Ind16.stVal-I** **(IEC 61850 . COUTGGIO1.Ind1.stVal)**	Operation / Status Display / IEC 61850 / Virtual Outputs 1
Module input state: Binary state of the Virtual Output (GGIO)	

COUTGGIO1.Ind17.stVal-I **...** **COUTGGIO1.Ind32.stVal-I**	Operation / Status Display / IEC 61850 / Virtual Outputs 1
Module input state: Binary state of the Virtual Output (GGIO)	

7.7 IEC103

IEC 60870-5-103 communication

7.7.1 IEC103: Global Parameters

Function	Device Para / IEC103 / General Settings	
Inactive	Inactive, Active Table	*S.3*
Activation or deactivation of the IEC103 communication.		

Baud rate	Device Para / IEC103 / General Settings	
19200	1200, 2400, 4800, 9600, 19200, 38400, 57600 Table	*S.3*
Baud rate		

Physical Settings	Device Para / IEC103 / General Settings	
8E1	8E1, 8O1, 8N1, 8N2 Table	*S.3*
Digit 1: Number of bits. Digit 2: E=even parity, O=odd parity, N=no parity. Digit 3: Number of stop bits. More information on the parity: It is possible that the last data bit is followed by a parity bit which is used for recognition of communication errors. The parity bit ensures that with even parity ("EVEN") always an even number of bits with valence "1" or with odd parity ("ODD") an odd number of "1" valence bits are transmitted. But it is also possible to transmit no parity bits (here the setting is "Parity = None"). More information on the stop-bits: The end of a data byte is terminated by the stop-bits.		

t-call	Device Para / IEC103 / General Settings	
60s	1s ... 3600s	*S.3*
If there is no request telegram sent from Scada to the device after expiry of this time - the device concludes a communication failure within the Scada system.		

Transfer Disturb Rec	Device Para / IEC103 / General Settings	
Inactive	Inactive, Active Table	*S.3*
Activates the transmission of disturbance records		

Timezone	Device Para / IEC103 / General Settings	
UTC	UTC, Local Time Table	*S.3*
Selection whether the timestamps in IEC103 messages shall be given as UTC or local time. (“Local time” always includes the actual daylight saving settings.)		

Energy Pulse Rate	Device Para / IEC103 / General Settings	
0	0 . . . 0	*S.3*
The energy values are always transmitted as counter values (i.e. as integer numbers). This setting defines the unit: If "1" is set then each counter increment is 1 kWh, if "2" is set then each counter increment is 2 kWh,etc. The setting "0" has the effect that no energy values are transmitted.		

DFC-Compat.	Device Para / IEC103 / General Settings	
Inactive	Inactive, Active Table	*S.3*
This setting is only required for certain substation implementations. If there should be communication problems related to the Command Response Queue this setting switches the device over to a different behavior.		

Ex activate test mode	Service / Test - Prot inhib. / Scada / IEC103	
Running	- . . . Internal test state Table	*S.3*
The signal assigned to this parameter switches the IEC103 communication into Test Mode.		

Ex activate Block MD	Service / Test - Prot inhib. / Scada / IEC103	
-	- . . . Internal test state Table	*S.3*
The signal assigned to this parameter activates the blocking of IEC103 transmission in monitor direction.		

Type of SCADA mapping	Device Para / IEC103 / Config. Data Obj.	
Standard	Standard, User-defined Table	*S.3*
*This setting decides whether the communication protocol shall use the default mapping of data objects, or some user-defined mapping that has been loaded from a *.HptSMap file.*		

7.7.2 IEC103: Direct Controls

Activate test mode	Service / Test - Prot inhib. / Scada / IEC103	
Inactive	Inactive, Active Table	*S.3*
This Direct Control parameter switches the IEC103 communication into Test Mode (or back to nomal mode).		

Activate Block MD	Service / Test - Prot inhib. / Scada / IEC103	
Inactive	Inactive, Active Table	*S.3*
This Direct Control parameter activates (or deactivates) the blocking of IEC103 transmission in monitor direction.		

Res all Diag Cr	Operation / Reset	
Inactive	Inactive, Active Table	*S.3*
Reset all diagnosis counters		

Slave ID	Device Para / IEC103 / General Settings	
1	1 ... 247	*S.3*
Device address (Slave ID) within the bus system. Each device address has to be unique within a bus system.		

7.7.3 IEC103: Signals (Output States)

Scada Cmd 1 **...** **Scada Cmd 10**	Operation / Status Display / IEC103
Scada Command	

Transmission	Operation / Status Display / IEC103
Signal: SCADA active	

Failure Event lost	Operation / Status Display / IEC103
Failure event lost	

Test mode active	Operation / Status Display / IEC103
Signal: IEC103 communication has been switched over into Test Mode.	

Block MD active	Operation / Status Display / IEC103
Signal: The blocking of IEC103 transmission in monitor direction has been activated.	

7.7.4 IEC103: Values, Counters

NReceived	Operation / Count and RevData / IEC103
Total Number of received Messages	

NSent	Operation / Count and RevData / IEC103
Total Number of sent Messages	

NBadFramings	Operation / Count and RevData / IEC103
#	*Number of bad Messages*

NBadParities	Operation / Count and RevData / IEC103
#	*Number of Parity Errors*

NBreakSignals	Operation / Count and RevData / IEC103
#	*Number of transmission errors with respect to the (electric) signal transport (physical layer).* *If the counter value gets increased constantly you should check for problems with the electrical connection (e.g. missing termination impedance of the serial interface), and make sure the transmission parameters (especially the baud rate) are correct.*

NInternalError	Operation / Count and RevData / IEC103
#	*Number of Internal Errors*

NBadCharChecksum	Operation / Count and RevData / IEC103
#	*Number of Checksum Errors*

Config info	Device Para / IEC103 / Config. Data Obj.
⟍	*Configuration comment (entered by the user during SCADA configuration)*

Config version	Device Para / IEC103 / Config. Data Obj.
⟍	*Version of the user-defined SCADA configuration*

Config status	Device Para / IEC103 / Config. Data Obj.
⟍	*Status of the user-defined SCADA configuration.* *Possible values:* *- Changing: New SCADA configuration is being loaded, but not active yet.* *- OK: The SCADA configuration is active.* *- Config. not avail.: The user-defined SCADA configuration is not available (e.g. has not been loaded into the device).* *- Error: Unexpected error. Please contact our service-team.*

7.8 IEC104

IEC 60870-5-104 communication

7.8.1 IEC104: Global Parameters

Function	Device Para / IEC104 / General Settings	
Inactive	Inactive, Active Table	*S.3*
Activation or deactivation of the IEC104 communication.		

TCP Port Config	Device Para / IEC104 / General Settings	
Default	Default, Private Table	*S.3*
TCP Port Configuration. This parameter needs to be set to “Private” only if another TCP Port than the default one shall be used.		

Port	Device Para / IEC104 / General Settings	
2404	Adjustable range: • 2404 ... 2404, If: TCP Port Config = Default • 49152 ... 65535, If: TCP Port Config = Private	*S.3*
IP Port Number. *In general it is recommended to keep the default value. if this is not possible then select a number out of the private range 49152-52151 or 52164-65535 that is not yet in use within your network.*		

Timeout t0	Device Para / IEC104 / Advanced	
30s	30s ... 30s	*S.3*
Timeout of connection establishment		

Timeout t1	Device Para / IEC104 / Advanced	
15s	15s ... 15s	*S.3*
Timeout of send or test APDUs		

Timeout t2	Device Para / IEC104 / Advanced	
10s	10s ... 10s	*S.3*
Timeout for acknowledges in case of no data messages		

Timeout t3	Device Para / IEC104 / Advanced	
20s	20s ... 20s	*S.3*
Timeout for sending test frames in case of a long idle state		

Param k	Device Para / IEC104 / Advanced	
12	12 ... 12	*S.3*
Protocol parameter k		

Param w	Device Para / IEC104 / Advanced	
8	8 ... 8	*S.3*
Protocol parameter w		

Length of address	Device Para / IEC104 / Advanced	
2	2 ... 2	*S.3*
Number of bytes of the Common Address of the ASDU		

Length of CoT	Device Para / IEC104 / Advanced	
2	2 ... 2	*S.3*
Number of bytes of the Cause of Transmission		

Length of Inf Obj addr	Device Para / IEC104 / Advanced	
3	3 ... 3	*S.3*
Number of bytes of the address of the Information Object		

Timezone	Device Para / IEC104 / General Settings	
UTC	UTC, Local Time Table	*S.3*
Selection whether the timestamps in the transmitted communication telegrams shall be given as UTC or local time. (“Local time” always includes the actual daylight saving settings.)		

Deadb integr time	Device Para / IEC104 / General Settings	
1s	0s ... 1000s	*S.3*
Deadband integration time.		

Timeout SBE	Device Para / IEC104 / General Settings	
30s	1s ... 60s	*S.3*
The communication outputs can be controlled in a two-stage procedure (SBE: Select Before Execute). These outputs have to be selected first by a Select command. After this the bit is reserved for this Execute request. This setting defines the timer for this reservation: After the timer has elapsed the bit is released.		

Update time	Device Para / IEC104 / Advanced	
1s	1s ... 60s	*S.3*
This setting specifies the time after which measurement values are refreshed. If cyclic transmission is selected new values are reported after this time has elapsed.		

Transmit Int. State	Device Para / IEC104 / Advanced	
Active	Inactive, Active Table	*S.3*
If this parameter is set to “active” (default) then the intermediate position of a switchgear, too, is transmitted. This needs to be changed to “inactive” only in the rare case that the substation communication does not support the reporting of intermediate positions.		

Trans. Cmd. State	Device Para / IEC104 / Advanced	
Active	Inactive, Active Table	*S.3*
_ If false it suppress change events for command states (Same address as cmd)		

Type of SCADA mapping	Device Para / IEC104 / Config. Data Obj.	
Standard	Standard, User-defined Table	*S.3*
*This setting decides whether the communication protocol shall use the default mapping of data objects, or some user-defined mapping that has been loaded from a *.HptSMap file.*		

7.8.2 IEC104: Direct Controls

Res all Diag Cr	Operation / Reset	
Inactive	Inactive, Active Table	*S.3*
Reset all diagnosis counters		

Common address	Device Para / IEC104 / General Settings	
1	1 ... 65535	*S.3*
Common Address of the ASDU		

7.8.3 IEC104: Signals (Output States)

busy	Operation / Status Display / IEC104
This message is set if the protocol is started. It will be reset if the protocol is shut down.	

ready	Operation / Status Display / IEC104
The message will be set if the protocol is successfully started and ready for data exchange.	

Transmission	Operation / Status Display / IEC104
⇧	*Signal: SCADA active*

Failure Event lost	Operation / Status Display / IEC104
⇧	*Failure event lost*

Scada Cmd 1 **...** **Scada Cmd 16**	Operation / Status Display / IEC104
⇧	*Scada Command*

7.8.4 IEC104: Values, Counters

NReceived	Operation / Count and RevData / IEC104
#	*Diagnostic counter: Number of received characters*

NSent	Operation / Count and RevData / IEC104
#	*Diagnostic counter: Number of sent characters*

Num. of lost conn.	Operation / Count and RevData / IEC104
#	*Diagnostic counter: Number of lost connections*

NBadChecksum	Operation / Count and RevData / IEC104
#	*Diagnostic counter: Number of frames received with bad checksum.*

Config info	Device Para / IEC104 / Config. Data Obj.
✎	*Configuration comment (entered by the user during SCADA configuration)*

Config version	Device Para / IEC104 / Config. Data Obj.
✎	*Version of the user-defined SCADA configuration*

Config status	Device Para / IEC104 / Config. Data Obj.
	Status of the user-defined SCADA configuration. *Possible values:* *- Changing: New SCADA configuration is being loaded, but not active yet.* *- OK: The SCADA configuration is active.* *- Config. not avail.: The user-defined SCADA configuration is not available (e.g. has not been loaded into the device).* *- Error: Unexpected error. Please contact our service-team.*

7.9 Profibus

Profibus Module

7.9.1 Profibus: Global Parameters

ConfigBinInp 1	Device Para / Profibus / ConfigBinInp 1-16	
-	- ... Internal test state Table	*S.3*
Virtual Digital Input. This corresponds to a virtual binary output of the protective device.		

Latched 1	Device Para / Profibus / ConfigBinInp 1-16	
Inactive	Inactive, Active Table	*S.3*
Defines whether the Input is latched.		

ConfigBinInp 2	Device Para / Profibus / ConfigBinInp 1-16	
-	- ... Internal test state Table	*S.3*
Virtual Digital Input. This corresponds to a virtual binary output of the protective device.		

Latched 2	Device Para / Profibus / ConfigBinInp 1-16	
Inactive	Inactive, Active Table	*S.3*
Defines whether the Input is latched.		

ConfigBinInp 3	Device Para / Profibus / ConfigBinInp 1-16	
-	- ... Internal test state Table	*S.3*
Virtual Digital Input. This corresponds to a virtual binary output of the protective device.		

Latched 3	Device Para / Profibus / ConfigBinInp 1-16	
Inactive	Inactive, Active Table	*S.3*
Defines whether the Input is latched.		

ConfigBinInp 4	Device Para / Profibus / ConfigBinInp 1-16	
-	- . . . Internal test state Table	*S.3*
Virtual Digital Input. This corresponds to a virtual binary output of the protective device.		

Latched 4	Device Para / Profibus / ConfigBinInp 1-16	
Inactive	Inactive, Active Table	*S.3*
Defines whether the Input is latched.		

ConfigBinInp 5	Device Para / Profibus / ConfigBinInp 1-16	
-	- . . . Internal test state Table	*S.3*
Virtual Digital Input. This corresponds to a virtual binary output of the protective device.		

Latched 5	Device Para / Profibus / ConfigBinInp 1-16	
Inactive	Inactive, Active Table	*S.3*
Defines whether the Input is latched.		

ConfigBinInp 6	Device Para / Profibus / ConfigBinInp 1-16	
-	- . . . Internal test state Table	*S.3*
Virtual Digital Input. This corresponds to a virtual binary output of the protective device.		

Latched 6	Device Para / Profibus / ConfigBinInp 1-16	
Inactive	Inactive, Active Table	*S.3*
Defines whether the Input is latched.		

ConfigBinInp 7	Device Para / Profibus / ConfigBinInp 1-16	
-	- . . . Internal test state Table	*S.3*
Virtual Digital Input. This corresponds to a virtual binary output of the protective device.		

Latched 7	Device Para / Profibus / ConfigBinInp 1-16	
Inactive	Inactive, Active Table	*S.3*
Defines whether the Input is latched.		

ConfigBinInp 8	Device Para / Profibus / ConfigBinInp 1-16	
-	- . . . Internal test state Table	*S.3*
Virtual Digital Input. This corresponds to a virtual binary output of the protective device.		

Latched 8	Device Para / Profibus / ConfigBinInp 1-16	
Inactive	Inactive, Active Table	*S.3*
Defines whether the Input is latched.		

ConfigBinInp 9	Device Para / Profibus / ConfigBinInp 1-16	
-	- . . . Internal test state Table	*S.3*
Virtual Digital Input. This corresponds to a virtual binary output of the protective device.		

Latched 9	Device Para / Profibus / ConfigBinInp 1-16	
Inactive	Inactive, Active Table	*S.3*
Defines whether the Input is latched.		

ConfigBinInp 10	Device Para / Profibus / ConfigBinInp 1-16	
-	- . . . Internal test state Table	*S.3*
Virtual Digital Input. This corresponds to a virtual binary output of the protective device.		

Latched 10	Device Para / Profibus / ConfigBinInp 1-16	
Inactive	Inactive, Active Table	*S.3*
Defines whether the Input is latched.		

ConfigBinInp 11	Device Para / Profibus / ConfigBinInp 1-16	
-	- . . . Internal test state Table	*S.3*
Virtual Digital Input. This corresponds to a virtual binary output of the protective device.		

Latched 11	Device Para / Profibus / ConfigBinInp 1-16	
Inactive	Inactive, Active Table	*S.3*
Defines whether the Input is latched.		

ConfigBinInp 12	Device Para / Profibus / ConfigBinInp 1-16	
-	- . . . Internal test state Table	*S.3*
Virtual Digital Input. This corresponds to a virtual binary output of the protective device.		

Latched 12	Device Para / Profibus / ConfigBinInp 1-16	
Inactive	Inactive, Active Table	*S.3*
Defines whether the Input is latched.		

ConfigBinInp 13	Device Para / Profibus / ConfigBinInp 1-16	
-	- . . . Internal test state Table	*S.3*
Virtual Digital Input. This corresponds to a virtual binary output of the protective device.		

Latched 13	Device Para / Profibus / ConfigBinInp 1-16	
Inactive	Inactive, Active Table	*S.3*
Defines whether the Input is latched.		

ConfigBinInp 14	Device Para / Profibus / ConfigBinInp 1-16	
-	- . . . Internal test state Table	*S.3*
Virtual Digital Input. This corresponds to a virtual binary output of the protective device.		

Latched 14	Device Para / Profibus / ConfigBinInp 1-16	
Inactive	Inactive, Active Table	*S.3*
Defines whether the Input is latched.		

ConfigBinInp 15	Device Para / Profibus / ConfigBinInp 1-16	
-	- . . . Internal test state Table	*S.3*
Virtual Digital Input. This corresponds to a virtual binary output of the protective device.		

Latched 15	Device Para / Profibus / ConfigBinInp 1-16	
Inactive	Inactive, Active Table	*S.3*
Defines whether the Input is latched.		

ConfigBinInp 16	Device Para / Profibus / ConfigBinInp 1-16	
-	- . . . Internal test state Table	*S.3*
Virtual Digital Input. This corresponds to a virtual binary output of the protective device.		

Latched 16	Device Para / Profibus / ConfigBinInp 1-16	
Inactive	Inactive, Active Table	*S.3*
Defines whether the Input is latched.		

ConfigBinInp 17	Device Para / Profibus / ConfigBinInp 17-32	
-	- . . . Internal test state Table	*S.3*
Virtual Digital Input. This corresponds to a virtual binary output of the protective device.		

Latched 17	Device Para / Profibus / ConfigBinInp 17-32	
Inactive	Inactive, Active Table	*S.3*
Defines whether the Input is latched.		

ConfigBinInp 18	Device Para / Profibus / ConfigBinInp 17-32	
-	- . . . Internal test state Table	*S.3*
Virtual Digital Input. This corresponds to a virtual binary output of the protective device.		

Latched 18	Device Para / Profibus / ConfigBinInp 17-32	
Inactive	Inactive, Active Table	*S.3*
Defines whether the Input is latched.		

ConfigBinInp 19	Device Para / Profibus / ConfigBinInp 17-32	
-	- . . . Internal test state Table	*S.3*
Virtual Digital Input. This corresponds to a virtual binary output of the protective device.		

Latched 19	Device Para / Profibus / ConfigBinInp 17-32	
Inactive	Inactive, Active Table	*S.3*
Defines whether the Input is latched.		

ConfigBinInp 20	Device Para / Profibus / ConfigBinInp 17-32	
-	- . . . Internal test state Table	*S.3*
Virtual Digital Input. This corresponds to a virtual binary output of the protective device.		

Latched 20	Device Para / Profibus / ConfigBinInp 17-32	
Inactive	Inactive, Active Table	*S.3*
Defines whether the Input is latched.		

ConfigBinInp 21	Device Para / Profibus / ConfigBinInp 17-32	
-	- . . . Internal test state Table	*S.3*
Virtual Digital Input. This corresponds to a virtual binary output of the protective device.		

Latched 21	Device Para / Profibus / ConfigBinInp 17-32	
Inactive	Inactive, Active Table	*S.3*
Defines whether the Input is latched.		

ConfigBinInp 22	Device Para / Profibus / ConfigBinInp 17-32	
-	- . . . Internal test state Table	*S.3*
Virtual Digital Input. This corresponds to a virtual binary output of the protective device.		

Latched 22	Device Para / Profibus / ConfigBinInp 17-32	
Inactive	Inactive, Active Table	*S.3*
Defines whether the Input is latched.		

ConfigBinInp 23	Device Para / Profibus / ConfigBinInp 17-32	
-	- . . . Internal test state Table	*S.3*
Virtual Digital Input. This corresponds to a virtual binary output of the protective device.		

Latched 23	Device Para / Profibus / ConfigBinInp 17-32	
Inactive	Inactive, Active Table	*S.3*
Defines whether the Input is latched.		

ConfigBinInp 24	Device Para / Profibus / ConfigBinInp 17-32	
-	- . . . Internal test state Table	*S.3*
Virtual Digital Input. This corresponds to a virtual binary output of the protective device.		

Latched 24	Device Para / Profibus / ConfigBinInp 17-32	
Inactive	Inactive, Active Table	*S.3*
Defines whether the Input is latched.		

ConfigBinInp 25	Device Para / Profibus / ConfigBinInp 17-32	
-	- . . . Internal test state Table	*S.3*
Virtual Digital Input. This corresponds to a virtual binary output of the protective device.		

Latched 25	Device Para / Profibus / ConfigBinInp 17-32	
Inactive	Inactive, Active Table	*S.3*
Defines whether the Input is latched.		

ConfigBinInp 26	Device Para / Profibus / ConfigBinInp 17-32	
-	- . . . Internal test state Table	*S.3*
Virtual Digital Input. This corresponds to a virtual binary output of the protective device.		

Latched 26	Device Para / Profibus / ConfigBinInp 17-32	
Inactive	Inactive, Active Table	*S.3*
Defines whether the Input is latched.		

ConfigBinInp 27	Device Para / Profibus / ConfigBinInp 17-32	
-	- . . . Internal test state Table	*S.3*
Virtual Digital Input. This corresponds to a virtual binary output of the protective device.		

Latched 27	Device Para / Profibus / ConfigBinInp 17-32	
Inactive	Inactive, Active Table	*S.3*
Defines whether the Input is latched.		

ConfigBinInp 28	Device Para / Profibus / ConfigBinInp 17-32	
-	- . . . Internal test state Table	*S.3*
Virtual Digital Input. This corresponds to a virtual binary output of the protective device.		

Latched 28	Device Para / Profibus / ConfigBinInp 17-32	
Inactive	Inactive, Active Table	*S.3*
Defines whether the Input is latched.		

ConfigBinInp 29	Device Para / Profibus / ConfigBinInp 17-32	
-	- . . . Internal test state Table	*S.3*
Virtual Digital Input. This corresponds to a virtual binary output of the protective device.		

Latched 29	Device Para / Profibus / ConfigBinInp 17-32	
Inactive	Inactive, Active Table	*S.3*
Defines whether the Input is latched.		

ConfigBinInp 30	Device Para / Profibus / ConfigBinInp 17-32	
-	- . . . Internal test state Table	*S.3*
Virtual Digital Input. This corresponds to a virtual binary output of the protective device.		

Latched 30	Device Para / Profibus / ConfigBinInp 17-32	
Inactive	Inactive, Active Table	*S.3*
Defines whether the Input is latched.		

ConfigBinInp 31	Device Para / Profibus / ConfigBinInp 17-32	
-	- . . . Internal test state Table	*S.3*
Virtual Digital Input. This corresponds to a virtual binary output of the protective device.		

Latched 31	Device Para / Profibus / ConfigBinInp 17-32	
Inactive	Inactive, Active Table	*S.3*
Defines whether the Input is latched.		

ConfigBinInp 32	Device Para / Profibus / ConfigBinInp 17-32	
-	- . . . Internal test state Table	*S.3*
Virtual Digital Input. This corresponds to a virtual binary output of the protective device.		

Latched 32	Device Para / Profibus / ConfigBinInp 17-32	
Inactive	Inactive, Active Table	*S.3*
Defines whether the Input is latched.		

Little Endian	Device Para / Profibus / Bus parameters	
Active	Inactive, Active Table	*S.3*
If this setting is “active” all numbers are transmitted with the byte order Little Endian, otherwise the byte order Big Endian is used. (If all numbers received by your SCADA system should be completely wrong, changing this setting might help.)		

Type of SCADA mapping	Device Para / Profibus / Config. Data Obj.	
Standard	Standard, User-defined Table	*S.3*
*This setting decides whether the communication protocol shall use the default mapping of data objects, or some user-defined mapping that has been loaded from a *.HptSMap file.*		

7.9.2 Profibus: Direct Controls

Reset Comds	Operation / Reset	
Inactive	Inactive, Active Table	*P.1*
All Profibus Commands will be reset.		

Slave ID	Operation / Status Display / Profibus / State Device Para / Profibus / Bus parameters	
2	2 . . . 125	*P.1*
Device address (Slave ID) within the bus system. Each device address has to be unique within a bus system.		

7.9.3 Profibus: Input States

Assignment 1-I ... **Assignment 16-I** (↳ **Profibus . ConfigBinInp 1**)	Operation / Status Display / Profibus / ConfigBinInp 1-16
⇩	*Module input state: Scada Assignment*

Assignment 17-I ... **Assignment 32-I** (↳ **Profibus . ConfigBinInp 17**)	Operation / Status Display / Profibus / ConfigBinInp 17-32
⇩	*Module input state: Scada Assignment*

7.9.4 Profibus: Signals (Output States)

Data OK	Operation / Status Display / Profibus / State
⇧	*Data within the Input field are OK (Yes=1)*

SubModul Err	Operation / Status Display / Profibus / State
⇧	*Assignable Signal, Failure in Sub-Module, Communication Failure.*

Connection active	Operation / Status Display / Profibus / State
⇧	*Connection active*

Scada Cmd 1 ... **Scada Cmd 16**	Operation / Status Display / Profibus / Commands
⇧	*Scada Command*

7.9.5 Profibus: Values, Counters

Fr Sync Err	Operation / Count and RevData / Profibus
#	*Frames, that were sent from the Master to the Slave are faulty.*

Num. CRC err.	Operation / Count and RevData / Profibus
#	*Number of CRC errors that the subsystem manager has recognized in the received response frames from the subsystem. (Each error caused a subsystem reset.)*

Num. frame loss err.	Operation / Count and RevData / Profibus
#	*Number of frame loss errors that the subsystem manager has recognized in the received response frames from the subsystem. (Each error caused a subsystem reset.)*

Num. trig. CRC err.	Operation / Count and RevData / Profibus
#	*Number of CRC errors that the subsystem has recognized in the received trigger frames from the host.*

Num. subsys. res.	Operation / Count and RevData / Profibus
#	*Number of subsystem restarts or resets that the subsystem manager has caused.*

Slave State	Operation / Status Display / Profibus / State
⟍	*Communication State between Slave and Master.*

Baud rate	Operation / Status Display / Profibus / State
⟍	*The baud rate that has been detected lastly, will still be shown after a connection issue.*

PNO Id	Operation / Status Display / Profibus / State
⟍	*PNO Identification Number. GSD Identification Number.*

Master ID	Operation / Status Display / Profibus / State
#	*Device address (Master ID) within the bus system. Each device address has to be unique within a bus system.*

HO Id PSub	Operation / Status Display / Profibus / State
#	*Handoff Id of PbSub*

t-WatchDog	Operation / Status Display / Profibus / State
#	*The Profibus Chip detects a communication issue if this timer is expired without any communication (Parameterising telegram).*

Config info	Operation / Status Display / Profibus / State Device Para / Profibus / Config. Data Obj.
⟍	*Configuration comment (entered by the user during SCADA configuration)*

Config version	Operation / Status Display / Profibus / State Device Para / Profibus / Config. Data Obj.
⟍	*Version of the user-defined SCADA configuration*

Config status	Operation / Status Display / Profibus / State Device Para / Profibus / Config. Data Obj.
	Status of the user-defined SCADA configuration. *Possible values:*

7.10 IRIG-B

IRIG-B-Module

7.10.1 IRIG-B: Device Planning Parameters

Mode	Device planning / Projected Elements	
-	-, use Table	*S.3*
IRIG-B-Module, general operation mode		

7.10.2 IRIG-B: Global Parameters

Function	Device Para / Time / TimeSync / IRIG-B	
Inactive	Inactive, Active Table	*S.3*
Permanent activation or deactivation of module/stage.		

IRIG-B00X	Device Para / Time / TimeSync / IRIG-B	
IRIGB-000	IRIGB-000 . . . IRIGB-007 Table	*S.3*
Determination of the Type: IRIG-B00X. IRIG-B types differ in types of included “Coded Expressions” (year, control-functions, straight-binary-seconds).		

7.10.3 IRIG-B: Direct Controls

Res IRIG-B Cr	Operation / Reset	
Inactive	Inactive, Active Table	*P.1*
Resetting of the Diagnosis Counters: IRIG-B		

7.10.4 IRIG-B: Signals (Output States)

IRIG-B active	Operation / Status Display / TimeSync / IRIG-B
Signal: If there is no valid IRIG-B signal for 60 sec, IRIG-B is regarded as inactive.	

High-Low Invert	Operation / Status Display / TimeSync / IRIG-B
Signal: The High and Low signals of the IRIG-B are inverted. This does NOT mean that the wiring is faulty. If the wiring is faulty no IRIG-B signal will be detected.	

Control Signal1 **...** **Control Signal9**	Operation / Status Display / TimeSync / IRIG-B
⇧	*Signal: IRIG-B Control Signal. The external IRIG-B generator can set these signals. They can be used for further control procedures inside the device (e.g. logic funtions).*

Control Signal10 **...** **Control Signal18**	Operation / Status Display / TimeSync / IRIG-B
⇧	*Signal: IRIG-B Control Signal. The external IRIG-B generator can set these signals. They can be used for further control procedures inside the device (e.g. logic funtions).*

7.10.5 IRIG-B: Counters

NoOfFramesOK	Operation / Count and RevData / TimeSync / IRIG-B
#	*Total Number valid Frames.*

NoOfFrameErrors	Operation / Count and RevData / TimeSync / IRIG-B
#	*Total Number of Frame Errors. Physically corrupted Frame.*

Edges	Operation / Count and RevData / TimeSync / IRIG-B
#	*Edges: Total number of rising and falling edges. This signal indicates if a signal is available at the IRIG-B input.*

7.11 SNTP

SNTP-Module

7.11.1 SNTP: Device Planning Parameters

Mode	Device planning / Projected Elements	
-	-, use Table	*S.3*
SNTP-Module, general operation mode		

7.11.2 SNTP: Global Parameters

Server1	Device Para / Time / TimeSync / SNTP	
Inactive	Inactive, Active Table	*S.3*
Server 1		

IP Byte1 **...** **IP Byte4**	Device Para / Time / TimeSync / SNTP	
0	0 ... 255	*S.3*
IP1.IP2.IP3.IP4		

Server2	Device Para / Time / TimeSync / SNTP	
Inactive	Inactive, Active Table	*S.3*
Server 2		

IP Byte1 **...** **IP Byte4**	Device Para / Time / TimeSync / SNTP	
0	0 ... 255	*S.3*
IP1.IP2.IP3.IP4		

7.11.3 SNTP: Direct Controls

Res Counter	Operation / Reset	
Inactive	Inactive, Active Table	*P.1*

Reset all Counters.

7.11.4 SNTP: Signals (Output States)

SNTP active	Operation / Status Display / TimeSync / SNTP

Signal: If there is no valid SNTP signal for 120 sec, SNTP is regarded as inactive.

7.11.5 SNTP: Values, Counters

NoOfSyncs	Operation / Count and RevData / TimeSync / SNTP

Total Number of Synchronizations.

NoOfConnectLost	Operation / Count and RevData / TimeSync / SNTP

Total Number of lost SNTP Connections (no sync for 120 sec).

NoOfSmallSyncs	Operation / Count and RevData / TimeSync / SNTP

Service counter: Total Number of very small Time Corrections.

NoOfNormSyncs	Operation / Count and RevData / TimeSync / SNTP

Service counter: Total Number of normal Time Corrections

NoOfBigSyncs	Operation / Count and RevData / TimeSync / SNTP

Service counter: Total Number of big Time Corrections

NoOfFiltSyncs	Operation / Count and RevData / TimeSync / SNTP

Service counter: Total Number of filtered Time Corrections

NoOfSlowTrans	Operation / Count and RevData / TimeSync / SNTP

Service counter: Total Number of slow Transfers.

NoOfHighOffs	Operation / Count and RevData / TimeSync / SNTP

Service counter: Total Number of high Offsets.

NoOfIntTimeouts	Operation / Count and RevData / TimeSync / SNTP
#	*Service counter: Total Number of internal timeouts.*

Used Server	Operation / Status Display / TimeSync / SNTP
	Which Server is used for SNTP synchronization.

StratumServer1	Operation / Status Display / TimeSync / SNTP
#	*Stratum of Server 1*

PrecServer1	Operation / Status Display / TimeSync / SNTP
	Precision of Server 1

StratumServer2	Operation / Status Display / TimeSync / SNTP
#	*Stratum of Server 2*

PrecServer2	Operation / Status Display / TimeSync / SNTP
	Precision of Server 2

ServerQlty	Operation / Status Display / TimeSync / SNTP
	Quality of Server used for Synchronization (GOOD, SUFFICIENT, BAD)

NetConn	Operation / Status Display / TimeSync / SNTP
	Quality of Network Connection (GOOD, SUFFICIENT, BAD).

8 Field settings

8.1 Field Para

Field settings

8.1.1 Field Para: Global Parameters

Phase Sequence	Field Para / General Settings	
ABC	ABC, ACB Table	*S.3*
Phase Sequence		

f	Field Para / General Settings	
50Hz	50Hz, 60Hz Table	*S.3*
Nominal frequency		

8.2 VT

Voltage Transformer

8.2.1 VT: Global Parameters

VT pri	Field Para / VT	
10000V	60V ... 500000V	*S.3*
Nominal voltage of the Voltage Transformers at the primary side. Note that always the phase-to-phase voltage must be entered here.		

VT sec	Field Para / VT	
100V	60.00V ... 520.00V	*S.3*
Nominal voltage of the Voltage Transformers at the secondary side. Note that always the phase-to-phase voltage must be entered here.		

VT con	Field Para / VT	
Phase to Ground	Phase to Phase, Phase to Ground Table	*S.3*
This parameter has to be set in order to ensure the correct assignment of the voltage measurement channels in the device.		

EVT pri	Field Para / VT	
10000V	60V ... 500000V	*S.3*
Primary nominal voltage of the e-n winding of the voltage transformers, which is only taken into account in the direct measurement of the residual voltage (GVT con=measured/broken delta).		

EVT sec	Field Para / VT	
100V	35.00V ... 520.00V	*S.3*
Secondary nominal voltage of the e-n winding of the voltage transformers, which is only taken into account in the direct measurement of the residual voltage.		

V Block f	Field Para / Frequency	
0.60Vn	0.15Vn ... 0.90Vn	*S.3*
Threshold for the release of the frequency stages: Frequency-based protection functions are blocked if the voltage drops below this setting. *This is necessary to avoid an undesired response of the frequency-based protection functions in case of a voltage disturbance caused by a fault. For example, faults with an arc flash generate a high proportion of harmonics in the voltage. Such disturbances will interfere with accurate frequency detection.*		

V Sync	Field Para / VT	
L12	Adjustable range: • L1, L2, L3, L12, L23, L31, If: VT con = Phase to Ground • L12, L23, L31, If: VT con ≠ Phase to Ground Table	S.3
The fourth measuring input of the voltage measuring card measures the voltage that is to be synchronized.		

delta phi - Mode	Field Para / Frequency	
two phases	one phase, two phases, three phases Table	S.3
The delta phi element (vector surge) trips, if the permissable voltage angle shift (delta phi) of the three measured voltages (phase-ground or phase-phase) in: one phase, two phases or within all phases is exceeded.		

Stab. window f	Field Para / Frequency	
4	0 ... 10	S.3
Stabilizing window, for stabilizing the frequency values against momentary fluctuations. The setting value is in cycles at the rated frequency. Set to "0" for VDE AR-N 4110:2023-9 / 4120:2018-11.		

Stab. window f for df/dt	Field Para / Frequency	
3	2 ... 10	S.3
Stabilizing window, for stabilizing the frequency values that are used as input for df/dt calculation against momentary fluctuations. The setting value is in cycles at the rated frequency.		

Window df/dt	Field Para / Frequency	
4	1 ... 10	S.3
Window for the determination of df/dt (ROCOF). The setting value is in cycles at the rated frequency.		

Stab. window df/dt	Field Para / Frequency	
5	0 ... 10	S.3
Stabilizing window, for stabilizing the df/dt (ROCOF) values against momentary fluctuations. The setting value is in cycles at the rated frequency.		

V Cutoff Level	Device Para / Measurem Display / Voltage	
0.005Vn	0.0Vn ... 0.100Vn	S.3
The Phase Voltage shown in the Display or within the PC Software will be displayed as zero, if the Phase Voltage falls below this Cutoff Level. This parameter has no impact on recorders. This parameter is related to the voltage that is connected to the device (phase-to-phase or phase-to-earth).		

VG meas Cutoff Level	Device Para / Measurem Display / Voltage	
0.005Vn	0.0Vn ... 0.100Vn	S.3
The measured Residual Voltage shown in the Display or within the PC Software will be displayed as zero, if the measured Residual Voltage falls below this Cutoff Level. This parameter has no impact on recorders.		

VG calc Cutoff Level	Device Para / Measurem Display / Voltage	
0.005Vn	0.0Vn ... 0.100Vn	*S.3*
The calculated Residual Voltage shown in the Display or within the PC Software will be displayed as zero, if the calculated Residual Voltage falls below this Cutoff Level. This parameter has no impact on recorders.		

V012 Comp Cutoff Level	Device Para / Measurem Display / Voltage	
0.005Vn	0.0Vn ... 0.100Vn	*S.3*
The Symmetrical Component shown in the Display or within the PC Software will be displayed as zero, if the Symmetrical Component falls below this Cutoff Level. This parameter has no impact on recorders.		

8.2.2 VT: Signals (Output States)

Phase seq. wrong	Operation / Status Display / Supervision / Phase Sequence
Signal that the device has detected a phase sequence (L1-L2-L3 / L1-L3-L2) that is different from the one that had been set at [Field settings / General Settings] »Phase Sequence«.	

8.2.3 VT: Values

f	Operation / Measured Values / Voltage
Measured value: Frequency	

df/dt	Operation / Measured Values / Voltage
Measured value (calculated): Rate-of-frequency-change.	

delta phi	Operation / Measured Values / Voltage
Measured value (calculated): Vector surge	

VL12	Operation / Measured Values / Voltage
Measured value: Phase-to-phase voltage (fundamental)	

VL23	Operation / Measured Values / Voltage
Measured value: Phase-to-phase voltage (fundamental)	

VL31	Operation / Measured Values / Voltage
Measured value: Phase-to-phase voltage (fundamental)	

VL1	Operation / Measured Values / Voltage
Measured value: Phase-to-neutral voltage (fundamental)	

VL2	Operation / Measured Values / Voltage
	Measured value: Phase-to-neutral voltage (fundamental)

VL3	Operation / Measured Values / Voltage
	Measured value: Phase-to-neutral voltage (fundamental)

VX meas	Operation / Measured Values / Voltage
	Measured value (measured): VX measured (fundamental)

VG calc	Operation / Measured Values / Voltage
	Measured value (calculated): VG (fundamental)

V0	Operation / Measured Values / Voltage
	Measured value (calculated): Symmetrical components Zero voltage(fundamental)

V1	Operation / Measured Values / Voltage
	Measured value (calculated): Symmetrical components positive phase sequence voltage(fundamental)

V2	Operation / Measured Values / Voltage
	Measured value (calculated): Symmetrical components negative phase sequence voltage(fundamental)

VL12 RMS	Operation / Measured Values / Voltage RMS
	Measured value: Phase-to-phase voltage (RMS)

VL23 RMS	Operation / Measured Values / Voltage RMS
	Measured value: Phase-to-phase voltage (RMS)

VL31 RMS	Operation / Measured Values / Voltage RMS
	Measured value: Phase-to-phase voltage (RMS)

VL1 RMS	Operation / Measured Values / Voltage RMS
	Measured value: Phase-to-neutral voltage (RMS)

VL2 RMS	Operation / Measured Values / Voltage RMS
	Measured value: Phase-to-neutral voltage (RMS)

VL3 RMS	Operation / Measured Values / Voltage RMS
	Measured value: Phase-to-neutral voltage (RMS)

VX meas RMS	Operation / Measured Values / Voltage RMS
	Measured value (measured): VX measured (RMS)

VG calc RMS	Operation / Measured Values / Voltage RMS
	Measured value (calculated): VG (RMS)

phi VL12	Operation / Measured Values / Voltage
	Measured value (calculated): Angle of Phasor VL12 *Reference phasor is required to calculate the angle. This is the first measured voltage (or current) channel with sufficiently high amplitude.*

phi VL23	Operation / Measured Values / Voltage
	Measured value (calculated): Angle of Phasor VL23 *Reference phasor is required to calculate the angle. This is the first measured voltage (or current) channel with sufficiently high amplitude.*

phi VL31	Operation / Measured Values / Voltage
	Measured value (calculated): Angle of Phasor VL31 *Reference phasor is required to calculate the angle. This is the first measured voltage (or current) channel with sufficiently high amplitude.*

phi VL1	Operation / Measured Values / Voltage
	Measured value (calculated): Angle of Phasor VL1 *Reference phasor is required to calculate the angle. This is the first measured voltage (or current) channel with sufficiently high amplitude.*

phi VL2	Operation / Measured Values / Voltage
	Measured value (calculated): Angle of Phasor VL2 *Reference phasor is required to calculate the angle. This is the first measured voltage (or current) channel with sufficiently high amplitude.*

phi VL3	Operation / Measured Values / Voltage
	Measured value (calculated): Angle of Phasor VL3 *Reference phasor is required to calculate the angle. This is the first measured voltage (or current) channel with sufficiently high amplitude.*

phi VX meas	Operation / Measured Values / Voltage
	Measured value: Angle of Phasor VX meas *Reference phasor is required to calculate the angle. This is the first measured voltage (or current) channel with sufficiently high amplitude.*

phi VG calc	Operation / Measured Values / Voltage
	Measured value (calculated): Angle of Phasor VG calc *Reference phasor is required to calculate the angle. This is the first measured voltage (or current) channel with sufficiently high amplitude.*

phi V0	Operation / Measured Values / Voltage
	Measured value (calculated): Angle Zero Sequence System *Reference phasor is required to calculate the angle. This is the first measured voltage (or current) channel with sufficiently high amplitude.*

phi V1	Operation / Measured Values / Voltage
	Measured value (calculated): Angle of Positive Sequence System *Reference phasor is required to calculate the angle. This is the first measured voltage (or current) channel with sufficiently high amplitude.*

phi V2	Operation / Measured Values / Voltage
	Measured Value (calculated): Angle of Negative Sequence System *Reference phasor is required to calculate the angle. This is the first measured voltage (or current) channel with sufficiently high amplitude.*

%(V2/V1)	Operation / Measured Values / Voltage
	Measured value (calculated): V2/V1, phase sequence will be taken into account automatically.

%VL12 THD	Operation / Measured Values / Voltage RMS
	Measured value (calculated): V12 Total Harmonic Distortion / Ground wave

%VL23 THD	Operation / Measured Values / Voltage RMS
	Measured value (calculated): V23 Total Harmonic Distortion / Ground wave

%VL31 THD	Operation / Measured Values / Voltage RMS
	Measured value (calculated): V31 Total Harmonic Distortion / Ground wave

%VL1 THD	Operation / Measured Values / Voltage RMS
	Measured value (calculated): VL1 Total Harmonic Distortion / Ground wave

%VL2 THD	Operation / Measured Values / Voltage RMS
	Measured value (calculated): VL2 Total Harmonic Distortion / Ground wave

%VL3 THD	Operation / Measured Values / Voltage RMS
	Measured value (calculated): VL3 Total Harmonic Distortion / Ground wave

VL12 THD	Operation / Measured Values / Voltage RMS
	Measured value (calculated): V12 Total Harmonic Distortion

VL23 THD	Operation / Measured Values / Voltage RMS
	Measured value (calculated): V23 Total Harmonic Distortion

VL31 THD	Operation / Measured Values / Voltage RMS
	Measured value (calculated): V31 Total Harmonic Distortion

VL1 THD	Operation / Measured Values / Voltage RMS
	Measured value (calculated): VL1 Total Harmonic Distortion

VL2 THD	Operation / Measured Values / Voltage RMS
	Measured value (calculated): VL2 Total Harmonic Distortion

VL3 THD	Operation / Measured Values / Voltage RMS
	Measured value (calculated): VL3 Total Harmonic Distortion

8.2.4 VT: Statistical Values

f max	Operation / Statistics / Max / Voltage
	Max. frequency value

f min	Operation / Statistics / Min / Voltage
	Min. frequency value

V1 max	Operation / Statistics / Max / Voltage
	Maximum value: Symmetrical components positive phase sequence voltage(fundamental)

V1 min	Operation / Statistics / Min / Voltage
	Minimum value: Symmetrical components positive phase sequence voltage(fundamental)

V2 max	Operation / Statistics / Max / Voltage
	Maximum value: Symmetrical components negative phase sequence voltage(fundamental)

V2 min	Operation / Statistics / Min / Voltage
	Minimum value: Symmetrical components negative phase sequence voltage(fundamental)

VL12 max RMS	Operation / Statistics / Max / Voltage
🗠	*VL12 maximum value (RMS)*

VL12 avg RMS	Operation / Statistics / Vavg
🗠	*VL12 average value (RMS)*

VL12 min RMS	Operation / Statistics / Min / Voltage
🗠	*VL12 minimum value (RMS)*

VL23 max RMS	Operation / Statistics / Max / Voltage
🗠	*VL23 maximum value (RMS)*

VL23 avg RMS	Operation / Statistics / Vavg
🗠	*VL23 average value (RMS)*

VL23 min RMS	Operation / Statistics / Min / Voltage
🗠	*VL23 minimum value (RMS)*

VL31 max RMS	Operation / Statistics / Max / Voltage
🗠	*VL31 maximum value (RMS)*

VL31 avg RMS	Operation / Statistics / Vavg
🗠	*VL31 average value (RMS)*

VL31 min RMS	Operation / Statistics / Min / Voltage
🗠	*VL31 minimum value (RMS)*

VL1 max RMS	Operation / Statistics / Max / Voltage
🗠	*VL1 maximum value (RMS)*

VL1 avg RMS	Operation / Statistics / Vavg
🗠	*VL1 average value (RMS)*

VL1 min RMS	Operation / Statistics / Min / Voltage
🗠	*VL1 minimum value (RMS)*

VL2 max RMS	Operation / Statistics / Max / Voltage
🗠	*VL2 maximum value (RMS)*

VL2 avg RMS	Operation / Statistics / Vavg
🗠	*VL2 average value (RMS)*

VL2 min RMS	Operation / Statistics / Min / Voltage
🗠	*VL2 minimum value (RMS)*

VL3 max RMS	Operation / Statistics / Max / Voltage
🗠	*VL3 maximum value (RMS)*

VL3 avg RMS	Operation / Statistics / Vavg
🗠	*VL3 average value (RMS)*

VL3 min RMS	Operation / Statistics / Min / Voltage
🗠	*VL3 minimum value (RMS)*

VX meas max RMS	Operation / Statistics / Max / Voltage
🗠	*Measured value: VX maximum value (RMS)*

VX meas min RMS	Operation / Statistics / Min / Voltage
🗠	*Measured value: VX minimum value (RMS)*

VG calc max RMS	Operation / Statistics / Max / Voltage
🗠	*Measured value (calculated):VX maximum value (RMS)*

VG calc min RMS	Operation / Statistics / Min / Voltage
🗠	*Measured value (calculated):VX minimum value (RMS)*

%(V2/V1) max	Operation / Statistics / Max / Voltage
🗠	*Measured value (calculated):V2/V1 maximum value, phase sequence will be taken into account automatically*

%(V2/V1) min	Operation / Statistics / Min / Voltage
🗠	*Measured value (calculated):V2/V1 minimum value , phase sequence will be taken into account automatically*

9 Protection

Module General Protection

9.1 Prot: Global Parameters

Function	Protection Para / Global Prot Para / Prot	
Active	Inactive, Active Table	*P.2*
Permanent activation or deactivation of module/stage.		

ExBlo Fc	Protection Para / Global Prot Para / Prot	
Inactive	Inactive, Active Table	*P.2*
Activate (allow) the external blocking of the global protection functionality of the device.		

ExBlo1 **ExBlo2**	Protection Para / Global Prot Para / Prot	
-	- . . . Internal test state Table	*P.2*
If external blocking of this module is activated (allowed), the global protection functionality of the device will be blocked if the state of the assigned signal becomes true.		

Blo TripCmd	Protection Para / Global Prot Para / Prot	
Inactive	Inactive, Active Table	*P.2*
Permanent blocking of the Trip Command of the entire Protection.		

ExBlo TripCmd Fc	Protection Para / Global Prot Para / Prot	
Inactive	Inactive, Active Table	*P.2*
Activate (allow) the external blocking of the trip command of the entire device.		

ExBlo TripCmd	Protection Para / Global Prot Para / Prot	
-	- . . . Internal test state Table	*P.2*
If external blocking of the tripping command is activated (allowed), the tripping command of the entire device will be blocked if the state of the assigned signal becomes true.		

9.2 Prot: Direct Controls

Res FaultNo a GridFaultNo	Operation / Reset	
Inactive	Inactive, Active Table	*P.1*
Resetting of fault number and grid fault number.		

9.3 Prot: Input States

ExBlo1-I (Prot . ExBlo1)	Operation / Status Display / Prot
Module input state: External blocking1	

ExBlo2-I	Operation / Status Display / Prot
Module input state: External blocking2	

ExBlo TripCmd-I (Prot . ExBlo TripCmd)	Operation / Status Display / Prot
Module input state: External Blocking of the Trip Command	

9.4 Prot: Signals (Output States)

available	Operation / Status Display / Prot
Signal: Protection is available	

Active	Operation / Status Display / All Actives Operation / Status Display / Prot
Signal: active	

ExBlo	Operation / Status Display / Prot
Signal: External Blocking	

Blo TripCmd	Operation / Status Display / Prot
⇧	*Signal: Trip Command blocked*

ExBlo TripCmd	Operation / Status Display / Prot
⇧	*Signal: External Blocking of the Trip Command*

Alarm L1	Operation / Status Display / Prot
⇧	*Signal: General-Alarm L1*

Alarm L2	Operation / Status Display / Prot
⇧	*Signal: General-Alarm L2*

Alarm L3	Operation / Status Display / Prot
⇧	*Signal: General-Alarm L3*

Alarm G	Operation / Status Display / Prot
⇧	*Signal: General-Alarm - Earth fault*

Alarm	Operation / Status Display / Alarms Operation / Status Display / Prot
⇧	*Signal: General Alarm*

Trip L1	Operation / Status Display / Prot
⇧	*Signal: General Trip L1*

Trip L2	Operation / Status Display / Prot
⇧	*Signal: General Trip L2*

Trip L3	Operation / Status Display / Prot
⇧	*Signal: General Trip L3*

Trip G	Operation / Status Display / Prot
⇧	*Signal: General Trip Ground fault*

Trip	Operation / Status Display / Trips Operation / Status Display / Prot
⇧	*Signal: General Trip*

Res FaultNo a GridFaultNo	Operation / Status Display / Prot
⇧	*Signal: Resetting of fault number and grid fault number.*

Fault No.	Operation / Count and RevData / Prot
⇧	*Fault number*

9.5 V[1] ... V[6] [27, 59]

Voltage-stage

9.5.1 V[1] ... V[6]: Device Planning Parameters

Mode	Device planning / Projected Elements	
V>	-, V>, V< Table	*S.3*
Voltage-stage, general operation mode		

Superv. only	Device planning / Definition	
no	no, yes Table	*S.3*
Voltage-stage, if set to “Yes”: Restriction of the function to a supervision functionality, i.e. there is no general alarm, no general trip and no trip command.		

9.5.2 V[1] ... V[6]: Global Parameters

ExBlo1 **ExBlo2**	Protection Para / Global Prot Para / V-Prot / V[1]	
-	- ... Internal test state Table	*P.2*
External blocking of the module, if blocking is activated (allowed) within a parameter set and if the state of the assigned signal is true.		

ExBlo TripCmd	Protection Para / Global Prot Para / V-Prot / V[1]	
• Only available if: Superv. only = no -	- ... Internal test state Table	*P.2*
External blocking of the Trip Command of the module/the stage, if blocking is activated (allowed) within a parameter set and if the state of the assigned signal is true.		

9.5.3 V[1] ... V[6]: Setting Group Parameters

Function	Protection Para / Set 1 / V-Prot / V[1] Protection Para / Set 2 / V-Prot / V[1] Protection Para / Set 3 / V-Prot / V[1] Protection Para / Set 4 / V-Prot / V[1]	
Active	Inactive, Active Table	*P.2*
Permanent activation or deactivation of module/stage.		

ExBlo Fc	Protection Para / Set 1 / V-Prot / V[1] Protection Para / Set 2 / V-Prot / V[1] Protection Para / Set 3 / V-Prot / V[1] Protection Para / Set 4 / V-Prot / V[1]	
Inactive	Inactive, Active Table	*P.2*
Activate (allow) or inactivate (disallow) blocking of the module/stage. This parameter is only effective if a signal is assigned to the corresponding global protection parameter. If the signal becomes true, those modules/stages are blocked that are parameterized "ExBlo Fc=active".		

Blo TripCmd	Protection Para / Set 1 / V-Prot / V[1] Protection Para / Set 2 / V-Prot / V[1] Protection Para / Set 3 / V-Prot / V[1] Protection Para / Set 4 / V-Prot / V[1]	
• Only available if: Superv. only = no Inactive	Inactive, Active Table	*P.2*
Permanent blocking of the Trip Command of the module/stage.		

ExBlo TripCmd Fc	Protection Para / Set 1 / V-Prot / V[1] Protection Para / Set 2 / V-Prot / V[1] Protection Para / Set 3 / V-Prot / V[1] Protection Para / Set 4 / V-Prot / V[1]	
• Only available if: Superv. only = no Inactive	Inactive, Active Table	*P.2*
Activate (allow) or inactivate (disallow) blocking of the module/stage. This parameter is only effective if a signal is assigned to the corresponding global protection parameter. If the signal becomes true, those modules/stages are blocked that are parameterized "ExBlo TripCmd Fc=active".		

Measuring Mode	Protection Para / Set 1 / V-Prot / V[1] Protection Para / Set 2 / V-Prot / V[1] Protection Para / Set 3 / V-Prot / V[1] Protection Para / Set 4 / V-Prot / V[1]	
Phase to Phase	Adjustable range: • Phase to Ground, Phase to Phase, If: VT con = Phase to Ground • Phase to Phase, If: VT con ≠ Phase to Ground Table	*P.2*
Measuring/Supervision Mode: Determines if the phase-to-phase or phase-to-earth voltages are to be supervised		

Measuring method	Protection Para / Set 1 / V-Prot / V[1] Protection Para / Set 2 / V-Prot / V[1] Protection Para / Set 3 / V-Prot / V[1] Protection Para / Set 4 / V-Prot / V[1]	
Fundamental	Fundamental, True RMS, Vavg Table	*P.2*
Measuring method: fundamental or rms or "sliding average supervision"		

Alarm Mode	Protection Para / Set 1 / V-Prot / V[1] Protection Para / Set 2 / V-Prot / V[1] Protection Para / Set 3 / V-Prot / V[1] Protection Para / Set 4 / V-Prot / V[1]	
any one	any one, any two, all Table	*P.2*
Alarm criterion for the voltage protection stage.		

V>	Protection Para / Set 1 / V-Prot / V[1] Protection Para / Set 2 / V-Prot / V[1] Protection Para / Set 3 / V-Prot / V[1] Protection Para / Set 4 / V-Prot / V[1]	
1.1Vn		*P.2*

If the pickup value is exceeded, the module/element will be started. If the pickup value is exceeded, the module/element will be started.

The definition of Vn is dependent on both the Field Parameter »VT con« and the Setting Group Parameter »Measuring Mode«:

If the measuring inputs of the voltage measuring card are fed with phase-to-ground voltages (»VT con« = "Phase-to-Ground")

then the setting

»Measuring Mode« = "Phase-to-Ground" means that Vn=VTsec/√3, and

»Measuring Mode« = "Phase-to-Phase" means that Vn=VTsec.

if the measuring inputs of the voltage measuring card are fed with phase-to-phase voltages (»VT con« = "Phase-to-Phase")

then only following setting is possible: »Measuring Mode« = "Phase-to-Phase" means that Vn=VTsec.

V> Reset	Protection Para / Set 1 / V-Prot / V[1] Protection Para / Set 2 / V-Prot / V[1] Protection Para / Set 3 / V-Prot / V[1] Protection Para / Set 4 / V-Prot / V[1]	
98.5%	80% ... 99.0%	*P.2*
Drop Out (is in percent of setting)		

V<	Protection Para / Set 1 / V-Prot / V[1] Protection Para / Set 2 / V-Prot / V[1] Protection Para / Set 3 / V-Prot / V[1] Protection Para / Set 4 / V-Prot / V[1]	
0.80Vn		*P.2*
If the pickup value is exceeded, the module/element will be started. If the pickup value is exceeded, the module/element will be started. *The definition of Vn is dependent on both the Field Parameter »VT con« and the Setting Group Parameter »Measuring Mode«:* *If the measuring inputs of the voltage measuring card are fed with phase-to-ground voltages (»VT con« = "Phase-to-Ground")* *then the setting* *»Measuring Mode« = "Phase-to-Ground" means that Vn=VTsec/√3, and* *»Measuring Mode« = "Phase-to-Phase" means that Vn=VTsec.* *if the measuring inputs of the voltage measuring card are fed with phase-to-phase voltages (»VT con« = "Phase-to-Phase")* *then only following setting is possible: »Measuring Mode« = "Phase-to-Phase" means that Vn=VTsec.*	

V< Reset	Protection Para / Set 1 / V-Prot / V[1] Protection Para / Set 2 / V-Prot / V[1] Protection Para / Set 3 / V-Prot / V[1] Protection Para / Set 4 / V-Prot / V[1]	
101.5%	101% ... 110.0%	*P.2*
Drop Out (is in percent of setting)		

t	Protection Para / Set 1 / V-Prot / V[1] Protection Para / Set 2 / V-Prot / V[1] Protection Para / Set 3 / V-Prot / V[1] Protection Para / Set 4 / V-Prot / V[1]	
1s	0.00s ... 3000.00s	*P.2*
Tripping delay		

Meas Circuit Superv	Protection Para / Set 1 / V-Prot / V[1] Protection Para / Set 2 / V-Prot / V[1] Protection Para / Set 3 / V-Prot / V[1] Protection Para / Set 4 / V-Prot / V[1]	
Inactive	Inactive, Active Table	*P.2*

Activates the use of the measuring circuit supervision. In this case the module will be blocked if a measuring circuit supervision module (e.g. LOP, VTS) signals a disturbed measuring circuit (e.g. caused by a fuse failure).

9.5.4 V[1] . . . V[6]: Input States

ExBlo1-I (**V[1] . ExBlo1**)	Operation / Status Display / V-Prot / V[1]

Module input state: External blocking1

ExBlo2-I	Operation / Status Display / V-Prot / V[1]

Module input state: External blocking2

ExBlo TripCmd-I	Operation / Status Display / V-Prot / V[1]

- Only available if: Superv. only = no

Module input state: External Blocking of the Trip Command

9.5.5 V[1] . . . V[6]: Signals (Output States)

Active	Operation / Status Display / All Actives Operation / Status Display / V-Prot / V[1]

Signal: active

ExBlo	Operation / Status Display / V-Prot / V[1]

Signal: External Blocking

Blo TripCmd	Operation / Status Display / V-Prot / V[1]

- Only available if: Superv. only = no

Signal: Trip Command blocked

ExBlo TripCmd	Operation / Status Display / V-Prot / V[1]

- Only available if: Superv. only = no

Signal: External Blocking of the Trip Command

Alarm L1	Operation / Status Display / V-Prot / V[1]
⇧	*Signal: Alarm L1*

Alarm L2	Operation / Status Display / V-Prot / V[1]
⇧	*Signal: Alarm L2*

Alarm L3	Operation / Status Display / V-Prot / V[1]
⇧	*Signal: Alarm L3*

Alarm	Operation / Status Display / Alarms Operation / Status Display / V-Prot / V[1]
⇧	*Signal: Alarm voltage stage*

Trip L1	Operation / Status Display / V-Prot / V[1]
⇧	*Signal: General Trip Phase L1*

Trip L2	Operation / Status Display / V-Prot / V[1]
⇧	*Signal: General Trip Phase L2*

Trip L3	Operation / Status Display / V-Prot / V[1]
⇧	*Signal: General Trip Phase L3*

Trip	Operation / Status Display / Trips Operation / Status Display / V-Prot / V[1]
⇧	*Signal: Trip*

TripCmd	Operation / Status Display / TripCmds Operation / Status Display / V-Prot / V[1]
⇧	• Only available if: Superv. only = no *Signal: Trip Command*

9.6 df/dt [81R]

Rate-of-frequency-change.

9.6.1 df/dt: Device Planning Parameters

Mode	Device planning / Projected Elements	
-	-, use Table	*S.3*
Frequency Protection Module, general operation mode		

Superv. only	Device planning / Definition	
no	no, yes Table	*S.3*
Frequency Protection Module, if set to “Yes”: Restriction of the function to a supervision functionality, i.e. there is no general alarm, no general trip and no trip command.		

9.6.2 df/dt: Global Parameters

ExBlo1 **ExBlo2**	Protection Para / Global Prot Para / Intercon-Prot / Mains Decouplg / df/dt	
-	- . . . Internal test state Table	*P.2*
External blocking of the module, if blocking is activated (allowed) within a parameter set and if the state of the assigned signal is true.		

ExBlo TripCmd	Protection Para / Global Prot Para / Intercon-Prot / Mains Decouplg / df/dt	
• Only available if: Superv. only = no -	- . . . Internal test state Table	*P.2*
External blocking of the Trip Command of the module/the stage, if blocking is activated (allowed) within a parameter set and if the state of the assigned signal is true.		

9.6.3 df/dt: Setting Group Parameters

Function	Protection Para / Set 1 / Intercon-Prot / Mains Decouplg / df/dt Protection Para / Set 2 / Intercon-Prot / Mains Decouplg / df/dt Protection Para / Set 3 / Intercon-Prot / Mains Decouplg / df/dt Protection Para / Set 4 / Intercon-Prot / Mains Decouplg / df/dt	
Inactive	Inactive, Active Table	*P.2*
Permanent activation or deactivation of module/stage.		

ExBlo Fc	Protection Para / Set 1 / Intercon-Prot / Mains Decouplg / df/dt Protection Para / Set 2 / Intercon-Prot / Mains Decouplg / df/dt Protection Para / Set 3 / Intercon-Prot / Mains Decouplg / df/dt Protection Para / Set 4 / Intercon-Prot / Mains Decouplg / df/dt	
Inactive	Inactive, Active Table	*P.2*
Activate (allow) or inactivate (disallow) blocking of the module/stage. This parameter is only effective if a signal is assigned to the corresponding global protection parameter. If the signal becomes true, those modules/stages are blocked that are parameterized "ExBlo Fc=active".		

Blo TripCmd	Protection Para / Set 1 / Intercon-Prot / Mains Decouplg / df/dt Protection Para / Set 2 / Intercon-Prot / Mains Decouplg / df/dt Protection Para / Set 3 / Intercon-Prot / Mains Decouplg / df/dt Protection Para / Set 4 / Intercon-Prot / Mains Decouplg / df/dt	
• Only available if: Superv. only = no Inactive	Inactive, Active Table	*P.2*
Permanent blocking of the Trip Command of the module/stage.		

ExBlo TripCmd Fc	Protection Para / Set 1 / Intercon-Prot / Mains Decouplg / df/dt Protection Para / Set 2 / Intercon-Prot / Mains Decouplg / df/dt Protection Para / Set 3 / Intercon-Prot / Mains Decouplg / df/dt Protection Para / Set 4 / Intercon-Prot / Mains Decouplg / df/dt	
• Only available if: Superv. only = no Inactive	Inactive, Active Table	*P.2*
Activate (allow) or inactivate (disallow) blocking of the module/stage. This parameter is only effective if a signal is assigned to the corresponding global protection parameter. If the signal becomes true, those modules/stages are blocked that are parameterized "ExBlo TripCmd Fc=active".		

df/dt	Protection Para / Set 1 / Intercon-Prot / Mains Decouplg / df/dt Protection Para / Set 2 / Intercon-Prot / Mains Decouplg / df/dt Protection Para / Set 3 / Intercon-Prot / Mains Decouplg / df/dt Protection Para / Set 4 / Intercon-Prot / Mains Decouplg / df/dt	
1.000Hz/s	0.100Hz/s ... 10.000Hz/s	*P.2*
Measured value (calculated): Rate-of-frequency-change.		

t-df/dt	Protection Para / Set 1 / Intercon-Prot / Mains Decouplg / df/dt Protection Para / Set 2 / Intercon-Prot / Mains Decouplg / df/dt Protection Para / Set 3 / Intercon-Prot / Mains Decouplg / df/dt Protection Para / Set 4 / Intercon-Prot / Mains Decouplg / df/dt	
1.00s	0.00s . . . 300.00s	*P.2*
Trip delay df/dt		

df/dt mode	Protection Para / Set 1 / Intercon-Prot / Mains Decouplg / df/dt Protection Para / Set 2 / Intercon-Prot / Mains Decouplg / df/dt Protection Para / Set 3 / Intercon-Prot / Mains Decouplg / df/dt Protection Para / Set 4 / Intercon-Prot / Mains Decouplg / df/dt	
absolute df/dt	absolute df/dt, positive df/dt, negative df/dt Table	*P.2*
df/dt mode		

9.6.4 df/dt: Input States

ExBlo1-I (df/dt . ExBlo1)	Operation / Status Display / Intercon-Prot / Mains Decouplg / df/dt
Module input state: External blocking1	

ExBlo2-I	Operation / Status Display / Intercon-Prot / Mains Decouplg / df/dt
Module input state: External blocking2	

ExBlo TripCmd-I	Operation / Status Display / Intercon-Prot / Mains Decouplg / df/dt
• Only available if: Superv. only = no *Module input state: External Blocking of the Trip Command*	

9.6.5 df/dt: Signals (Output States)

Active	Operation / Status Display / All Actives Operation / Status Display / Intercon-Prot / Mains Decouplg / df/dt
Signal: active	

ExBlo	Operation / Status Display / Intercon-Prot / Mains Decouplg / df/dt
Signal: External Blocking	

Blo by V<	Operation / Status Display / Intercon-Prot / Mains Decouplg / df/dt
Signal: Module is blocked by undervoltage.	

Blo TripCmd	Operation / Status Display / Intercon-Prot / Mains Decouplg / df/dt
⇧	• Only available if: Superv. only = no *Signal: Trip Command blocked*

ExBlo TripCmd	Operation / Status Display / Intercon-Prot / Mains Decouplg / df/dt
⇧	• Only available if: Superv. only = no *Signal: External Blocking of the Trip Command*

Alarm	Operation / Status Display / Alarms Operation / Status Display / Intercon-Prot / Mains Decouplg / df/dt
⇧	*Signal: Alarm Frequency Protection (collective signal)*

Trip	Operation / Status Display / Trips Operation / Status Display / Intercon-Prot / Mains Decouplg / df/dt
⇧	*Signal: Trip Frequency Protection (collective signal)*

TripCmd	Operation / Status Display / TripCmds Operation / Status Display / Intercon-Prot / Mains Decouplg / df/dt
⇧	• Only available if: Superv. only = no *Signal: Trip Command*

9.7 delta phi [78V]

Vector surge

9.7.1 delta phi: Device Planning Parameters

Mode	Device planning / Projected Elements	
-	-, use Table	*S.3*
Frequency Protection Module, general operation mode		

Superv. only	Device planning / Definition	
no	no, yes Table	*S.3*
Frequency Protection Module, if set to “Yes”: Restriction of the function to a supervision functionality, i.e. there is no general alarm, no general trip and no trip command.		

9.7.2 delta phi: Global Parameters

ExBlo1 **ExBlo2**	Protection Para / Global Prot Para / Intercon-Prot / Mains Decouplg / delta phi	
-	- . . . Internal test state Table	*P.2*
External blocking of the module, if blocking is activated (allowed) within a parameter set and if the state of the assigned signal is true.		

ExBlo TripCmd	Protection Para / Global Prot Para / Intercon-Prot / Mains Decouplg / delta phi	
• Only available if: Superv. only = no -	- . . . Internal test state Table	*P.2*
External blocking of the Trip Command of the module/the stage, if blocking is activated (allowed) within a parameter set and if the state of the assigned signal is true.		

9.7.3 delta phi: Setting Group Parameters

Function	Protection Para / Set 1 / Intercon-Prot / Mains Decouplg / delta phi Protection Para / Set 2 / Intercon-Prot / Mains Decouplg / delta phi Protection Para / Set 3 / Intercon-Prot / Mains Decouplg / delta phi Protection Para / Set 4 / Intercon-Prot / Mains Decouplg / delta phi	
Inactive	Inactive, Active ↳ Table	*P.2*
Permanent activation or deactivation of module/stage.		

ExBlo Fc	Protection Para / Set 1 / Intercon-Prot / Mains Decouplg / delta phi Protection Para / Set 2 / Intercon-Prot / Mains Decouplg / delta phi Protection Para / Set 3 / Intercon-Prot / Mains Decouplg / delta phi Protection Para / Set 4 / Intercon-Prot / Mains Decouplg / delta phi	
Inactive	Inactive, Active ↳ Table	*P.2*
Activate (allow) or inactivate (disallow) blocking of the module/stage. This parameter is only effective if a signal is assigned to the corresponding global protection parameter. If the signal becomes true, those modules/stages are blocked that are parameterized "ExBlo Fc=active".		

Blo TripCmd	Protection Para / Set 1 / Intercon-Prot / Mains Decouplg / delta phi Protection Para / Set 2 / Intercon-Prot / Mains Decouplg / delta phi Protection Para / Set 3 / Intercon-Prot / Mains Decouplg / delta phi Protection Para / Set 4 / Intercon-Prot / Mains Decouplg / delta phi	
• Only available if: Superv. only = no Inactive	Inactive, Active ↳ Table	*P.2*
Permanent blocking of the Trip Command of the module/stage.		

ExBlo TripCmd Fc	Protection Para / Set 1 / Intercon-Prot / Mains Decouplg / delta phi Protection Para / Set 2 / Intercon-Prot / Mains Decouplg / delta phi Protection Para / Set 3 / Intercon-Prot / Mains Decouplg / delta phi Protection Para / Set 4 / Intercon-Prot / Mains Decouplg / delta phi	
• Only available if: Superv. only = no Inactive	Inactive, Active ↳ Table	*P.2*
Activate (allow) or inactivate (disallow) blocking of the module/stage. This parameter is only effective if a signal is assigned to the corresponding global protection parameter. If the signal becomes true, those modules/stages are blocked that are parameterized "ExBlo TripCmd Fc=active".		

delta phi	Protection Para / Set 1 / Intercon-Prot / Mains Decouplg / delta phi Protection Para / Set 2 / Intercon-Prot / Mains Decouplg / delta phi Protection Para / Set 3 / Intercon-Prot / Mains Decouplg / delta phi Protection Para / Set 4 / Intercon-Prot / Mains Decouplg / delta phi	
10°	1° ... 30°	*P.2*
Measured value (calculated): Vector surge		

9.7.4 delta phi: Input States

ExBlo1-I (⮡ delta phi . ExBlo1)	Operation / Status Display / Intercon-Prot / Mains Decouplg / delta phi
	Module input state: External blocking1

ExBlo2-I	Operation / Status Display / Intercon-Prot / Mains Decouplg / delta phi
	Module input state: External blocking2

ExBlo TripCmd-I	Operation / Status Display / Intercon-Prot / Mains Decouplg / delta phi
	• Only available if: Superv. only = no *Module input state: External Blocking of the Trip Command*

9.7.5 delta phi: Signals (Output States)

Active	Operation / Status Display / All Actives Operation / Status Display / Intercon-Prot / Mains Decouplg / delta phi
	Signal: active

ExBlo	Operation / Status Display / Intercon-Prot / Mains Decouplg / delta phi
	Signal: External Blocking

Blo by V<	Operation / Status Display / Intercon-Prot / Mains Decouplg / delta phi
	Signal: Module is blocked by undervoltage.

Blo TripCmd	Operation / Status Display / Intercon-Prot / Mains Decouplg / delta phi
	• Only available if: Superv. only = no *Signal: Trip Command blocked*

ExBlo TripCmd	Operation / Status Display / Intercon-Prot / Mains Decouplg / delta phi
	• Only available if: Superv. only = no *Signal: External Blocking of the Trip Command*

Alarm	Operation / Status Display / Alarms Operation / Status Display / Intercon-Prot / Mains Decouplg / delta phi
	Signal: Alarm Frequency Protection (collective signal)

Trip	Operation / Status Display / Trips Operation / Status Display / Intercon-Prot / Mains Decouplg / delta phi
⇧	*Signal: Trip Frequency Protection (collective signal)*

TripCmd	Operation / Status Display / TripCmds Operation / Status Display / Intercon-Prot / Mains Decouplg / delta phi
⇧	• Only available if: Superv. only = no *Signal: Trip Command*

9.8 Intertripping

9.8.1 Intertripping: Device Planning Parameters

Mode	Device planning / Projected Elements	
-	-, use Table	*S.3*
External Protection - Module, general operation mode		

9.8.2 Intertripping: Global Parameters

ExBlo1 **ExBlo2**	Protection Para / Global Prot Para / Intercon-Prot / Mains Decouplg / Intertripping	
-	- . . . Internal test state Table	*P.2*
External blocking of the module, if blocking is activated (allowed) within a parameter set and if the state of the assigned signal is true.		

ExBlo TripCmd	Protection Para / Global Prot Para / Intercon-Prot / Mains Decouplg / Intertripping	
-	- . . . Internal test state Table	*P.2*
External blocking of the Trip Command of the module/the stage, if blocking is activated (allowed) within a parameter set and if the state of the assigned signal is true.		

Alarm	Protection Para / Global Prot Para / Intercon-Prot / Mains Decouplg / Intertripping	
-	- . . . Internal test state Table	*P.2*
Assignment for External Alarm		

Trip	Protection Para / Global Prot Para / Intercon-Prot / Mains Decouplg / Intertripping	
-	- . . . Internal test state Table	*P.2*
External trip of the CB if the state of the assigned signal is true.		

9.8.3 Intertripping: Setting Group Parameters

Function	Protection Para / Set 1 / Intercon-Prot / Mains Decouplg / Intertripping Protection Para / Set 2 / Intercon-Prot / Mains Decouplg / Intertripping Protection Para / Set 3 / Intercon-Prot / Mains Decouplg / Intertripping Protection Para / Set 4 / Intercon-Prot / Mains Decouplg / Intertripping	
Inactive	Inactive, Active Table	*P.2*
Permanent activation or deactivation of module/stage.		

ExBlo Fc	Protection Para / Set 1 / Intercon-Prot / Mains Decouplg / Intertripping Protection Para / Set 2 / Intercon-Prot / Mains Decouplg / Intertripping Protection Para / Set 3 / Intercon-Prot / Mains Decouplg / Intertripping Protection Para / Set 4 / Intercon-Prot / Mains Decouplg / Intertripping	
Inactive	Inactive, Active Table	*P.2*
Activate (allow) or inactivate (disallow) blocking of the module/stage. This parameter is only effective if a signal is assigned to the corresponding global protection parameter. If the signal becomes true, those modules/stages are blocked that are parameterized "ExBlo Fc=active".		

Blo TripCmd	Protection Para / Set 1 / Intercon-Prot / Mains Decouplg / Intertripping Protection Para / Set 2 / Intercon-Prot / Mains Decouplg / Intertripping Protection Para / Set 3 / Intercon-Prot / Mains Decouplg / Intertripping Protection Para / Set 4 / Intercon-Prot / Mains Decouplg / Intertripping	
Inactive	Inactive, Active Table	*P.2*
Permanent blocking of the Trip Command of the module/stage.		

ExBlo TripCmd Fc	Protection Para / Set 1 / Intercon-Prot / Mains Decouplg / Intertripping Protection Para / Set 2 / Intercon-Prot / Mains Decouplg / Intertripping Protection Para / Set 3 / Intercon-Prot / Mains Decouplg / Intertripping Protection Para / Set 4 / Intercon-Prot / Mains Decouplg / Intertripping	
Inactive	Inactive, Active Table	*P.2*
Activate (allow) or inactivate (disallow) blocking of the module/stage. This parameter is only effective if a signal is assigned to the corresponding global protection parameter. If the signal becomes true, those modules/stages are blocked that are parameterized "ExBlo TripCmd Fc=active".		

9.8.4 Intertripping: Input States

ExBlo1-I **(Intertripping . ExBlo1)**	Operation / Status Display / Intercon-Prot / Mains Decouplg / Intertripping
Module input state: External blocking1	

ExBlo2-I	Operation / Status Display / Intercon-Prot / Mains Decouplg / Intertripping
⇩	*Module input state: External blocking2*

ExBlo TripCmd-I	Operation / Status Display / Intercon-Prot / Mains Decouplg / Intertripping
⇩	*Module input state: External Blocking of the Trip Command*

Alarm-I **(↳ Intertripping . Alarm)**	Operation / Status Display / Intercon-Prot / Mains Decouplg / Intertripping
⇩	*Module input state: Alarm*

Trip-I **(↳ Intertripping . Trip)**	Operation / Status Display / Intercon-Prot / Mains Decouplg / Intertripping
⇩	*Module input state: Trip*

9.8.5 Intertripping: Signals (Output States)

Active	Operation / Status Display / All Actives Operation / Status Display / Intercon-Prot / Mains Decouplg / Intertripping
⇧	*Signal: active*

ExBlo	Operation / Status Display / Intercon-Prot / Mains Decouplg / Intertripping
⇧	*Signal: External Blocking*

Blo TripCmd	Operation / Status Display / Intercon-Prot / Mains Decouplg / Intertripping
⇧	*Signal: Trip Command blocked*

ExBlo TripCmd	Operation / Status Display / Intercon-Prot / Mains Decouplg / Intertripping
⇧	*Signal: External Blocking of the Trip Command*

Alarm	Operation / Status Display / Alarms Operation / Status Display / Intercon-Prot / Mains Decouplg / Intertripping
⇧	*Signal: Alarm*

Trip	Operation / Status Display / Trips Operation / Status Display / Intercon-Prot / Mains Decouplg / Intertripping
⇧	*Signal: Trip*

TripCmd	Operation / Status Display / TripCmds Operation / Status Display / Intercon-Prot / Mains Decouplg / Intertripping
⇧	*Signal: Trip Command*

9.9 LVRT[1], LVRT[2] [27]

Low Voltage Ride Through

9.9.1 LVRT[1], LVRT[2]: Device Planning Parameters

Mode	Device planning / Projected Elements	
-	-, use Table	*S.3*
general operation mode		

Superv. only	Device planning / Definition	
no	no, yes Table	*S.3*
Low Voltage Ride Through, if set to “Yes”: Restriction of the function to a supervision functionality, i.e. there is no general alarm, no general trip and no trip command.		

9.9.2 LVRT[1], LVRT[2]: Global Parameters

ExBlo1 **ExBlo2**	Protection Para / Global Prot Para / Intercon-Prot / LVRT[1]	
-	- . . . Internal test state Table	*P.2*
External blocking of the module, if blocking is activated (allowed) within a parameter set and if the state of the assigned signal is true.		

ExBlo TripCmd	Protection Para / Global Prot Para / Intercon-Prot / LVRT[1]	
• Only available if: Superv. only = no -	- . . . Internal test state Table	*P.2*
External blocking of the Trip Command of the module/the stage, if blocking is activated (allowed) within a parameter set and if the state of the assigned signal is true.		

9.9.3 LVRT[1], LVRT[2]: Setting Group Parameters

Function	Protection Para / Set 1 / Intercon-Prot / LVRT[1] / General Settings Protection Para / Set 2 / Intercon-Prot / LVRT[1] / General Settings Protection Para / Set 3 / Intercon-Prot / LVRT[1] / General Settings Protection Para / Set 4 / Intercon-Prot / LVRT[1] / General Settings	
Inactive	Inactive, Active Table	*P.2*
Permanent activation or deactivation of module/stage.		

ExBlo Fc	Protection Para / Set 1 / Intercon-Prot / LVRT[1] / General Settings Protection Para / Set 2 / Intercon-Prot / LVRT[1] / General Settings Protection Para / Set 3 / Intercon-Prot / LVRT[1] / General Settings Protection Para / Set 4 / Intercon-Prot / LVRT[1] / General Settings	
Inactive	Inactive, Active Table	*P.2*
Activate (allow) or inactivate (disallow) blocking of the module/stage. This parameter is only effective if a signal is assigned to the corresponding global protection parameter. If the signal becomes true, those modules/stages are blocked that are parameterized "ExBlo Fc=active".		

Blo TripCmd	Protection Para / Set 1 / Intercon-Prot / LVRT[1] / General Settings Protection Para / Set 2 / Intercon-Prot / LVRT[1] / General Settings Protection Para / Set 3 / Intercon-Prot / LVRT[1] / General Settings Protection Para / Set 4 / Intercon-Prot / LVRT[1] / General Settings	
• Only available if: Superv. only = no Inactive	Inactive, Active Table	*P.2*
Permanent blocking of the Trip Command of the module/stage.		

ExBlo TripCmd Fc	Protection Para / Set 1 / Intercon-Prot / LVRT[1] / General Settings Protection Para / Set 2 / Intercon-Prot / LVRT[1] / General Settings Protection Para / Set 3 / Intercon-Prot / LVRT[1] / General Settings Protection Para / Set 4 / Intercon-Prot / LVRT[1] / General Settings	
• Only available if: Superv. only = no Inactive	Inactive, Active Table	*P.2*
Activate (allow) or inactivate (disallow) blocking of the module/stage. This parameter is only effective if a signal is assigned to the corresponding global protection parameter. If the signal becomes true, those modules/stages are blocked that are parameterized "ExBlo TripCmd Fc=active".		

Measuring Mode	Protection Para / Set 1 / Intercon-Prot / LVRT[1] / General Settings Protection Para / Set 2 / Intercon-Prot / LVRT[1] / General Settings Protection Para / Set 3 / Intercon-Prot / LVRT[1] / General Settings Protection Para / Set 4 / Intercon-Prot / LVRT[1] / General Settings	
Phase to Phase	Adjustable range: • Phase to Ground, Phase to Phase, If: VT con = Phase to Ground • Phase to Phase, If: VT con ≠ Phase to Ground Table	*P.2*
Measuring/Supervision Mode: Determines if the phase-to-phase or phase-to-earth voltages are to be supervised		

Measuring method	Protection Para / Set 1 / Intercon-Prot / LVRT[1] / General Settings Protection Para / Set 2 / Intercon-Prot / LVRT[1] / General Settings Protection Para / Set 3 / Intercon-Prot / LVRT[1] / General Settings Protection Para / Set 4 / Intercon-Prot / LVRT[1] / General Settings	
Fundamental	Fundamental, True RMS Table	*P.2*
Measuring method: fundamental or rms or 3rd harmonic (only generator protection relays)		

Alarm Mode	Protection Para / Set 1 / Intercon-Prot / LVRT[1] / General Settings Protection Para / Set 2 / Intercon-Prot / LVRT[1] / General Settings Protection Para / Set 3 / Intercon-Prot / LVRT[1] / General Settings Protection Para / Set 4 / Intercon-Prot / LVRT[1] / General Settings	
any one	any one, any two, all, only 2 Table	*P.2*
Alarm criterion for the voltage protection stage.		

Meas Circuit Superv	Protection Para / Set 1 / Intercon-Prot / LVRT[1] / General Settings Protection Para / Set 2 / Intercon-Prot / LVRT[1] / General Settings Protection Para / Set 3 / Intercon-Prot / LVRT[1] / General Settings Protection Para / Set 4 / Intercon-Prot / LVRT[1] / General Settings	
Inactive	Inactive, Active Table	*P.2*
Activates the use of the measuring circuit supervision. In this case the module will be blocked if a measuring circuit supervision module (e.g. LOP, VTS) signals a disturbed measuring circuit (e.g. caused by a fuse failure).		

AR controlled LVRT	Protection Para / Set 1 / Intercon-Prot / LVRT[1] / General Settings Protection Para / Set 2 / Intercon-Prot / LVRT[1] / General Settings Protection Para / Set 3 / Intercon-Prot / LVRT[1] / General Settings Protection Para / Set 4 / Intercon-Prot / LVRT[1] / General Settings	
Inactive	Inactive, Active Table	*P.2*
Activates the supervision of the number of voltage dips during a defined time (t-LVRT).		

Number of V dips to trip	Protection Para / Set 1 / Intercon-Prot / LVRT[1] / General Settings Protection Para / Set 2 / Intercon-Prot / LVRT[1] / General Settings Protection Para / Set 3 / Intercon-Prot / LVRT[1] / General Settings Protection Para / Set 4 / Intercon-Prot / LVRT[1] / General Settings	
• Only available if: AR controlled LVRT = Active 1	1 . . . 6	*P.2*
Number of voltage dips until the disconnection signal (trip) will be issued.		

t-LVRT	Protection Para / Set 1 / Intercon-Prot / LVRT[1] / General Settings Protection Para / Set 2 / Intercon-Prot / LVRT[1] / General Settings Protection Para / Set 3 / Intercon-Prot / LVRT[1] / General Settings Protection Para / Set 4 / Intercon-Prot / LVRT[1] / General Settings	
• Only available if: AR controlled LVRT = Active 30.00s	0.00s . . . 3000.00s	*P.2*
This timer defines the supervision interval (window/period) for counting the number of voltage dips to trip (“No of V dips to trip”). The first voltage dip will start the timer. The counted number of voltage dips will be reset if the timer is expired. The timer will also be reset if the maximum “No of V dips to trip” is reached.		

Vstart<	Protection Para / Set 1 / Intercon-Prot / LVRT[1] / LVRT Profile Protection Para / Set 2 / Intercon-Prot / LVRT[1] / LVRT Profile Protection Para / Set 3 / Intercon-Prot / LVRT[1] / LVRT Profile Protection Para / Set 4 / Intercon-Prot / LVRT[1] / LVRT Profile	
0.90Vn		*P.2*
A voltage dip is detected if the measured voltage falls below this threshold.		

Vrecover>	Protection Para / Set 1 / Intercon-Prot / LVRT[1] / LVRT Profile Protection Para / Set 2 / Intercon-Prot / LVRT[1] / LVRT Profile Protection Para / Set 3 / Intercon-Prot / LVRT[1] / LVRT Profile Protection Para / Set 4 / Intercon-Prot / LVRT[1] / LVRT Profile	
0.93Vn		*P.2*
The voltage is recovered if the measured voltage raises above this threshold.		

V(t1)	Protection Para / Set 1 / Intercon-Prot / LVRT[1] / LVRT Profile Protection Para / Set 2 / Intercon-Prot / LVRT[1] / LVRT Profile Protection Para / Set 3 / Intercon-Prot / LVRT[1] / LVRT Profile Protection Para / Set 4 / Intercon-Prot / LVRT[1] / LVRT Profile	
0.00Vn		*P.2*
Voltage value of a point V(t(n)). These points define the LVRT profile.		

t1	Protection Para / Set 1 / Intercon-Prot / LVRT[1] / LVRT Profile Protection Para / Set 2 / Intercon-Prot / LVRT[1] / LVRT Profile Protection Para / Set 3 / Intercon-Prot / LVRT[1] / LVRT Profile Protection Para / Set 4 / Intercon-Prot / LVRT[1] / LVRT Profile	
0.00s	0.00s . . . 20.00s	*P.2*
Point in time for the corresponding voltage value V(t(n)). These points define the LVRT profile.		

V(t2)	Protection Para / Set 1 / Intercon-Prot / LVRT[1] / LVRT Profile Protection Para / Set 2 / Intercon-Prot / LVRT[1] / LVRT Profile Protection Para / Set 3 / Intercon-Prot / LVRT[1] / LVRT Profile Protection Para / Set 4 / Intercon-Prot / LVRT[1] / LVRT Profile	
0.00Vn		*P.2*
Voltage value of a point V(t(n)). These points define the LVRT profile.		

t2	Protection Para / Set 1 / Intercon-Prot / LVRT[1] / LVRT Profile Protection Para / Set 2 / Intercon-Prot / LVRT[1] / LVRT Profile Protection Para / Set 3 / Intercon-Prot / LVRT[1] / LVRT Profile Protection Para / Set 4 / Intercon-Prot / LVRT[1] / LVRT Profile	
0.15s	0.00s ... 20.00s	*P.2*
Point in time for the corresponding voltage value V(t(n)). These points define the LVRT profile.		

V(t3)	Protection Para / Set 1 / Intercon-Prot / LVRT[1] / LVRT Profile Protection Para / Set 2 / Intercon-Prot / LVRT[1] / LVRT Profile Protection Para / Set 3 / Intercon-Prot / LVRT[1] / LVRT Profile Protection Para / Set 4 / Intercon-Prot / LVRT[1] / LVRT Profile	
0.70Vn		*P.2*
Voltage value of a point V(t(n)). These points define the LVRT profile.		

t3	Protection Para / Set 1 / Intercon-Prot / LVRT[1] / LVRT Profile Protection Para / Set 2 / Intercon-Prot / LVRT[1] / LVRT Profile Protection Para / Set 3 / Intercon-Prot / LVRT[1] / LVRT Profile Protection Para / Set 4 / Intercon-Prot / LVRT[1] / LVRT Profile	
0.15s	0.00s ... 20.00s	*P.2*
Point in time for the corresponding voltage value V(t(n)). These points define the LVRT profile.		

V(t4)	Protection Para / Set 1 / Intercon-Prot / LVRT[1] / LVRT Profile Protection Para / Set 2 / Intercon-Prot / LVRT[1] / LVRT Profile Protection Para / Set 3 / Intercon-Prot / LVRT[1] / LVRT Profile Protection Para / Set 4 / Intercon-Prot / LVRT[1] / LVRT Profile	
0.70Vn		*P.2*
Voltage value of a point V(t(n)). These points define the LVRT profile.		

t4	Protection Para / Set 1 / Intercon-Prot / LVRT[1] / LVRT Profile Protection Para / Set 2 / Intercon-Prot / LVRT[1] / LVRT Profile Protection Para / Set 3 / Intercon-Prot / LVRT[1] / LVRT Profile Protection Para / Set 4 / Intercon-Prot / LVRT[1] / LVRT Profile	
0.70s	0.00s ... 20.00s	*P.2*
Point in time for the corresponding voltage value V(t(n)). These points define the LVRT profile.		

V(t5)	Protection Para / Set 1 / Intercon-Prot / LVRT[1] / LVRT Profile Protection Para / Set 2 / Intercon-Prot / LVRT[1] / LVRT Profile Protection Para / Set 3 / Intercon-Prot / LVRT[1] / LVRT Profile Protection Para / Set 4 / Intercon-Prot / LVRT[1] / LVRT Profile	
0.90Vn		*P.2*
Voltage value of a point V(t(n)). These points define the LVRT profile.		

t5	Protection Para / Set 1 / Intercon-Prot / LVRT[1] / LVRT Profile Protection Para / Set 2 / Intercon-Prot / LVRT[1] / LVRT Profile Protection Para / Set 3 / Intercon-Prot / LVRT[1] / LVRT Profile Protection Para / Set 4 / Intercon-Prot / LVRT[1] / LVRT Profile	
1.50s	0.00s . . . 20.00s	*P.2*
Point in time for the corresponding voltage value V(t(n)). These points define the LVRT profile.		

V(t6)	Protection Para / Set 1 / Intercon-Prot / LVRT[1] / LVRT Profile Protection Para / Set 2 / Intercon-Prot / LVRT[1] / LVRT Profile Protection Para / Set 3 / Intercon-Prot / LVRT[1] / LVRT Profile Protection Para / Set 4 / Intercon-Prot / LVRT[1] / LVRT Profile	
0.90Vn		*P.2*
Voltage value of a point V(t(n)). These points define the LVRT profile.		

t6	Protection Para / Set 1 / Intercon-Prot / LVRT[1] / LVRT Profile Protection Para / Set 2 / Intercon-Prot / LVRT[1] / LVRT Profile Protection Para / Set 3 / Intercon-Prot / LVRT[1] / LVRT Profile Protection Para / Set 4 / Intercon-Prot / LVRT[1] / LVRT Profile	
3.00s	0.00s . . . 20.00s	*P.2*
Point in time for the corresponding voltage value V(t(n)). These points define the LVRT profile.		

V(t7)	Protection Para / Set 1 / Intercon-Prot / LVRT[1] / LVRT Profile Protection Para / Set 2 / Intercon-Prot / LVRT[1] / LVRT Profile Protection Para / Set 3 / Intercon-Prot / LVRT[1] / LVRT Profile Protection Para / Set 4 / Intercon-Prot / LVRT[1] / LVRT Profile	
0.90Vn		*P.2*
Voltage value of a point V(t(n)). These points define the LVRT profile.		

t7	Protection Para / Set 1 / Intercon-Prot / LVRT[1] / LVRT Profile Protection Para / Set 2 / Intercon-Prot / LVRT[1] / LVRT Profile Protection Para / Set 3 / Intercon-Prot / LVRT[1] / LVRT Profile Protection Para / Set 4 / Intercon-Prot / LVRT[1] / LVRT Profile	
3.00s	0.00s . . . 20.00s	*P.2*
Point in time for the corresponding voltage value V(t(n)). These points define the LVRT profile.		

V(t8)	Protection Para / Set 1 / Intercon-Prot / LVRT[1] / LVRT Profile Protection Para / Set 2 / Intercon-Prot / LVRT[1] / LVRT Profile Protection Para / Set 3 / Intercon-Prot / LVRT[1] / LVRT Profile Protection Para / Set 4 / Intercon-Prot / LVRT[1] / LVRT Profile	
0.90Vn		*P.2*
Voltage value of a point V(t(n)). These points define the LVRT profile.		

t8	Protection Para / Set 1 / Intercon-Prot / LVRT[1] / LVRT Profile Protection Para / Set 2 / Intercon-Prot / LVRT[1] / LVRT Profile Protection Para / Set 3 / Intercon-Prot / LVRT[1] / LVRT Profile Protection Para / Set 4 / Intercon-Prot / LVRT[1] / LVRT Profile	
3.00s	0.00s . . . 20.00s	*P.2*
Point in time for the corresponding voltage value V(t(n)). These points define the LVRT profile.		

V(t9)	Protection Para / Set 1 / Intercon-Prot / LVRT[1] / LVRT Profile Protection Para / Set 2 / Intercon-Prot / LVRT[1] / LVRT Profile Protection Para / Set 3 / Intercon-Prot / LVRT[1] / LVRT Profile Protection Para / Set 4 / Intercon-Prot / LVRT[1] / LVRT Profile	
0.90Vn		*P.2*
Voltage value of a point V(t(n)). These points define the LVRT profile.		

t9	Protection Para / Set 1 / Intercon-Prot / LVRT[1] / LVRT Profile Protection Para / Set 2 / Intercon-Prot / LVRT[1] / LVRT Profile Protection Para / Set 3 / Intercon-Prot / LVRT[1] / LVRT Profile Protection Para / Set 4 / Intercon-Prot / LVRT[1] / LVRT Profile	
3.00s	0.00s . . . 20.00s	*P.2*
Point in time for the corresponding voltage value V(t(n)). These points define the LVRT profile.		

V(t10)	Protection Para / Set 1 / Intercon-Prot / LVRT[1] / LVRT Profile Protection Para / Set 2 / Intercon-Prot / LVRT[1] / LVRT Profile Protection Para / Set 3 / Intercon-Prot / LVRT[1] / LVRT Profile Protection Para / Set 4 / Intercon-Prot / LVRT[1] / LVRT Profile	
0.90Vn		*P.2*
Voltage value of a point V(t(n)). These points define the LVRT profile.		

t10	Protection Para / Set 1 / Intercon-Prot / LVRT[1] / LVRT Profile Protection Para / Set 2 / Intercon-Prot / LVRT[1] / LVRT Profile Protection Para / Set 3 / Intercon-Prot / LVRT[1] / LVRT Profile Protection Para / Set 4 / Intercon-Prot / LVRT[1] / LVRT Profile	
3.00s	0.00s . . . 20.00s	*P.2*
Point in time for the corresponding voltage value V(t(n)). These points define the LVRT profile.		

9.9.4 LVRT[1], LVRT[2]: Direct Controls

Res LVRT Cr	Operation / Reset	
Inactive	Inactive, Active Table	*P.1*

Reset of the counter for the total number of voltage dips and reset of the counter of the total number of voltage dips that caused a trip.

9.9.5 LVRT[1], LVRT[2]: Input States

ExBlo1-I (**LVRT[1] . ExBlo1**)	Operation / Status Display / Intercon-Prot / LVRT[1]

Module input state: External blocking1

ExBlo2-I	Operation / Status Display / Intercon-Prot / LVRT[1]

Module input state: External blocking2

ExBlo TripCmd-I	Operation / Status Display / Intercon-Prot / LVRT[1]

- Only available if: Superv. only = no

Module input state: External Blocking of the Trip Command

9.9.6 LVRT[1], LVRT[2]: Signals (Output States)

Active	Operation / Status Display / All Actives Operation / Status Display / Intercon-Prot / LVRT[1]

Signal: active

ExBlo	Operation / Status Display / Intercon-Prot / LVRT[1]

Signal: External Blocking

Blo TripCmd	Operation / Status Display / Intercon-Prot / LVRT[1]

- Only available if: Superv. only = no

Signal: Trip Command blocked

ExBlo TripCmd	Operation / Status Display / Intercon-Prot / LVRT[1]

- Only available if: Superv. only = no

Signal: External Blocking of the Trip Command

Alarm L1	Operation / Status Display / Intercon-Prot / LVRT[1]
⇧	*Signal: Alarm L1*

Alarm L2	Operation / Status Display / Intercon-Prot / LVRT[1]
⇧	*Signal: Alarm L2*

Alarm L3	Operation / Status Display / Intercon-Prot / LVRT[1]
⇧	*Signal: Alarm L3*

Alarm	Operation / Status Display / Alarms Operation / Status Display / Intercon-Prot / LVRT[1]
⇧	*Signal: Alarm voltage stage*

Trip L1	Operation / Status Display / Intercon-Prot / LVRT[1]
⇧	*Signal: General Trip Phase L1*

Trip L2	Operation / Status Display / Intercon-Prot / LVRT[1]
⇧	*Signal: General Trip Phase L2*

Trip L3	Operation / Status Display / Intercon-Prot / LVRT[1]
⇧	*Signal: General Trip Phase L3*

Trip	Operation / Status Display / Trips Operation / Status Display / Intercon-Prot / LVRT[1]
⇧	*Signal: Trip*

TripCmd	Operation / Status Display / TripCmds Operation / Status Display / Intercon-Prot / LVRT[1]
⇧	• Only available if: Superv. only = no *Signal: Trip Command*

t-LVRT is running	Operation / Status Display / Intercon-Prot / LVRT[1]
⇧	*Signal: t-LVRT is running*

9.9.7 LVRT[1], LVRT[2]: Counters

Num Vdips in t-LVRT	Operation / Count and RevData / LVRT[1]
#	*Number of Voltage dips during t-LVRT*

Cr Tot Numb of Vdips	Operation / Count and RevData / LVRT[1]
#	*Counter Total number of voltage dips.*

Cr Num Vdips to Trip	Operation / Count and RevData / LVRT[1]
#	*Counter Total number of voltage dips that caused a Trip*

9.10 VG[1], VG[2] [27A, 59N,A]

Residual voltage-Stage

9.10.1 VG[1], VG[2]: Device Planning Parameters

Mode	Device planning / Projected Elements	
-	-, V>, V< Table	*S.3*
Residual voltage-Stage, general operation mode		

Superv. only	Device planning / Definition	
no	no, yes Table	*S.3*
Residual voltage-Stage, if set to “Yes”: Restriction of the function to a supervision functionality, i.e. there is no general alarm, no general trip and no trip command.		

9.10.2 VG[1], VG[2]: Global Parameters

ExBlo1 **ExBlo2**	Protection Para / Global Prot Para / V-Prot / VG[1]	
-	- . . . Internal test state Table	*P.2*
External blocking of the module, if blocking is activated (allowed) within a parameter set and if the state of the assigned signal is true.		

ExBlo TripCmd	Protection Para / Global Prot Para / V-Prot / VG[1]	
• Only available if: Superv. only = no -	- . . . Internal test state Table	*P.2*
External blocking of the Trip Command of the module/the stage, if blocking is activated (allowed) within a parameter set and if the state of the assigned signal is true.		

9.10.3 VG[1], VG[2]: Setting Group Parameters

Function	Protection Para / Set 1 / V-Prot / VG[1] Protection Para / Set 2 / V-Prot / VG[1] Protection Para / Set 3 / V-Prot / VG[1] Protection Para / Set 4 / V-Prot / VG[1]	
Inactive	Inactive, Active Table	*P.2*
Permanent activation or deactivation of module/stage.		

ExBlo Fc	Protection Para / Set 1 / V-Prot / VG[1] Protection Para / Set 2 / V-Prot / VG[1] Protection Para / Set 3 / V-Prot / VG[1] Protection Para / Set 4 / V-Prot / VG[1]	
Inactive	Inactive, Active Table	*P.2*
Activate (allow) or inactivate (disallow) blocking of the module/stage. This parameter is only effective if a signal is assigned to the corresponding global protection parameter. If the signal becomes true, those modules/stages are blocked that are parameterized "ExBlo Fc=active".		

Blo TripCmd	Protection Para / Set 1 / V-Prot / VG[1] Protection Para / Set 2 / V-Prot / VG[1] Protection Para / Set 3 / V-Prot / VG[1] Protection Para / Set 4 / V-Prot / VG[1]	
• Only available if: Superv. only = no Inactive	Inactive, Active Table	*P.2*
Permanent blocking of the Trip Command of the module/stage.		

ExBlo TripCmd Fc	Protection Para / Set 1 / V-Prot / VG[1] Protection Para / Set 2 / V-Prot / VG[1] Protection Para / Set 3 / V-Prot / VG[1] Protection Para / Set 4 / V-Prot / VG[1]	
• Only available if: Superv. only = no Inactive	Inactive, Active Table	*P.2*
Activate (allow) or inactivate (disallow) blocking of the module/stage. This parameter is only effective if a signal is assigned to the corresponding global protection parameter. If the signal becomes true, those modules/stages are blocked that are parameterized "ExBlo TripCmd Fc=active".		

VG Source	Protection Para / Set 1 / V-Prot / VG[1] Protection Para / Set 2 / V-Prot / VG[1] Protection Para / Set 3 / V-Prot / VG[1] Protection Para / Set 4 / V-Prot / VG[1]	
measured	Adjustable range: • measured, calculated, If: VT con = Phase to Ground • measured, If: VT con ≠ Phase to Ground Table	*P.2*
Selection if VG is measured or calculated (neutral voltage or residual voltage)		

Measuring method	Protection Para / Set 1 / V-Prot / VG[1] Protection Para / Set 2 / V-Prot / VG[1] Protection Para / Set 3 / V-Prot / VG[1] Protection Para / Set 4 / V-Prot / VG[1]	
Fundamental	Fundamental, True RMS Table	*P.2*
Measuring method: fundamental or rms or 3rd harmonic (only generator protection relays)		

VG>	Protection Para / Set 1 / V-Prot / VG[1] Protection Para / Set 2 / V-Prot / VG[1] Protection Para / Set 3 / V-Prot / VG[1] Protection Para / Set 4 / V-Prot / VG[1]	
1Vn		*P.2*
If the pickup value is exceeded, the module/stage will be started.		

VG> Reset	Protection Para / Set 1 / V-Prot / VG[1] Protection Para / Set 2 / V-Prot / VG[1] Protection Para / Set 3 / V-Prot / VG[1] Protection Para / Set 4 / V-Prot / VG[1]	
97.0%	80% ... 98.5%	*P.2*
Drop Out (is in percent of setting)		

VG<	Protection Para / Set 1 / V-Prot / VG[1] Protection Para / Set 2 / V-Prot / VG[1] Protection Para / Set 3 / V-Prot / VG[1] Protection Para / Set 4 / V-Prot / VG[1]	
0.8Vn		*P.2*
Undervoltage Threshold		

VG< Reset	Protection Para / Set 1 / V-Prot / VG[1] Protection Para / Set 2 / V-Prot / VG[1] Protection Para / Set 3 / V-Prot / VG[1] Protection Para / Set 4 / V-Prot / VG[1]	
103.0%	101.5% ... 110.0%	*P.2*
Drop Out (is in percent of setting)		

t	Protection Para / Set 1 / V-Prot / VG[1] Protection Para / Set 2 / V-Prot / VG[1] Protection Para / Set 3 / V-Prot / VG[1] Protection Para / Set 4 / V-Prot / VG[1]	
0.00s	0.00s ... 300.00s	*P.2*
Tripping delay		

Meas Circuit Superv	Protection Para / Set 1 / V-Prot / VG[1] Protection Para / Set 2 / V-Prot / VG[1] Protection Para / Set 3 / V-Prot / VG[1] Protection Para / Set 4 / V-Prot / VG[1]	
Inactive	Inactive, Active Table	*P.2*
Activates the use of the measuring circuit supervision. In this case the module will be blocked if a measuring circuit supervision module (e.g. LOP, VTS) signals a disturbed measuring circuit (e.g. caused by a fuse failure).		

9.10.4 VG[1], VG[2]: Input States

ExBlo1-I (VG[1] . ExBlo1)	Operation / Status Display / V-Prot / VG[1]
Module input state: External blocking1	

ExBlo2-I	Operation / Status Display / V-Prot / VG[1]
Module input state: External blocking2	

ExBlo TripCmd-I	Operation / Status Display / V-Prot / VG[1]
• Only available if: Superv. only = no *Module input state: External Blocking of the Trip Command*	

9.10.5 VG[1], VG[2]: Signals (Output States)

Active	Operation / Status Display / All Actives Operation / Status Display / V-Prot / VG[1]
Signal: active	

ExBlo	Operation / Status Display / V-Prot / VG[1]
⇧	*Signal: External Blocking*

Blo TripCmd	Operation / Status Display / V-Prot / VG[1]
⇧	• Only available if: Superv. only = no *Signal: Trip Command blocked*

ExBlo TripCmd	Operation / Status Display / V-Prot / VG[1]
⇧	• Only available if: Superv. only = no *Signal: External Blocking of the Trip Command*

Alarm	Operation / Status Display / Alarms Operation / Status Display / V-Prot / VG[1]
⇧	*Signal: Alarm Residual Voltage Supervision-stage*

Trip	Operation / Status Display / Trips Operation / Status Display / V-Prot / VG[1]
⇧	*Signal: Trip*

TripCmd	Operation / Status Display / TripCmds Operation / Status Display / V-Prot / VG[1]
⇧	• Only available if: Superv. only = no *Signal: Trip Command*

9.11 V012[1] ... V012[6] [47]

Symmetrical Components: Supervision of the Positive Phase Sequence or Negative Phase Sequence

9.11.1 V012[1] ... V012[6]: Device Planning Parameters

Mode	Device planning / Projected Elements	
-	-, V1>, V1<, V2> Table	*S.3*
Unbalance Protection: Supervision of the Voltage System		

Superv. only	Device planning / Definition	
no	no, yes Table	*S.3*
Symmetrical Components: Supervision of the Positive Phase Sequence or Negative Phase Sequence, if set to “Yes”: Restriction of the function to a supervision functionality, i.e. there is no general alarm, no general trip and no trip command.		

9.11.2 V012[1] ... V012[6]: Global Parameters

ExBlo1	Protection Para / Global Prot Para / V-Prot / V012[1]	
-	- ... Internal test state Table	*P.2*
External blocking of the module, if blocking is activated (allowed) within a parameter set and if the state of the assigned signal is true.1		

ExBlo2	Protection Para / Global Prot Para / V-Prot / V012[1]	
-	- ... Internal test state Table	*P.2*
External blocking of the module, if blocking is activated (allowed) within a parameter set and if the state of the assigned signal is true.2		

ExBlo TripCmd	Protection Para / Global Prot Para / V-Prot / V012[1]	
• Only available if: Superv. only = no -	- ... Internal test state Table	*P.2*
External blocking of the Trip Command of the module/the stage, if blocking is activated (allowed) within a parameter set and if the state of the assigned signal is true.		

9.11.3 V012[1] . . . V012[6]: Setting Group Parameters

Function	Protection Para / Set 1 / V-Prot / V012[1] Protection Para / Set 2 / V-Prot / V012[1] Protection Para / Set 3 / V-Prot / V012[1] Protection Para / Set 4 / V-Prot / V012[1]	
Inactive	Inactive, Active Table	*P.2*
Permanent activation or deactivation of module/stage.		

ExBlo Fc	Protection Para / Set 1 / V-Prot / V012[1] Protection Para / Set 2 / V-Prot / V012[1] Protection Para / Set 3 / V-Prot / V012[1] Protection Para / Set 4 / V-Prot / V012[1]	
Inactive	Inactive, Active Table	*P.2*
Activate (allow) or inactivate (disallow) blocking of the module/stage. This parameter is only effective if a signal is assigned to the corresponding global protection parameter. If the signal becomes true, those modules/stages are blocked that are parameterized "ExBlo Fc=active".		

Blo TripCmd	Protection Para / Set 1 / V-Prot / V012[1] Protection Para / Set 2 / V-Prot / V012[1] Protection Para / Set 3 / V-Prot / V012[1] Protection Para / Set 4 / V-Prot / V012[1]	
• Only available if: Superv. only = no Inactive	Inactive, Active Table	*P.2*
Permanent blocking of the Trip Command of the module/stage.		

ExBlo TripCmd Fc	Protection Para / Set 1 / V-Prot / V012[1] Protection Para / Set 2 / V-Prot / V012[1] Protection Para / Set 3 / V-Prot / V012[1] Protection Para / Set 4 / V-Prot / V012[1]	
• Only available if: Superv. only = no Inactive	Inactive, Active Table	*P.2*
Activate (allow) or inactivate (disallow) blocking of the module/stage. This parameter is only effective if a signal is assigned to the corresponding global protection parameter. If the signal becomes true, those modules/stages are blocked that are parameterized "ExBlo TripCmd Fc=active".		

V1>	Protection Para / Set 1 / V-Prot / V012[1] Protection Para / Set 2 / V-Prot / V012[1] Protection Para / Set 3 / V-Prot / V012[1] Protection Para / Set 4 / V-Prot / V012[1]	
1.00Vn		*P.2*
Positive Phase Sequence Overvoltage		

V1> Reset	Protection Para / Set 1 / V-Prot / V012[1] Protection Para / Set 2 / V-Prot / V012[1] Protection Para / Set 3 / V-Prot / V012[1] Protection Para / Set 4 / V-Prot / V012[1]	
97.0%	80% ... 98.5%	*P.2*
Drop Out (is in percent of setting)		

V1<	Protection Para / Set 1 / V-Prot / V012[1] Protection Para / Set 2 / V-Prot / V012[1] Protection Para / Set 3 / V-Prot / V012[1] Protection Para / Set 4 / V-Prot / V012[1]	
1.00Vn		*P.2*
Positive Phase Sequence Undervoltage		

V1< Reset	Protection Para / Set 1 / V-Prot / V012[1] Protection Para / Set 2 / V-Prot / V012[1] Protection Para / Set 3 / V-Prot / V012[1] Protection Para / Set 4 / V-Prot / V012[1]	
103.0%	101.5% ... 110.0%	*P.2*
Drop Out (is in percent of setting)		

V2>	Protection Para / Set 1 / V-Prot / V012[1] Protection Para / Set 2 / V-Prot / V012[1] Protection Para / Set 3 / V-Prot / V012[1] Protection Para / Set 4 / V-Prot / V012[1]	
1.00Vn		*P.2*
Negative Phase Sequence Overvoltage		

V2> Reset	Protection Para / Set 1 / V-Prot / V012[1] Protection Para / Set 2 / V-Prot / V012[1] Protection Para / Set 3 / V-Prot / V012[1] Protection Para / Set 4 / V-Prot / V012[1]	
97.0%	80% ... 98.5%	*P.2*
Drop Out (is in percent of setting)		

%(V2/V1)	Protection Para / Set 1 / V-Prot / V012[1] Protection Para / Set 2 / V-Prot / V012[1] Protection Para / Set 3 / V-Prot / V012[1] Protection Para / Set 4 / V-Prot / V012[1]	
Inactive	Inactive, Active Table	*P.2*
The %(V2/V1) setting is the unbalance trip pickup setting. It is defined by the ratio of negative sequence voltage to positive sequence voltage (% Unbalance=V2/V1). Phase sequence will be taken into account automatically.		

%(V2/V1)	Protection Para / Set 1 / V-Prot / V012[1] Protection Para / Set 2 / V-Prot / V012[1] Protection Para / Set 3 / V-Prot / V012[1] Protection Para / Set 4 / V-Prot / V012[1]	
• Only available if: %(V2/V1) = Active 20%	2% ... 40%	*P.2*
The %(V2/V1) setting is the unbalance trip pickup setting. It is defined by the ratio of negative sequence voltage to positive sequence voltage (% Unbalance=V2/V1). Phase sequence will be taken into account automatically.		

t	Protection Para / Set 1 / V-Prot / V012[1] Protection Para / Set 2 / V-Prot / V012[1] Protection Para / Set 3 / V-Prot / V012[1] Protection Para / Set 4 / V-Prot / V012[1]	
0.00s	0.00s ... 300.00s	*P.2*
Tripping delay		

Meas Circuit Superv	Protection Para / Set 1 / V-Prot / V012[1] Protection Para / Set 2 / V-Prot / V012[1] Protection Para / Set 3 / V-Prot / V012[1] Protection Para / Set 4 / V-Prot / V012[1]	
Inactive	Inactive, Active Table	*P.2*
Activates the use of the measuring circuit supervision. In this case the module will be blocked if a measuring circuit supervision module (e.g. LOP, VTS) signals a disturbed measuring circuit (e.g. caused by a fuse failure).		

9.11.4 V012[1] ... V012[6]: Input States

ExBlo1-I (V012[1] . ExBlo1)	Operation / Status Display / V-Prot / V012[1]
Module input state: External blocking1	

ExBlo2-I (V012[1] . ExBlo2)	Operation / Status Display / V-Prot / V012[1]
Module input state: External blocking2	

ExBlo TripCmd-I	Operation / Status Display / V-Prot / V012[1]
• Only available if: Superv. only = no *Module input state: External Blocking of the Trip Command*	

9.11.5 V012[1] ... V012[6]: Signals (Output States)

Active	Operation / Status Display / All Actives Operation / Status Display / V-Prot / V012[1]
⇧	*Signal: active*

ExBlo	Operation / Status Display / V-Prot / V012[1]
⇧	*Signal: External Blocking*

Blo TripCmd	Operation / Status Display / V-Prot / V012[1]
⇧	• Only available if: Superv. only = no *Signal: Trip Command blocked*

ExBlo TripCmd	Operation / Status Display / V-Prot / V012[1]
⇧	• Only available if: Superv. only = no *Signal: External Blocking of the Trip Command*

Alarm	Operation / Status Display / Alarms Operation / Status Display / V-Prot / V012[1]
⇧	*Signal: Alarm voltage asymmetry*

Trip	Operation / Status Display / Trips Operation / Status Display / V-Prot / V012[1]
⇧	*Signal: Trip*

TripCmd	Operation / Status Display / TripCmds Operation / Status Display / V-Prot / V012[1]
⇧	• Only available if: Superv. only = no *Signal: Trip Command*

9.12 f[1] ... f[6] [81]

Frequency Protection Module

9.12.1 f[1] ... f[6]: Device Planning Parameters

Mode	Device planning / Projected Elements	
f<	- ... delta phi Table	*S.3*
Frequency Protection Module, general operation mode		

Superv. only	Device planning / Definition	
no	no, yes Table	*S.3*
Frequency Protection Module, if set to “Yes”: Restriction of the function to a supervision functionality, i.e. there is no general alarm, no general trip and no trip command.		

9.12.2 f[1] ... f[6]: Global Parameters

ExBlo1 **ExBlo2**	Protection Para / Global Prot Para / f-Prot / f[1]	
-	- ... Internal test state Table	*P.2*
External blocking of the module, if blocking is activated (allowed) within a parameter set and if the state of the assigned signal is true.		

ExBlo TripCmd	Protection Para / Global Prot Para / f-Prot / f[1]	
• Only available if: Superv. only = no -	- ... Internal test state Table	*P.2*
External blocking of the Trip Command of the module/the stage, if blocking is activated (allowed) within a parameter set and if the state of the assigned signal is true.		

9.12.3 f[1] ... f[6]: Setting Group Parameters

Function	Protection Para / Set 1 / f-Prot / f[1] Protection Para / Set 2 / f-Prot / f[1] Protection Para / Set 3 / f-Prot / f[1] Protection Para / Set 4 / f-Prot / f[1]	
Active	Inactive, Active Table	*P.2*

Permanent activation or deactivation of module/stage.

ExBlo Fc	Protection Para / Set 1 / f-Prot / f[1] Protection Para / Set 2 / f-Prot / f[1] Protection Para / Set 3 / f-Prot / f[1] Protection Para / Set 4 / f-Prot / f[1]	
Inactive	Inactive, Active Table	*P.2*

Activate (allow) or inactivate (disallow) blocking of the module/stage. This parameter is only effective if a signal is assigned to the corresponding global protection parameter. If the signal becomes true, those modules/stages are blocked that are parameterized "ExBlo Fc=active".

Blo TripCmd	Protection Para / Set 1 / f-Prot / f[1] Protection Para / Set 2 / f-Prot / f[1] Protection Para / Set 3 / f-Prot / f[1] Protection Para / Set 4 / f-Prot / f[1]	
• Only available if: Superv. only = no Inactive	Inactive, Active Table	*P.2*

Permanent blocking of the Trip Command of the module/stage.

ExBlo TripCmd Fc	Protection Para / Set 1 / f-Prot / f[1] Protection Para / Set 2 / f-Prot / f[1] Protection Para / Set 3 / f-Prot / f[1] Protection Para / Set 4 / f-Prot / f[1]	
• Only available if: Superv. only = no Inactive	Inactive, Active Table	*P.2*

Activate (allow) or inactivate (disallow) blocking of the module/stage. This parameter is only effective if a signal is assigned to the corresponding global protection parameter. If the signal becomes true, those modules/stages are blocked that are parameterized "ExBlo TripCmd Fc=active".

f>	Protection Para / Set 1 / f-Prot / f[1] Protection Para / Set 2 / f-Prot / f[1] Protection Para / Set 3 / f-Prot / f[1] Protection Para / Set 4 / f-Prot / f[1]	
51.00Hz	40.00Hz ... 69.00Hz	*P.2*

Pickup value for overfrequency.

f<	Protection Para / Set 1 / f-Prot / f[1] Protection Para / Set 2 / f-Prot / f[1] Protection Para / Set 3 / f-Prot / f[1] Protection Para / Set 4 / f-Prot / f[1]	
49.00Hz	40.00Hz ... 69.00Hz	*P.2*
Pickup value for underfrequency.		

Freq. drop-off	Protection Para / Set 1 / f-Prot / f[1] Protection Para / Set 2 / f-Prot / f[1] Protection Para / Set 3 / f-Prot / f[1] Protection Para / Set 4 / f-Prot / f[1]	
0.020Hz	0.010Hz ... 0.100Hz	*P.2*
Drop-off for the Frequency function. This setting modifies the shape of the hysteresis that is used for the frequency protection.		

t	Protection Para / Set 1 / f-Prot / f[1] Protection Para / Set 2 / f-Prot / f[1] Protection Para / Set 3 / f-Prot / f[1] Protection Para / Set 4 / f-Prot / f[1]	
1.00s	0.00s ... 3600.00s	*P.2*
Tripping delay		

df/dt	Protection Para / Set 1 / f-Prot / f[1] Protection Para / Set 2 / f-Prot / f[1] Protection Para / Set 3 / f-Prot / f[1] Protection Para / Set 4 / f-Prot / f[1]	
1.000Hz/s	0.100Hz/s ... 10.000Hz/s	*P.2*
Measured value (calculated): Rate-of-frequency-change.		

t-df/dt	Protection Para / Set 1 / f-Prot / f[1] Protection Para / Set 2 / f-Prot / f[1] Protection Para / Set 3 / f-Prot / f[1] Protection Para / Set 4 / f-Prot / f[1]	
1.00s	0.00s ... 300.00s	*P.2*
Trip delay df/dt		

DF	Protection Para / Set 1 / f-Prot / f[1] Protection Para / Set 2 / f-Prot / f[1] Protection Para / Set 3 / f-Prot / f[1] Protection Para / Set 4 / f-Prot / f[1]	
1.00Hz	0.0Hz ... 10.0Hz	*P.2*
Frequency difference for the maximum admissible variation of the mean of the rate of frequency-change. This function is inactive if DF=0.		

DT	Protection Para / Set 1 / f-Prot / f[1] Protection Para / Set 2 / f-Prot / f[1] Protection Para / Set 3 / f-Prot / f[1] Protection Para / Set 4 / f-Prot / f[1]	
1.00s	0.1s ... 10.0s	*P.2*
Time interval of the maximum admissible rate-of-frequency-change.		

df/dt mode	Protection Para / Set 1 / f-Prot / f[1] Protection Para / Set 2 / f-Prot / f[1] Protection Para / Set 3 / f-Prot / f[1] Protection Para / Set 4 / f-Prot / f[1]	
absolute df/dt	absolute df/dt, positive df/dt, negative df/dt Table	*P.2*
df/dt mode		

delta phi	Protection Para / Set 1 / f-Prot / f[1] Protection Para / Set 2 / f-Prot / f[1] Protection Para / Set 3 / f-Prot / f[1] Protection Para / Set 4 / f-Prot / f[1]	
10°	1° ... 30°	*P.2*
Measured value (calculated): Vector surge		

9.12.4 f[1] ... f[6]: Input States

ExBlo1-I (f[1] . ExBlo1)	Operation / Status Display / f-Prot / f[1]
Module input state: External blocking1	

ExBlo2-I	Operation / Status Display / f-Prot / f[1]
Module input state: External blocking2	

ExBlo TripCmd-I	Operation / Status Display / f-Prot / f[1]
• Only available if: Superv. only = no *Module input state: External Blocking of the Trip Command*	

9.12.5 f[1] . . . f[6]: Signals (Output States)

Active	Operation / Status Display / All Actives Operation / Status Display / f-Prot / f[1]
Signal: active	

ExBlo	Operation / Status Display / f-Prot / f[1]
Signal: External Blocking	

Blo by V<	Operation / Status Display / f-Prot / f[1]
Signal: Module is blocked by undervoltage.	

Blo TripCmd	Operation / Status Display / f-Prot / f[1]
• Only available if: Superv. only = no *Signal: Trip Command blocked*	

ExBlo TripCmd	Operation / Status Display / f-Prot / f[1]
• Only available if: Superv. only = no *Signal: External Blocking of the Trip Command*	

Alarm f	Operation / Status Display / f-Prot / f[1]
Signal: Alarm Frequency Protection	

Alarm df/dt | DF/DT	Operation / Status Display / f-Prot / f[1]
Alarm instantaneous or average value of the rate-of-frequency-change	

Alarm delta phi	Operation / Status Display / f-Prot / f[1]
Signal: Alarm Vector Surge	

Alarm	Operation / Status Display / Alarms Operation / Status Display / f-Prot / f[1]
Signal: Alarm Frequency Protection (collective signal)	

Trip f	Operation / Status Display / f-Prot / f[1]
Signal: Frequency has exceeded the limit.	

Trip df/dt | DF/DT	Operation / Status Display / f-Prot / f[1]
Signal: Trip df/dt or DF/DT	

Trip delta phi	Operation / Status Display / f-Prot / f[1]
⇧	*Signal: Trip Vector Surge*

Trip	Operation / Status Display / Trips Operation / Status Display / f-Prot / f[1]
⇧	*Signal: Trip Frequency Protection (collective signal)*

TripCmd	Operation / Status Display / TripCmds Operation / Status Display / f-Prot / f[1]
⇧	• Only available if: Superv. only = no *Signal: Trip Command*

9.13 ReCon[1], ReCon[2]

Reconnection

9.13.1 ReCon[1], ReCon[2]: Device Planning Parameters

Mode	Device planning / Projected Elements	
-	-, use Table	*S.3*
general operation mode		

9.13.2 ReCon[1], ReCon[2]: Global Parameters

ExBlo1 **ExBlo2**	Protection Para / Global Prot Para / Intercon-Prot / ReCon[1] / General Settings	
-	- . . . Internal test state Table	*P.2*
External blocking of the module, if blocking is activated (allowed) within a parameter set and if the state of the assigned signal is true.		

V Ext Release PCC	Protection Para / Global Prot Para / Intercon-Prot / ReCon[1] / General Settings	
-	- . . . Internal test state Table	*P.2*
Release Signal by the Point of Common Coupling. The line-to-line voltage is greater than 95% of VN.		

PCC Fuse Fail VT	Protection Para / Global Prot Para / Intercon-Prot / ReCon[1] / General Settings	
-	- . . . DI 8 Table	*P.2*
Blocking if the fuse of a voltage transformer has tripped at the PCC.		

reconnected	Protection Para / Global Prot Para / Intercon-Prot / ReCon[1] / General Settings	
-	- . . . Internal test state Table	*P.2*
This signal indicates the state "reconnected" (mains parallel).		

Decoupling1 ... **Decoupling6**	Protection Para / Global Prot Para / Intercon-Prot / ReCon[1] / Decoupling	
-	- ... LE80.Out inverted Table	*P.2*

Decoupling function, that triggers the reconnection.

9.13.3 ReCon[1], ReCon[2]: Setting Group Parameters

Function	Protection Para / Set 1 / Intercon-Prot / ReCon[1] / General Settings Protection Para / Set 2 / Intercon-Prot / ReCon[1] / General Settings Protection Para / Set 3 / Intercon-Prot / ReCon[1] / General Settings Protection Para / Set 4 / Intercon-Prot / ReCon[1] / General Settings	
Inactive	Inactive, Active Table	*P.2*

Permanent activation or deactivation of module/stage.

ExBlo Fc	Protection Para / Set 1 / Intercon-Prot / ReCon[1] / General Settings Protection Para / Set 2 / Intercon-Prot / ReCon[1] / General Settings Protection Para / Set 3 / Intercon-Prot / ReCon[1] / General Settings Protection Para / Set 4 / Intercon-Prot / ReCon[1] / General Settings	
Inactive	Inactive, Active Table	*P.2*

Activate (allow) or inactivate (disallow) blocking of the module/stage. This parameter is only effective if a signal is assigned to the corresponding global protection parameter. If the signal becomes true, those modules/stages are blocked that are parameterized "ExBlo Fc=active".

Meas Circuit Superv	Protection Para / Set 1 / Intercon-Prot / ReCon[1] / General Settings Protection Para / Set 2 / Intercon-Prot / ReCon[1] / General Settings Protection Para / Set 3 / Intercon-Prot / ReCon[1] / General Settings Protection Para / Set 4 / Intercon-Prot / ReCon[1] / General Settings	
Inactive	Inactive, Active Table	*P.2*

Activates the use of the measuring circuit supervision. In this case the module will be blocked if a measuring circuit supervision module (e.g. LOP, VTS) signals a disturbed measuring circuit (e.g. caused by a fuse failure).

V Ext Release PCC Fc	Protection Para / Set 1 / Intercon-Prot / ReCon[1] / General Settings Protection Para / Set 2 / Intercon-Prot / ReCon[1] / General Settings Protection Para / Set 3 / Intercon-Prot / ReCon[1] / General Settings Protection Para / Set 4 / Intercon-Prot / ReCon[1] / General Settings	
Inactive	Inactive, Active Table	*P.2*

Activate the release signal of the Point of Common Coupling. The line-to-line voltage is greater than 95% of VN.

Reconnect. Release Cond	Protection Para / Set 1 / Intercon-Prot / ReCon[1] / Release Para Protection Para / Set 2 / Intercon-Prot / ReCon[1] / Release Para Protection Para / Set 3 / Intercon-Prot / ReCon[1] / Release Para Protection Para / Set 4 / Intercon-Prot / ReCon[1] / Release Para	
Both	V Internal Release, V Ext Release PCC, Both Table	*P.2*
This parameter ensures that the mains voltage is recovered.		

PCC Fuse Fail VT Fk	Protection Para / Set 1 / Intercon-Prot / ReCon[1] / Release Para Protection Para / Set 2 / Intercon-Prot / ReCon[1] / Release Para Protection Para / Set 3 / Intercon-Prot / ReCon[1] / Release Para Protection Para / Set 4 / Intercon-Prot / ReCon[1] / Release Para	
Only available if: • Reconnect. Release Cond = V Ext Release PCC • Reconnect. Release Cond = Both Inactive	Inactive, Active Table	*P.2*
Blocking if the fuse of a voltage transformer has tripped at the PCC.		

Measuring method	Protection Para / Set 1 / Intercon-Prot / ReCon[1] / Release Para Protection Para / Set 2 / Intercon-Prot / ReCon[1] / Release Para Protection Para / Set 3 / Intercon-Prot / ReCon[1] / Release Para Protection Para / Set 4 / Intercon-Prot / ReCon[1] / Release Para	
Fundamental	Fundamental, True RMS, Vavg Table	*P.2*
Measuring method: fundamental or rms or "sliding average supervision"		

VLL max Release	Protection Para / Set 1 / Intercon-Prot / ReCon[1] / Release Para Protection Para / Set 2 / Intercon-Prot / ReCon[1] / Release Para Protection Para / Set 3 / Intercon-Prot / ReCon[1] / Release Para Protection Para / Set 4 / Intercon-Prot / ReCon[1] / Release Para	
Only available if: • Reconnect. Release Cond = V Internal Release • Reconnect. Release Cond = Both 1.10Vn	1.00Vn ... 1.50Vn	*P.2*
Maximum voltage (line-to-line) for reclosure (Restoration Voltage)		

VLL min Release	Protection Para / Set 1 / Intercon-Prot / ReCon[1] / Release Para Protection Para / Set 2 / Intercon-Prot / ReCon[1] / Release Para Protection Para / Set 3 / Intercon-Prot / ReCon[1] / Release Para Protection Para / Set 4 / Intercon-Prot / ReCon[1] / Release Para	
Only available if: • Reconnect. Release Cond = V Internal Release • Reconnect. Release Cond = Both 0.95Vn	0.50Vn ... 1.00Vn	*P.2*
Minimum voltage (line-to-line) for reclosure (Restoration Voltage)		

f max Release	Protection Para / Set 1 / Intercon-Prot / ReCon[1] / Release Para Protection Para / Set 2 / Intercon-Prot / ReCon[1] / Release Para Protection Para / Set 3 / Intercon-Prot / ReCon[1] / Release Para Protection Para / Set 4 / Intercon-Prot / ReCon[1] / Release Para	
50.10Hz	40.00Hz ... 69.90Hz	*P.2*
Upper frequency limit for the reclosure		

f min Release	Protection Para / Set 1 / Intercon-Prot / ReCon[1] / Release Para Protection Para / Set 2 / Intercon-Prot / ReCon[1] / Release Para Protection Para / Set 3 / Intercon-Prot / ReCon[1] / Release Para Protection Para / Set 4 / Intercon-Prot / ReCon[1] / Release Para	
49.9Hz	40.00Hz ... 69.90Hz	*P.2*
Lower frequency limit for the reclosure (Restoration Voltage)		

t-Release Blo	Protection Para / Set 1 / Intercon-Prot / ReCon[1] / Release Para Protection Para / Set 2 / Intercon-Prot / ReCon[1] / Release Para Protection Para / Set 3 / Intercon-Prot / ReCon[1] / Release Para Protection Para / Set 4 / Intercon-Prot / ReCon[1] / Release Para	
600s	0.00s ... 3600.00s	*P.2*
Time stage (delay) for the reclosure of the energy resources. The Mains seddle time takes based on exirience approx. 10 - 15 minutes.		

9.13.4 ReCon[1], ReCon[2]: Input States

ExBlo1-I **(ReCon[1] . ExBlo1)**	Operation / Status Display / Intercon-Prot / ReCon[1]
Module input state: External blocking1	

ExBlo2-I	Operation / Status Display / Intercon-Prot / ReCon[1]
Module input state: External blocking2	

V Ext Release PCC-I **(↳ ReCon[1] . V Ext Release PCC)**	Operation / Status Display / Intercon-Prot / ReCon[1]
⇩	*Module input state: Release signal is being generated by the PCC (External Release)*

PCC Fuse Fail VT-I **(↳ ReCon[1] . PCC Fuse Fail VT)**	Operation / Status Display / Intercon-Prot / ReCon[1]
⇩	*State of the module input: Blocking if the fuse of a voltage transformer has tripped at the PCC.*

reconnected-I **(↳ ReCon[1] . reconnected)**	Operation / Status Display / Intercon-Prot / ReCon[1]
⇩	*This signal indicates the state "reconnected" (mains parallel).*

Decoupling1-I **...** **Decoupling6-I** **(↳ ReCon[1] . Decoupling1)**	Operation / Status Display / Intercon-Prot / ReCon[1]
⇩	*Decoupling function, that triggers the reconnection.*

9.13.5 ReCon[1], ReCon[2]: Signals (Output States)

Active	Operation / Status Display / All Actives Operation / Status Display / Intercon-Prot / ReCon[1]
⇧	*Signal: active*

ExBlo	Operation / Status Display / Intercon-Prot / ReCon[1]
⇧	*Signal: External Blocking*

Blo by Meas Circ Superv	Operation / Status Display / Intercon-Prot / ReCon[1]
⇧	*Signal: Module blocked by measuring cirucuit supervision*

Eval Recon-Conditions	Operation / Status Display / Intercon-Prot / ReCon[1]
⇧	*Signal: Evaluation of reconnection conditions after decoupling event*

t-Release running	Operation / Status Display / Intercon-Prot / ReCon[1]
⇧	*Signal: The timer "t-Release" is running. Thus, all conditions for reconnection are fulfilled. After the timer has expired reconnection release will be issued.*

Release Energy Res.	Operation / Status Display / Intercon-Prot / ReCon[1]
⇧	*Signal: Signal: Release Energy Resource.*

V out of range	Operation / Status Display / Intercon-Prot / ReCon[1]
⇧	*Signal: Reconnection release is blocked because voltage is out of range*

f out ouf range	Operation / Status Display / Intercon-Prot / ReCon[1]
⇧	*Signal: Reconnection release is blocked because frequency is out of range*

9.14 Sync [25]

Synchrocheck

9.14.1 Sync: Device Planning Parameters

Mode	Device planning / Projected Elements	
-	-, use Table	*S.3*
Synchrocheck, general operation mode		

9.14.2 Sync: Global Parameters

ExBlo1 **ExBlo2**	Protection Para / Global Prot Para / Intercon-Prot / Sync	
-	- . . . Internal test state Table	*C.2*
External blocking of the module, if blocking is activated (allowed) within a parameter set and if the state of the assigned signal is true.		

Bypass	Protection Para / Global Prot Para / Intercon-Prot / Sync	
-	- . . . LE80.Out inverted Table	*C.2*
The Synchrocheck will be bypassed if the state of the assigned signal (logic input) becomes true.		

CB Pos Detect	Protection Para / Global Prot Para / Intercon-Prot / Sync	
Pos	-, Pos Table	*C.2*
Criterion by which the Circuit Breaker Switch Position is to be detected.		

CBCloseInitiate	Protection Para / Global Prot Para / Intercon-Prot / Sync	
-	- . . . LE80.Out inverted Table	*C.2*
Breaker Close Initiate with synchronism check from any control sources (e.g. HMI / SCADA). If the state of the assigned signal becomes true, a Breaker Close will be initiated (Trigger Source).		

Transformer-Mode	Protection Para / Global Prot Para / Intercon-Prot / Sync	
Inactive	Inactive, Active Table	*C.2*
Activate transformer mode to enable phase and angle corrections for this function.		

V Line / V Bus	Protection Para / Global Prot Para / Intercon-Prot / Sync	
• Only available if: Transformer-Mode = Active 1.000	0.002 ... 500.000	*C.2*
Ratio of the voltage amplitudes between the line and bus side when using transformer mode.		

Angle Correction	Protection Para / Global Prot Para / Intercon-Prot / Sync	
• Only available if: Transformer-Mode = Active 0.0°	-360.0° ... 360.0°	*C.2*
Correction angle resulting from the difference in angle between the line and bus side when using transformer mode.		

9.14.3 Sync: Setting Group Parameters

Function	Protection Para / Set 1 / Intercon-Prot / Sync / General Settings Protection Para / Set 2 / Intercon-Prot / Sync / General Settings Protection Para / Set 3 / Intercon-Prot / Sync / General Settings Protection Para / Set 4 / Intercon-Prot / Sync / General Settings	
Inactive	Inactive, Active Table	*P.2*
Permanent activation or deactivation of module/stage.		

ExBlo Fc	Protection Para / Set 1 / Intercon-Prot / Sync / General Settings Protection Para / Set 2 / Intercon-Prot / Sync / General Settings Protection Para / Set 3 / Intercon-Prot / Sync / General Settings Protection Para / Set 4 / Intercon-Prot / Sync / General Settings	
Inactive	Inactive, Active Table	*P.2*
Activate (allow) or inactivate (disallow) blocking of the module/stage. This parameter is only effective if a signal is assigned to the corresponding global protection parameter. If the signal becomes true, those modules/stages are blocked that are parameterized "ExBlo Fc=active".		

Bypass Fc	Protection Para / Set 1 / Intercon-Prot / Sync / General Settings Protection Para / Set 2 / Intercon-Prot / Sync / General Settings Protection Para / Set 3 / Intercon-Prot / Sync / General Settings Protection Para / Set 4 / Intercon-Prot / Sync / General Settings	
Inactive	Inactive, Active Table	*P.2*
Allowing to bypass the Synchrocheck, if the state signal that is assigned to the parameter with the same name within the Global Parameters (logic input) becomes true.		

SyncMode	Protection Para / Set 1 / Intercon-Prot / Sync / Mode / Times Protection Para / Set 2 / Intercon-Prot / Sync / Mode / Times Protection Para / Set 3 / Intercon-Prot / Sync / Mode / Times Protection Para / Set 4 / Intercon-Prot / Sync / Mode / Times	
System2System	System2System, Generator2System Table	*P.2*
Synchrocheck mode: GENERATOR2SYSTEM = Synchronizing generator to system (breaker close initiate needed). SYSTEM2SYSTEM = SynchronCheck between two systems (Stand-Alone, no breaker info needed)		

t-MaxCBCloseDelay	Protection Para / Set 1 / Intercon-Prot / Sync / Mode / Times Protection Para / Set 2 / Intercon-Prot / Sync / Mode / Times Protection Para / Set 3 / Intercon-Prot / Sync / Mode / Times Protection Para / Set 4 / Intercon-Prot / Sync / Mode / Times	
• Only available if: SyncMode = Generator2System 0.05s	0.00s . . . 300.00s	*P.2*
Maximum circuit breaker close time delay (Only used for GENERATOR-SYSTEM working mode and is critical for a correct synchronized switching)		

t-MaxSyncSuperv	Protection Para / Set 1 / Intercon-Prot / Sync / Mode / Times Protection Para / Set 2 / Intercon-Prot / Sync / Mode / Times Protection Para / Set 3 / Intercon-Prot / Sync / Mode / Times Protection Para / Set 4 / Intercon-Prot / Sync / Mode / Times	
• Only available if: SyncMode = Generator2System 30.00s	0.00s . . . 3000.00s	*P.2*
Synchron-Run timer: Max. time allowed for synchronizing process after a close initiate. Only used for GENERATOR2SYSTEM working mode.		

MinLiveBusVoltage	Protection Para / Set 1 / Intercon-Prot / Sync / DeadLiveVLevels Protection Para / Set 2 / Intercon-Prot / Sync / DeadLiveVLevels Protection Para / Set 3 / Intercon-Prot / Sync / DeadLiveVLevels Protection Para / Set 4 / Intercon-Prot / Sync / DeadLiveVLevels	
0.65Vn		*P.2*
Minimum Live Bus voltage (Live bus detected, when all three phase bus voltages are above this limit).		

MaxDeadBusVoltage	Protection Para / Set 1 / Intercon-Prot / Sync / DeadLiveVLevels Protection Para / Set 2 / Intercon-Prot / Sync / DeadLiveVLevels Protection Para / Set 3 / Intercon-Prot / Sync / DeadLiveVLevels Protection Para / Set 4 / Intercon-Prot / Sync / DeadLiveVLevels	
0.03Vn	0.01Vn ... 1.00Vn	*P.2*
Maximum Dead Bus voltage (Dead bus detected, when all three phase bus voltages are below this limit).		

MinLiveLineVoltage	Protection Para / Set 1 / Intercon-Prot / Sync / DeadLiveVLevels Protection Para / Set 2 / Intercon-Prot / Sync / DeadLiveVLevels Protection Para / Set 3 / Intercon-Prot / Sync / DeadLiveVLevels Protection Para / Set 4 / Intercon-Prot / Sync / DeadLiveVLevels	
0.65Vn		*P.2*
Minimum Live Line voltage (Live line detected, when line voltage above this limit).		

MaxDeadLineVoltage	Protection Para / Set 1 / Intercon-Prot / Sync / DeadLiveVLevels Protection Para / Set 2 / Intercon-Prot / Sync / DeadLiveVLevels Protection Para / Set 3 / Intercon-Prot / Sync / DeadLiveVLevels Protection Para / Set 4 / Intercon-Prot / Sync / DeadLiveVLevels	
0.03Vn	0.01Vn ... 1.00Vn	*P.2*
Maximum Dead Line voltage (Dead Line detected, when line voltage below this limit).		

t-VoltDead	Protection Para / Set 1 / Intercon-Prot / Sync / DeadLiveVLevels Protection Para / Set 2 / Intercon-Prot / Sync / DeadLiveVLevels Protection Para / Set 3 / Intercon-Prot / Sync / DeadLiveVLevels Protection Para / Set 4 / Intercon-Prot / Sync / DeadLiveVLevels	
0.167s	0.000s ... 300.000s	*P.2*
Voltage dead time (A Dead Bus/Line condition will be accepted only if the voltage falls below the set dead voltage levels longer than this time setting).		

MaxVoltageDiff	Protection Para / Set 1 / Intercon-Prot / Sync / Conditions Protection Para / Set 2 / Intercon-Prot / Sync / Conditions Protection Para / Set 3 / Intercon-Prot / Sync / Conditions Protection Para / Set 4 / Intercon-Prot / Sync / Conditions	
0.24Vn	0.01Vn ... 1.00Vn	*P.2*
Maximum voltage difference between bus and line voltage phasors (Delta V)for synchronism (Related to bus voltage secondary rating)		

MaxSlipFrequency	Protection Para / Set 1 / Intercon-Prot / Sync / Conditions Protection Para / Set 2 / Intercon-Prot / Sync / Conditions Protection Para / Set 3 / Intercon-Prot / Sync / Conditions Protection Para / Set 4 / Intercon-Prot / Sync / Conditions	
0.20Hz	0.01Hz ... 2.00Hz	*P.2*
Maximum frequency difference (Slip: Delta f) between bus and line voltage allowed for synchronism		

MaxAngleDiff	Protection Para / Set 1 / Intercon-Prot / Sync / Conditions Protection Para / Set 2 / Intercon-Prot / Sync / Conditions Protection Para / Set 3 / Intercon-Prot / Sync / Conditions Protection Para / Set 4 / Intercon-Prot / Sync / Conditions	
20°	1° ... 60°	*P.2*
Maximum phase angle difference (Delta-Phi in degree) between bus and line voltages allowed for synchronism		

DBDL	Protection Para / Set 1 / Intercon-Prot / Sync / Override Protection Para / Set 2 / Intercon-Prot / Sync / Override Protection Para / Set 3 / Intercon-Prot / Sync / Override Protection Para / Set 4 / Intercon-Prot / Sync / Override	
Inactive	Inactive, Active Table	*P.2*
Enable/disable Dead-Bus AND Dead-Line synchronism overriding		

DBLL	Protection Para / Set 1 / Intercon-Prot / Sync / Override Protection Para / Set 2 / Intercon-Prot / Sync / Override Protection Para / Set 3 / Intercon-Prot / Sync / Override Protection Para / Set 4 / Intercon-Prot / Sync / Override	
Inactive	Inactive, Active Table	*P.2*
Enable/disable Dead-Bus AND Live-Line synchronism overriding		

LBDL	Protection Para / Set 1 / Intercon-Prot / Sync / Override Protection Para / Set 2 / Intercon-Prot / Sync / Override Protection Para / Set 3 / Intercon-Prot / Sync / Override Protection Para / Set 4 / Intercon-Prot / Sync / Override	
Inactive	Inactive, Active Table	*P.2*
Enable/disable Live-Bus AND Dead-Line synchronism overriding		

9.14.4 Sync: Input States

ExBlo1-I **(Sync . ExBlo1)**	Operation / Status Display / Intercon-Prot / Sync
Module input state: External blocking1	

ExBlo2-I	Operation / Status Display / Intercon-Prot / Sync
Module input state: External blocking2	

Bypass-I **(⇨ Sync . Bypass)**	Operation / Status Display / Intercon-Prot / Sync
⇩	*State of the module input: The Synchrocheck will be bypassed if the state of the assigned signal (logic input) becomes true.*

CBCloseInitiate-I **(⇨ Sync . CBCloseInitiate)**	Operation / Status Display / Intercon-Prot / Sync
⇩	*State of the module input: Breaker Close Initiate with synchronism check from any control sources (e.g. HMI / SCADA). If the state of the assigned signal becomes true, a Breaker Close will be initiated (Trigger Source).*

9.14.5 Sync: Signals (Output States)

Active	Operation / Status Display / All Actives Operation / Status Display / Intercon-Prot / Sync
⇧	*Signal: active*

ExBlo	Operation / Status Display / Intercon-Prot / Sync
⇧	*Signal: External Blocking*

LiveBus	Operation / Status Display / Intercon-Prot / Sync
⇧	*Signal: Live-Bus flag: 1=Live-Bus, 0=Voltage is below the LiveBus threshold*

LiveLine	Operation / Status Display / Intercon-Prot / Sync
⇧	*Signal: Live Line flag: 1=Live-Line, 0=Voltage is below the LiveLine threshold*

SynchronRunTiming	Operation / Status Display / Intercon-Prot / Sync
⇧	*Signal: Synchron-Run-timer is timing (This timer starts when Close-Initiate is coming and stops if breaker is closed. Timeout means synchronizing failed.)*

SynchronFailed	Operation / Status Display / Intercon-Prot / Sync
⇧	*Signal: This signal indicates a failed synchronization. It is set for 5s when the circuit breaker is still open after the Synchron-Run-timer has timed out.*

SyncOverridden	Operation / Status Display / Intercon-Prot / Sync
⇧	*Signal:Synchronism Check is overridden because one of the Synchronism overriding conditions (DB/DL or ExtBypass) is met.*

VDiffTooHigh	Operation / Status Display / Intercon-Prot / Sync
⇧	*Signal: Voltage difference between bus and line too high.*

SlipTooHigh	Operation / Status Display / Intercon-Prot / Sync
⇧	*Signal: Frequency difference (slip frequency) between bus and line voltages too high.*

AngleDiffTooHigh	Operation / Status Display / Intercon-Prot / Sync
⇧	*Signal: Phase Angle difference between bus and line voltages too high.*

Sys-in-Sync	Operation / Status Display / Intercon-Prot / Sync
⇧	*Signal: Bus and line voltages are in synchronism according to the system synchronism criteria.*

Ready to Close	Operation / Status Display / Intercon-Prot / Sync
⇧	*Signal: Ready to Close*

9.14.6 Sync: Values

Slip Freq	Operation / Measured Values / Synchronism
⟍	*Slip frequency*

Volt Diff	Operation / Measured Values / Synchronism
⟍	*Voltage difference between bus and line.*

Angle Diff	Operation / Measured Values / Synchronism
⟍	*Angle difference between bus and line voltages.*

f Bus	Operation / Measured Values / Synchronism
⟍	*Bus frequency*

f Line	Operation / Measured Values / Synchronism
⟍	*Line frequency*

V Bus	Operation / Measured Values / Synchronism
⟍	*Bus Voltage*

V Line	Operation / Measured Values / Synchronism
⟍	*Line Voltage*

Angle Bus	Operation / Measured Values / Synchronism
⟍	*Bus Angle (Reference)*

Angle Line	Operation / Measured Values / Synchronism
	Line Angle

9.15 ExP[1] ... ExP[4]

External Protection - Module

9.15.1 ExP[1] ... ExP[4]: Device Planning Parameters

Mode	Device planning / Projected Elements	
-	-, use Table	*S.3*
External Protection - Module, general operation mode		

Superv. only	Device planning / Definition	
no	no, yes Table	*S.3*
External Protection - Module, if set to “Yes”: Restriction of the function to a supervision functionality, i.e. there is no general alarm, no general trip and no trip command.		

9.15.2 ExP[1] ... ExP[4]: Global Parameters

ExBlo1 **ExBlo2**	Protection Para / Global Prot Para / ExP / ExP[1]	
-	- ... Internal test state Table	*P.2*
External blocking of the module, if blocking is activated (allowed) within a parameter set and if the state of the assigned signal is true.		

ExBlo TripCmd	Protection Para / Global Prot Para / ExP / ExP[1]	
• Only available if: Superv. only = no -	- ... Internal test state Table	*P.2*
External blocking of the Trip Command of the module/the stage, if blocking is activated (allowed) within a parameter set and if the state of the assigned signal is true.		

Alarm	Protection Para / Global Prot Para / ExP / ExP[1]	
-	- ... Internal test state Table	*P.2*
Assignment for External Alarm		

Trip	Protection Para / Global Prot Para / ExP / ExP[1]	
-	- ... Internal test state Table	*P.2*
External trip of the CB if the state of the assigned signal is true.		

9.15.3 ExP[1] ... ExP[4]: Setting Group Parameters

Function	Protection Para / Set 1 / ExP / ExP[1] Protection Para / Set 2 / ExP / ExP[1] Protection Para / Set 3 / ExP / ExP[1] Protection Para / Set 4 / ExP / ExP[1]	
Inactive	Inactive, Active Table	*P.2*
Permanent activation or deactivation of module/stage.		

ExBlo Fc	Protection Para / Set 1 / ExP / ExP[1] Protection Para / Set 2 / ExP / ExP[1] Protection Para / Set 3 / ExP / ExP[1] Protection Para / Set 4 / ExP / ExP[1]	
Inactive	Inactive, Active Table	*P.2*
Activate (allow) or inactivate (disallow) blocking of the module/stage. This parameter is only effective if a signal is assigned to the corresponding global protection parameter. If the signal becomes true, those modules/stages are blocked that are parameterized "ExBlo Fc=active".		

Blo TripCmd	Protection Para / Set 1 / ExP / ExP[1] Protection Para / Set 2 / ExP / ExP[1] Protection Para / Set 3 / ExP / ExP[1] Protection Para / Set 4 / ExP / ExP[1]	
• Only available if: Superv. only = no Inactive	Inactive, Active Table	*P.2*
Permanent blocking of the Trip Command of the module/stage.		

ExBlo TripCmd Fc	Protection Para / Set 1 / ExP / ExP[1] Protection Para / Set 2 / ExP / ExP[1] Protection Para / Set 3 / ExP / ExP[1] Protection Para / Set 4 / ExP / ExP[1]	
• Only available if: Superv. only = no Inactive	Inactive, Active Table	*P.2*
Activate (allow) or inactivate (disallow) blocking of the module/stage. This parameter is only effective if a signal is assigned to the corresponding global protection parameter. If the signal becomes true, those modules/stages are blocked that are parameterized "ExBlo TripCmd Fc=active".		

9.15.4 ExP[1] ... ExP[4]: Input States

ExBlo1-I (↳ **ExP[1] . ExBlo1**)	Operation / Status Display / ExP / ExP[1]
⇩	*Module input state: External blocking1*

ExBlo2-I	Operation / Status Display / ExP / ExP[1]
⇩	*Module input state: External blocking2*

ExBlo TripCmd-I	Operation / Status Display / ExP / ExP[1]
⇩	• Only available if: Superv. only = no *Module input state: External Blocking of the Trip Command*

Alarm-I (↳ **ExP[1] . Alarm**)	Operation / Status Display / ExP / ExP[1]
⇩	*Module input state: Alarm*

Trip-I (↳ **ExP[1] . Trip**)	Operation / Status Display / ExP / ExP[1]
⇩	*Module input state: Trip*

9.15.5 ExP[1] ... ExP[4]: Signals (Output States)

Active	Operation / Status Display / All Actives Operation / Status Display / ExP / ExP[1]
⇧	*Signal: active*

ExBlo	Operation / Status Display / ExP / ExP[1]
⇧	*Signal: External Blocking*

Blo TripCmd	Operation / Status Display / ExP / ExP[1]
⇧	• Only available if: Superv. only = no *Signal: Trip Command blocked*

ExBlo TripCmd	Operation / Status Display / ExP / ExP[1]
⇧	• Only available if: Superv. only = no *Signal: External Blocking of the Trip Command*

Alarm	Operation / Status Display / Alarms Operation / Status Display / ExP / ExP[1]
⇧	*Signal: Alarm*

Trip	Operation / Status Display / Trips Operation / Status Display / ExP / ExP[1]
⇧	*Signal: Trip*

TripCmd	Operation / Status Display / TripCmds Operation / Status Display / ExP / ExP[1]
⇧	• Only available if: Superv. only = no *Signal: Trip Command*

9.16 CBF [62BF]

Circuit breaker failure protection module

9.16.1 CBF: Device Planning Parameters

Mode	Device planning / Projected Elements	
-	-, use Table	*S.3*
Module Circuit Breaker Failure protection, general operation mode		

9.16.2 CBF: Global Parameters

ExBlo1 **ExBlo2**	Protection Para / Global Prot Para / Supervision / CBF	
-	- . . . Internal test state Table	*P.2*
External blocking of the module, if blocking is activated (allowed) within a parameter set and if the state of the assigned signal is true.		

Trigger	Protection Para / Global Prot Para / Supervision / CBF	
All TripCmds	- . -, All TripCmds, External TripCmds Table	*P.2*
Determining the trigger mode for the Breaker Failure.		

Trigger1 **Trigger2** **,** **Trigger3**	Protection Para / Global Prot Para / Supervision / CBF	
-	- . . . LE80.Out inverted Table	*P.2*
Trigger that will start the CBF		

9.16.3 CBF: Setting Group Parameters

Function	Protection Para / Set 1 / Supervision / CBF Protection Para / Set 2 / Supervision / CBF Protection Para / Set 3 / Supervision / CBF Protection Para / Set 4 / Supervision / CBF	
Inactive	Inactive, Active Table	*P.2*
Permanent activation or deactivation of module/stage.		

ExBlo Fc	Protection Para / Set 1 / Supervision / CBF Protection Para / Set 2 / Supervision / CBF Protection Para / Set 3 / Supervision / CBF Protection Para / Set 4 / Supervision / CBF	
Inactive	Inactive, Active Table	*P.2*
Activate (allow) or inactivate (disallow) blocking of the module/stage. This parameter is only effective if a signal is assigned to the corresponding global protection parameter. If the signal becomes true, those modules/stages are blocked that are parameterized "ExBlo Fc=active".		

t-CBF	Protection Para / Set 1 / Supervision / CBF Protection Para / Set 2 / Supervision / CBF Protection Para / Set 3 / Supervision / CBF Protection Para / Set 4 / Supervision / CBF	
0.20s	0.00s ... 10.00s	*P.2*
If the delay time is expired, a CBF alarm is issued.		

9.16.4 CBF: Direct Controls

Res Lockout	Operation / Reset	
Inactive	Inactive, Active Table	*P.1*
Reset Lockout		

9.16.5 CBF: Input States

ExBlo1-I (**CBF . ExBlo1**)	Operation / Status Display / Supervision / CBF
Module input state: External blocking1	

ExBlo2-I	Operation / Status Display / Supervision / CBF
Module input state: External blocking2	

Trigger1-I **Trigger2-I** **,** **Trigger3-I** **(↳ CBF . Trigger1)**	Operation / Status Display / Supervision / CBF
⇩	*Module Input: Trigger that will start the CBF*

9.16.6 CBF: Signals (Output States)

Active	Operation / Status Display / All Actives Operation / Status Display / Supervision / CBF
⇧	*Signal: active*

ExBlo	Operation / Status Display / Supervision / CBF
⇧	*Signal: External Blocking*

Waiting for Trigger	Operation / Status Display / Supervision / CBF
⇧	*Waiting for Trigger*

running	Operation / Status Display / Supervision / CBF
⇧	*Signal: CBF-Module started*

Alarm	Operation / Status Display / Trips Operation / Status Display / Supervision / CBF
⇧	*Signal: Circuit Breaker Failure*

Lockout	Operation / Status Display / Supervision / CBF
⇧	*Signal: Lockout*

Res Lockout	Operation / Status Display / Supervision / CBF
⇧	*Signal: Reset Lockout*

9.17 Red.Ethernet

Redundant Ethernet

9.17.1 Red.Ethernet: Device Planning Parameters

Mode	Device planning / Projected Elements	
Switch	Switch, PRP, HSR Table	*S.3*
Redundant Ethernet, general operation mode		

9.17.2 Red.Ethernet: Global Parameters

Supervision PRP	Device Para / TCP/IP / Red.Ethernet	
Active	Inactive, Active Table	*S.3*
Supervision PRP		

superv.Int.PRP	Device Para / TCP/IP / Red.Ethernet	
• Only available if: Supervision PRP = Active 2	1 ... 60	*S.3*
Interval for supervision messages: PRP		

Supervision HSR	Device Para / TCP/IP / Red.Ethernet	
Active	Inactive, Active Table	*S.3*
Supervision HSR		

superv.Int.HSR	Device Para / TCP/IP / Red.Ethernet	
• Only available if: Supervision HSR = Active 2	1 ... 60	*S.3*
Interval for supervision messages: HSR		

9.17.3 Red.Ethernet: Direct Controls

Res Counter	Operation / Reset	
Inactive	Inactive, Active Table	*P.1*
Reset all Counters.		

9.17.4 Red.Ethernet: Signals (Output States)

Uplink A	Operation / Status Display / Red.Ethernet
Uplink A	

OpenRingA	Operation / Status Display / Red.Ethernet
Open HSR ring detected on port A. A	

Uplink B	Operation / Status Display / Red.Ethernet
Uplink B	

OpenRingB	Operation / Status Display / Red.Ethernet
Open HSR ring detected on port A. B	

9.17.5 Red.Ethernet: Values, Counters

DiagCounter1_	Operation / Count and RevData / Red.Ethernet
*Number of total requests (all slave addresses on bus)_*	

DiagCounter2_	Operation / Count and RevData / Red.Ethernet
*Number of requests for this slave address_*	

DiagCounter3_ **...** **DiagCounter8_**	Operation / Count and RevData / Red.Ethernet
*Number of total response messages_*	

CountSentFramesA	Operation / Count and RevData / Red.Ethernet
#	*Number of frames sent on port A.*

CountSentFramesB	Operation / Count and RevData / Red.Ethernet
#	*Number of frames sent on port B.*

CountResFramesA	Operation / Count and RevData / Red.Ethernet
#	*Number of frames received on port A.*

CountResFramesB	Operation / Count and RevData / Red.Ethernet
#	*Number of frames received on port B.*

CountErrorPA	Operation / Count and RevData / Red.Ethernet
#	*Number of errors on port A.*

CountErrorPB	Operation / Count and RevData / Red.Ethernet
#	*Number of errors on port B.*

CountMissDupl	Operation / Count and RevData / Red.Ethernet
#	*Number of missing duplicated frames.*

MaxDuplFrDelay	Operation / Count and RevData / Red.Ethernet
#	*Max delay time of a duplicated frames.*

CountTxMsg	Operation / Count and RevData / Red.Ethernet
#	*Total number of received frames.*

CountRxMsg	Operation / Count and RevData / Red.Ethernet
#	*Total number of sent frames.*

CountDuplMsg	Operation / Count and RevData / Red.Ethernet
#	*Total number of duplicate frames rejected in software.*

CountSigMapOverflow	Operation / Count and RevData / Red.Ethernet
#	*Total number of forced erase entries from Rx frame signature map.*

MaxSigMapEntries	Operation / Count and RevData / Red.Ethernet
#	*Maximum reached size of Rx frame signature map.*

CountSigMapEntries	Operation / Count and RevData / Red.Ethernet
#	*Current size of Rx frame signature map.*

Duplex mode A	Operation / Status Display / Red.Ethernet
⟍	*Duplex mode*

Speed A	Operation / Status Display / Red.Ethernet
⟍	*Speed*

Duplex mode B	Operation / Status Display / Red.Ethernet
⟍	*Duplex mode*

Speed B	Operation / Status Display / Red.Ethernet
⟍	*Speed*

9.18 PTP

PTP-Module

9.18.1 PTP: Device Planning Parameters

Mode	Device planning / Projected Elements	
-	-, Default E2E, Default P2P, IEEE C37.238, IEC 61850-9-3:2016 Table	*S.3*
PTP-Module, general operation mode		

9.18.2 PTP: Global Parameters

Net.Trans.Prot.	Device Para / Time / TimeSync / PTP	
UDP IPv4		*S.3*
PTP Network Transport Protocol (IEEE 802.3 or UDP IPv4)		

Domain	Device Para / Time / TimeSync / PTP	
0	0 ... 255	*S.3*
Domain number. Im Fall Power Profile IEEE C37.238 empfohlener Wert ist 254 und für IEC61850-9-3 ist 254.		

PathDelay Intv.	Device Para / Time / TimeSync / PTP	
1	1 ... 256 Table	*S.3*
PathDelay Intv.		

PeerPathDelay Intv.	Device Para / Time / TimeSync / PTP	
1	1 ... 256 Table	*S.3*
PeerPathDelay Intv.		

Vlan act.	Device Para / Time / TimeSync / PTP	
Inactive		*S.3*
Vlan activation		

Vlan ID	Device Para / Time / TimeSync / PTP	
• Only available if: Vlan act. = Active 1	1 ... 4094	*S.3*
Vlan ID		

Vlan prio	Device Para / Time / TimeSync / PTP	
• Only available if: Vlan act. = Active 4	0 ... 7	*S.3*
PTP VLAN priority.		

9.18.3 PTP: Direct Controls

Res Counter	Operation / Reset	
Inactive	Inactive, Active Table	*P.1*
Reset all Counters.		

9.18.4 PTP: Signals (Output States)

PTP active	Operation / Status Display / TimeSync / PTP
PTP active	

9.18.5 PTP: Values, Counters

Sync msg	Operation / Count and RevData / TimeSync / PTP
Sync message	

Sync followUp msg	Operation / Count and RevData / TimeSync / PTP
Sync follow up message	

Announce msg	Operation / Count and RevData / TimeSync / PTP
Announce message	

DelayReq Tx msg	Operation / Count and RevData / TimeSync / PTP
Delay request transmit message	

DelayResp Rx msg	Operation / Count and RevData / TimeSync / PTP
#	*Delay response receive message*

PDelayReq Tx msg	Operation / Count and RevData / TimeSync / PTP
#	*Peer delay request transmit message*

PDelayResp Rx msg	Operation / Count and RevData / TimeSync / PTP
#	*Peer delay response receive message*

PDelayRespFolUp Rx msg	Operation / Count and RevData / TimeSync / PTP
#	*Peer delay response follow up receive message*

PDelayReq Rx msg	Operation / Count and RevData / TimeSync / PTP
#	*Peer delay request receive message*

PDelayResp Tx msg	Operation / Count and RevData / TimeSync / PTP
#	*Peer delay response transmit message*

Unhandled Rx msg	Operation / Count and RevData / TimeSync / PTP
#	*Unhandled receive message*

Master ID	Operation / Status Display / TimeSync / PTP
⟍	*Grandmaster Clock ID*

Sync Status	Operation / Status Display / TimeSync / PTP
⟍	*Synchronization Status*

Delay mech.	Operation / Status Display / TimeSync / PTP
⟍	*Path delay mechanism*

Path delay time	Operation / Status Display / TimeSync / PTP
⟍	*Path delay time*

PathDelay PortA	Operation / Status Display / TimeSync / PTP
	Path delay time PortA

PathDelay PortB	Operation / Status Display / TimeSync / PTP
	PathDelay PortB

Offs.	Operation / Status Display / TimeSync / PTP
	Offset

Drift	Operation / Status Display / TimeSync / PTP
	Drift

9.19 Supervision

9.19.1 TCS [74TC]

Trip Circuit Supervision

9.19.1.1 TCS: Device Planning Parameters

Mode	Device planning / Projected Elements	
-	-, use Table	*S.3*
Trip Circuit Supervision, general operation mode		

9.19.1.2 TCS: Global Parameters

Mode	Protection Para / Global Prot Para / Supervision / TCS	
Closed	Closed, Either Table	*P.2*
Select if trip circuit is going to be monitored when the breaker is closed or when the breaker is either open or close.		

Input 1	Protection Para / Global Prot Para / Supervision / TCS	
-	- . . . DI 8 Table	*P.2*
Select the input configured to monitor the trip coil when the breaker is closed.		

Input 2	Protection Para / Global Prot Para / Supervision / TCS	
• Only available if: Mode = Either -	- . . . DI 8 Table	*P.2*
Select the input configured to monitor the trip coil when the breaker is open. Only available if Mode set to “Either”.		

ExBlo1 **ExBlo2**	Protection Para / Global Prot Para / Supervision / TCS	
-	- . . . Internal test state Table	*P.2*
External blocking of the module, if blocking is activated (allowed) within a parameter set and if the state of the assigned signal is true.		

9.19.1.3 TCS: Setting Group Parameters

Function	Protection Para / Set 1 / Supervision / TCS Protection Para / Set 2 / Supervision / TCS Protection Para / Set 3 / Supervision / TCS Protection Para / Set 4 / Supervision / TCS	
Inactive	Inactive, Active Table	*P.2*
Permanent activation or deactivation of module/stage.		

ExBlo Fc	Protection Para / Set 1 / Supervision / TCS Protection Para / Set 2 / Supervision / TCS Protection Para / Set 3 / Supervision / TCS Protection Para / Set 4 / Supervision / TCS	
Inactive	Inactive, Active Table	*P.2*
Activate (allow) or inactivate (disallow) blocking of the module/stage. This parameter is only effective if a signal is assigned to the corresponding global protection parameter. If the signal becomes true, those modules/stages are blocked that are parameterized "ExBlo Fc=active".		

t-TCS	Protection Para / Set 1 / Supervision / TCS Protection Para / Set 2 / Supervision / TCS Protection Para / Set 3 / Supervision / TCS Protection Para / Set 4 / Supervision / TCS	
0.2s	0.10s ... 10.00s	*P.2*
Delay time of the Trip Circuit Supervision		

9.19.1.4 TCS: Input States

Aux ON-I **(TCS . Input 1)**	Operation / Status Display / Supervision / TCS
Module Input State: Position indicator/check-back signal of the CB (52a)	

Aux OFF-I	Operation / Status Display / Supervision / TCS
Module input state: Position indicator/check-back signal of the CB (52b)	

ExBlo1-I **(TCS . ExBlo1)**	Operation / Status Display / Supervision / TCS
Module input state: External blocking1	

ExBlo2-I	Operation / Status Display / Supervision / TCS
⇩	*Module input state: External blocking2*

9.19.1.5 TCS: Signals (Output States)

Active	Operation / Status Display / All Actives Operation / Status Display / Supervision / TCS
⇧	*Signal: active*

ExBlo	Operation / Status Display / Supervision / TCS
⇧	*Signal: External Blocking*

Alarm	Operation / Status Display / Alarms Operation / Status Display / Supervision / TCS
⇧	*Signal: Alarm Trip Circuit Supervision*

Not Possible	Operation / Status Display / Supervision / TCS
⇧	*Not possible because no state indicator assigned to the breaker.*

9.19.2 VTS

Voltage transformer supervision

9.19.2.1 VTS: Device Planning Parameters

Mode	Device planning / Projected Elements	
-	-, use Table	*S.3*
Voltage transformer supervision, general operation mode		

9.19.2.2 VTS: Global Parameters

ExBlo1 **ExBlo2**	Protection Para / Global Prot Para / Supervision / VTS	
-	- . . . Internal test state Table	*P.2*
External blocking of the module, if blocking is activated (allowed) within a parameter set and if the state of the assigned signal is true.		

Ex FF VT-I	Protection Para / Global Prot Para / Supervision / VTS	
-	- . . . Internal test state Table	*P.2*
State of the module input: Alarm Fuse Failure Voltage Transformers		

Ex FF EVT-I	Protection Para / Global Prot Para / Supervision / VTS	
-	- . . . Internal test state Table	*P.2*
State of the module input: Alarm Fuse Failure Earth Voltage Transformers		

9.19.2.3 VTS: Setting Group Parameters

Function	Protection Para / Set 1 / Supervision / VTS Protection Para / Set 2 / Supervision / VTS Protection Para / Set 3 / Supervision / VTS Protection Para / Set 4 / Supervision / VTS	
Inactive	Inactive, Active Table	*P.2*
Permanent activation or deactivation of module/stage.		

ExBlo Fc	Protection Para / Set 1 / Supervision / VTS Protection Para / Set 2 / Supervision / VTS Protection Para / Set 3 / Supervision / VTS Protection Para / Set 4 / Supervision / VTS	
Inactive	Inactive, Active Table	*P.2*

Activate (allow) or inactivate (disallow) blocking of the module/stage. This parameter is only effective if a signal is assigned to the corresponding global protection parameter. If the signal becomes true, those modules/stages are blocked that are parameterized "ExBlo Fc=active".

ΔV	Protection Para / Set 1 / Supervision / VTS Protection Para / Set 2 / Supervision / VTS Protection Para / Set 3 / Supervision / VTS Protection Para / Set 4 / Supervision / VTS	
0.50Vn	0.20Vn ... 1.00Vn	*P.2*

In order to prevent faulty tripping of phase selective protection functions that use the voltage as tripping criterion. If the difference of the residual voltage and the calculated value V0 is higher than the pick up value ΔV, an alarm event effected after the excitation time. In such a case, the existence of a fuse failure, a broken wire or a faulty measuring circuit can be assumed.

Alarm delay	Protection Para / Set 1 / Supervision / VTS Protection Para / Set 2 / Supervision / VTS Protection Para / Set 3 / Supervision / VTS Protection Para / Set 4 / Supervision / VTS	
1.0s	0.0s ... 9999.0s	*P.2*

Alarm delay

9.19.2.4 VTS: Input States

Ex Fuse Fail VT-I **(VTS . Ex FF VT-I)**	Operation / Status Display / Supervision / VTS

Module input state: External fuse failure voltage transformers

Ex Fuse Fail EVT-I **(VTS . Ex FF EVT-I)**	Operation / Status Display / Supervision / VTS

Module input state: External fuse failure earth voltage transformer

ExBlo1-I **(VTS . ExBlo1)**	Operation / Status Display / Supervision / VTS

Module input state: External blocking1

ExBlo2-I	Operation / Status Display / Supervision / VTS
⇩	*Module input state: External blocking2*

9.19.2.5 VTS: Signals (Output States)

Active	Operation / Status Display / All Actives Operation / Status Display / Supervision / VTS
⇧	*Signal: active*

ExBlo	Operation / Status Display / Supervision / VTS
⇧	*Signal: External Blocking*

Alarm ΔV	Operation / Status Display / Supervision / VTS
⇧	*Signal: Alarm ΔV Voltage Transformer Measuring Circuit Supervision*

Alarm	Operation / Status Display / Alarms Operation / Status Display / Supervision / VTS
⇧	*Signal: Alarm Voltage Transformer Measuring Circuit Supervision*

Ex FF VT	Operation / Status Display / Supervision / VTS
⇧	*Signal: Ex FF VT*

Ex FF EVT	Operation / Status Display / Supervision / VTS
⇧	*Signal: Alarm Fuse Failure Earth Voltage Transformers*

10 Control

Control

Control Page	
	Control Page This item represents a special dialog. (See the Technical Manual for details.)

10.1 Ctrl: Global Parameters

Res NonIL	Control / General Settings	
single Operation	single Operation, timeout, permanent Table	*C.2*
	Resetmode Non-Interlocking	

Timeout NonIL	Control / General Settings	
• Only available if: Res NonIL ≠ permanent 60s	2s ... 3600s	*C.2*
	Timeout Non-Interlocking	

NonIL Assign	Control / General Settings	
-	- ... Internal test state Table	*C.2*
	Assignment Non-Interlocking	

10.2 Ctrl: Direct Controls

Switching Authority	Control / General Settings	
Local	None, Local, Remote, Local and Remote Table	*C.2*
	Switching Authority	

NonInterl	Control / General Settings	
Inactive	Inactive, Active Table	*C.2*
	DC for Non-Interlocking	

Reset max values	Operation / Reset	
False	False, True Table	*C.1*
Direct Command to reset the maximum values of: switching comands per second, and percentage of rejected commands.		

10.3 Ctrl: Input States

NonInterl-I (Ctrl . NonIL Assign)	Operation / Status Display / Control / General Control
Non-Interlocking	

10.4 Ctrl: Signals (Output States)

Local	Operation / Status Display / Control / General Control
Switching Authority: Local	

Remote	Operation / Status Display / Control / General Control
Switching Authority: Remote	

NonInterl	Operation / Status Display / Control / General Control
Non-Interlocking is active	

SG Indeterm	Operation / Status Display / Control / General Control
(At least one) Switchgear is moving (Position cannot be determined).	

SG Disturb	Operation / Status Display / Control / General Control
(At least one) Switchgear is disturbed.	

CES SAuthority	Operation / Status Display / Control / General Control
Command Execution Supervision: Number of rejected Commands because of missing switching authority.	

CES DoubleOperating	Operation / Status Display / Control / General Control
Command Execution Supervision: Number of rejected Commands because a second switch command is in conflict with a pending one.	

10.5 Ctrl: Values

Switching Authority	Operation / Security / Security States
	Switching Authority

Switch.Cmds per s	Operation / Count and RevData / Control / Ctrl
	The number of switching commands per second. (This is mainly an internal diagnosis value.)

Rej. Switch.Cmds	Operation / Count and RevData / Control / Ctrl
	The percentage of rejected switching commands per second. (This is mainly an internal diagnosis value.)

Switch.Cmds max	Operation / Count and RevData / Control / Ctrl
	The maximum number of switching commands per second. (This is mainly an internal diagnosis value.)

Rej.Swtch.Cmds max	Operation / Count and RevData / Control / Ctrl
	The maximum percentage of rejected switching commands per second. (This is mainly an internal diagnosis value.)

10.6 SG[1]

Switchgear

10.6.1 SG[1]: Global Parameters

Aux ON	Control / SG / SG[1] / Pos Indicatrs Wirng	
DI 1	- ... LE80.Out inverted Table	*C.2*
The CB is in ON-position if the state of the assigned signal is true (52a).		

Aux OFF	Control / SG / SG[1] / Pos Indicatrs Wirng	
DI 2	- ... LE80.Out inverted Table	*C.2*
The CB is in OFF-position if the state of the assigned signal is true (52b).		

Ready	Control / SG / SG[1] / Pos Indicatrs Wirng	
Only available if: -	- ... LE80.Out inverted Table	*C.2*
Circuit breaker is ready for operation if the state of the assigned signal is true. This digital input can be used by some protective elements (if they are available within the device) like Auto Reclosure (AR), e.g. as a trigger signal.		

Removed	Control / SG / SG[1] / Pos Indicatrs Wirng	
Only available if: -	- ... LE80.Out inverted Table	*C.2*
The withdrawable circuit breaker is Removed		

Interl ON1 **Interl ON2** **,** **Interl ON3**	Control / SG / SG[1] / Interlockings	
Only available if: -	- ... Internal test state Table	*C.2*
Interlocking of the ON command		

Interl OFF1 **Interl OFF2** **,** **Interl OFF3**	Control / SG / SG[1] / Interlockings	
Only available if: -	- ... Internal test state Table	*C.2*
Interlocking of the OFF command		

SCmd ON	Control / SG / SG[1] / Ex ON/OFF Cmd	
Only available if: -	- ... LE80.Out inverted Table	*C.2*
Switching ON Command, e.g. the state of the Logics or the state of the digital input		

SCmd OFF	Control / SG / SG[1] / Ex ON/OFF Cmd	
Only available if: -	- ... LE80.Out inverted Table	*C.2*
Switching OFF Command, e.g. the state of the Logics or the state of the digital input		

t-TripCmd	Control / SG / SG[1] / Trip Manager	
Only available if: 0.2s	0s ... 300.00s	*P.2*
Minimum hold time of the OFF-command (circuit breaker, load break switch)		

Latched	Control / SG / SG[1] / Trip Manager	
Only available if: Inactive	Inactive, Active Table	*P.2*
Defines whether the Trip Command is latched.		

Ack TripCmd	Control / SG / SG[1] / Trip Manager	
Only available if: -	- ... Internal test state Table	*P.2*
Ack TripCmd		

Off Cmd1	Control / SG / SG[1] / Trip Manager	
Only available if: TripCmd	- ... TripCmd Table	*P.2*
Off Command to the Circuit Breaker if the state of the assigned signal becomes true.		

Off Cmd2	Control / SG / SG[1] / Trip Manager	
Only available if: TripCmd	- ... TripCmd Table	*P.2*
Off Command to the Circuit Breaker if the state of the assigned signal becomes true.		

Off Cmd3	Control / SG / SG[1] / Trip Manager	
Only available if: TripCmd	- ... TripCmd Table	*P.2*
Off Command to the Circuit Breaker if the state of the assigned signal becomes true.		

Off Cmd4	Control / SG / SG[1] / Trip Manager	
Only available if: TripCmd	- ... TripCmd Table	*P.2*
Off Command to the Circuit Breaker if the state of the assigned signal becomes true.		

Off Cmd5 **...** **Off Cmd30**	Control / SG / SG[1] / Trip Manager	
Only available if: -	- ... TripCmd Table	*P.2*
Off Command to the Circuit Breaker if the state of the assigned signal becomes true.		

Synchronism	Control / SG / SG[1] / Synchron Switchg	
-	- ... LE80.Out inverted Table	*C.2*
Synchronism		

t-MaxSyncSuperv	Control / SG / SG[1] / Synchron Switchg	
0.2s	0s ... 3000.00s	*C.2*
Synchron-Run timer: Max. time allowed for synchronizing process after a close initiate. Only used for GENERATOR2SYSTEM working mode.		

ON incl Prot ON	Control / SG / SG[1] / General Settings	
Active	Inactive, Active Table	*C.2*
The ON Command includes the ON Command issued by the Protection module.		

OFF incl TripCmd	Control / SG / SG[1] / General Settings	
Active	Inactive, Active Table	*C.2*
The OFF Command includes the OFF Command issued by the Protection module.		

t-Move ON	Control / SG / SG[1] / General Settings	
0.1s	0.01s ... 100.00s	*C.2*
Time to move to the ON Position		

t-Move OFF	Control / SG / SG[1] / General Settings	
0.1s	0.01s ... 100.00s	*C.2*
Time to move to the OFF Position		

t-Dwell	Control / SG / SG[1] / General Settings	
Only available if: 0s	0s ... 100.00s	*C.2*
Dwell time		

10.6.2 SG[1]: Direct Controls

Manipulate Position	Control / SG / SG[1] / General Settings	
Inactive	Inactive, Pos OFF, Pos ON Table	*C.2*
WARNING! Fake Position - Manual Position Manipulation		

Res SGwear Sl SG	Operation / Reset	
Inactive	Inactive, Active Table	*P.1*
Resetting the slow Switchgear Alarm		

Ack TripCmd	Operation / Acknowledge	
Only available if: Inactive	Inactive, Active Table	*P.1*
Acknowledge Trip Command		

Force Trip Cmd	Service / Test - Prot inhib. / Force SG	
Only available if: Inactive	Inactive, Active Table	*P.1*
Direct Command to force the device to issue a trip command (for testing purposes).		

10.6.3 SG[1]: Input States

Aux ON-I **(SG[1] . Aux ON)**	Operation / Status Display / Control / SG[1]
Module Input State: Position indicator/check-back signal of the CB (52a)	

Aux OFF-I **(SG[1] . Aux OFF)**	Operation / Status Display / Control / SG[1]
Module input state: Position indicator/check-back signal of the CB (52b)	

Ready-I	Operation / Status Display / Control / SG[1]
Only available if: *Module input state: CB ready*	

Sys-in-Sync-I	Operation / Status Display / Control / SG[1]
State of the module input: This signals has to become true within the synchronization time. If not, switching is unsuccessful.	

Removed-I	Operation / Status Display / Control / SG[1]
Only available if: *State of the module input: The withdrawable circuit breaker is Removed*	

Ack TripCmd-I	Operation / Status Display / Control / SG[1]
Only available if: *State of the module input: Acknowledgement Signal (for the Trip Command) Module input signal*	

Interl ON1-I **Interl ON2-I** **,** **Interl ON3-I**	Operation / Status Display / Control / SG[1]
⇩	Only available if: *State of the module input: Interlocking of the ON command*

Interl OFF1-I **Interl OFF2-I** **,** **Interl OFF3-I**	Operation / Status Display / Control / SG[1]
⇩	Only available if: *State of the module input: Interlocking of the OFF command*

SCmd ON-I	Operation / Status Display / Control / SG[1]
⇩	Only available if: *State of the module input: Switching ON Command, e.g. the state of the Logics or the state of the digital input*

SCmd OFF-I	Operation / Status Display / Control / SG[1]
⇩	Only available if: *State of the module input: Switching OFF Command, e.g. the state of the Logics or the state of the digital input*

10.6.4 SG[1]: Signals (Output States)

SI SingleContactInd	Operation / Status Display / Control / SG[1]
⇧	*Signal: The Position of the Switchgear is detected by one auxiliary contact (pole) only. Thus indeterminate and disturbed Positions cannot be detected.*

Pos not ON	Operation / Status Display / Control / SG[1]
⇧	*Signal: Pos not ON*

Pos ON	Operation / Status Display / Control / SG[1]
⇧	*Signal: Circuit Breaker is in ON-Position*

Pos OFF	Operation / Status Display / Control / SG[1]
⇧	*Signal: Circuit Breaker is in OFF-Position*

Pos Indeterm	Operation / Status Display / Control / SG[1]
⇧	*Signal: Circuit Breaker is in Indeterminate Position*

Pos Disturb	Operation / Status Display / Control / SG[1]
⇧	*Signal: Circuit Breaker Disturbed - Undefined Breaker Position. The Position Indicators contradict themselves. After expiring of a supervision timer this signal becomes true.*

Pos	Operation / Status Display / Control / SG[1]
⇧	*Signal: Circuit Breaker Position (0 = Indeterminate, 1 = OFF, 2 = ON, 3 = Disturbed)*

Ready	Operation / Status Display / Control / SG[1]
⇧	Only available if: *Signal: Circuit breaker is ready for operation.*

t-Dwell	Operation / Status Display / Control / SG[1]
⇧	Only available if: *Signal: Dwell time*

Removed	Operation / Status Display / Control / SG[1]
⇧	Only available if: *Signal: The withdrawable circuit breaker is Removed*

Interl ON	Operation / Status Display / Control / SG[1]
⇧	Only available if: *Signal: One or more IL_On inputs are active.*

Interl OFF	Operation / Status Display / Control / SG[1]
⇧	Only available if: *Signal: One or more IL_Off inputs are active.*

CES succesf	Operation / Status Display / Control / SG[1]
⇧	Only available if: *Signal: Command Execution Supervision: Switching command executed successfully.*

CES Disturbed	Operation / Status Display / Control / SG[1]
⇧	Only available if: *Signal: Command Execution Supervision: Switching Command unsuccessful. Switchgear in disturbed position.*

CES Fail TripCmd	Operation / Status Display / Control / SG[1]
⇧	*Signal: Command Execution Supervision: Command execution failed because trip command is pending.*

CES SwitchDir	Operation / Status Display / Control / SG[1]
⇧	Only available if: *Signal: Command Execution Supervision respectively Switching Direction Control: This signal becomes true, if a switch command is issued even though the switchgear is already in the requested position. Example: A switchgear that is already OFF should be switched OFF again (doubly). The same applies to CLOSE commands.*

CES ON d OFF	Operation / Status Display / Control / SG[1]
⇧	Only available if: *Signal: Command Execution Supervision: On Command during a pending OFF Command.*

CES SG not ready	Operation / Status Display / Control / SG[1]
⇧	*Signal: Command Execution Supervision: Switchgear not ready*

CES Fiel Interl	Operation / Status Display / Control / SG[1]
⇧	Only available if: *Signal: Command Execution Supervision: Switching Command not executed because of field interlocking.*

CES SyncTimeout	Operation / Status Display / Control / SG[1]
⇧	*Signal: Command Execution Supervision: Switching Command not executed. No Synchronization signal while t-sync was running.*

CES SG removed	Operation / Status Display / Control / SG[1]
⇧	*Signal: Command Execution Supervision: Switching Command unsuccessful, Switchgear removed.*

Prot ON	Operation / Status Display / Control / SG[1]
⇧	*Signal: ON Command issued by the Prot module*

TripCmd	Operation / Status Display / TripCmds Operation / Status Display / Control / SG[1]
⇧	Only available if: *Signal: Trip Command*

Ack TripCmd	Operation / Status Display / Control / SG[1]
⇧	Only available if: *Signal: Acknowledge Trip Command*

ON incl Prot ON	Operation / Status Display / Control / SG[1]
⇧	*Signal: The ON Command includes the ON Command issued by the Protection module.*

OFF incl TripCmd	Operation / Status Display / Control / SG[1]
⇧	*Signal: The OFF Command includes the OFF Command issued by the Protection module.*

Position Ind manipul	Operation / Status Display / Control / SG[1]
⇧	*Signal: Position Indicators faked*

SGwear Slow SG	Operation / Status Display / Control / SG[1]
⇧	*Signal: Alarm, the circuit breaker (load-break switch) becomes slower*

Res SGwear Sl SG	Operation / Status Display / Control / SG[1]
⇧	*Signal: Resetting the slow Switchgear Alarm*

ON Cmd	Operation / Status Display / Control / SG[1]
⇧	Only available if: *Signal: ON Command issued to the switchgear. Depending on the setting the signal may include the ON command of the Prot module.*

OFF Cmd	Operation / Status Display / Control / SG[1]
⇧	Only available if: *Signal: OFF Command issued to the switchgear. Depending on the setting the signal may include the OFF command of the Prot module.*

ON Cmd manual	Operation / Status Display / Control / SG[1]
⇧	*Signal: ON Cmd manual*

OFF Cmd manual	Operation / Status Display / Control / SG[1]
⇧	*Signal: OFF Cmd manual*

Sync ON request	Operation / Status Display / Control / SG[1]
⇪	*Signal: Synchronous ON request*

Test Trip Cmd	Operation / Status Display / Control / SG[1]
⇪	Only available if: *A trip command has been triggered manually (for testing purposes).*

10.6.5 SG[1]

Switchgear

10.6.5.1 SG[1]: Global Parameters

Operations Alarm	Control / SG / SG[1] / SG Wear	
9999	1 . . . 100000	*C.2*
Maximum number of operations. If the operations counter »TripCmd Cr« exceeds this limit then the signal »Operations Alarm« is set.		

10.6.5.2 SG[1]: Direct Controls

Res TripCmd Cr	Operation / Reset	
Inactive	Inactive, Active Table	*P.1*
Resetting of the Counter: Total number of trips of the switchgear		

10.6.5.3 SG[1]: Signals (Output States)

Operations Alarm	Operation / Status Display / Control / SG[1]
Signal: Too many Operations. (The operations counter »TripCmd Cr« has exceeded the limit set at »Operations Alarm«.)	

Res TripCmd Cr	Operation / Status Display / Control / SG[1]
Signal: Resetting of the Counter: Total number of trips of the switchgear	

10.6.5.4 SG[1]: Counters

TripCmd Cr	Operation / Count and RevData / Control / SG[1]
Counter: Total number of trips of the switchgear.	

11 System Alarms

System Alarms

11.1 SysA: Device Planning Parameters

Mode	Device planning / Projected Elements	
-	-, use Table	*S.3*
general operation mode		

11.2 SysA: Global Parameters

Function	SysA / General Settings	
Inactive	Inactive, Active Table	*P.2*
Permanent activation or deactivation of module/stage.		

ExBlo Fc	SysA / General Settings	
-	- ... Internal test state Table	*P.2*
Activate (allow) or inactivate (disallow) blocking of the module/stage. This parameter is only effective if a signal is assigned to the corresponding global protection parameter. If the signal becomes true, those modules/stages are blocked that are parameterized "ExBlo Fc=active".		

Alarm	SysA / THD / V THD	
Inactive	Inactive, Active Table	*P.2*
Alarm		

Threshold	SysA / THD / V THD	
10000V	1V ... 500000V	*P.2*
Threshold (to be entered as primary value)		

t-Delay	SysA / THD / V THD	
0s	0s ... 3600s	*P.2*
Tripping Delay		

11.3 SysA: Input States

ExBlo-I **(SysA . ExBlo Fc)**	Operation / Status Display / SysA
Module input state: External blocking	

11.4 SysA: Signals (Output States)

Active	Operation / Status Display / All Actives Operation / Status Display / SysA
Signal: active	

ExBlo	Operation / Status Display / SysA
Signal: External Blocking	

Alarm V THD	Operation / Status Display / SysA
Signal: Alarm Total Harmonic Distortion Voltage	

Trip V THD	Operation / Status Display / SysA
Signal: Trip Total Harmonic Distortion Voltage	

12 Recorders

12.1 Event rec

The event recorder logs all events like switching operations, change of parameters, alarms, trips, operating mode selections, blockings and state transitions of inputs and outputs.

Event rec	
	The event recorder logs all events like switching operations, change of parameters, alarms, trips, operating mode selections, blockings and state transitions of inputs and outputs. This item represents a special dialog. (See the Technical Manual for details.)

12.1.1 Event rec: Direct Controls

Res all rec	Operation / Reset	
Inactive	Inactive, Active Table	*P.1*
	Reset all records	

12.1.2 Event rec: Signals (Output States)

Res all records	Operation / Status Display / Recorders / Event rec
	Signal: All records are being deleted. (Remark: Immediately afterwards, this signal becomes inactive again.)

12.2 Disturb rec

After a trigger event has become true, the disturbance recorder writes analogue and digital tracks

Disturb rec	
	After a trigger event has become true, the disturbance recorder writes analogue and digital tracks This item represents a special dialog. (See the Technical Manual for details.)

12.2.1 Disturb rec: Global Parameters

Start: 1	Device Para / Recorders / Disturb rec	
Trip	- . . . Internal test state Table	*S.3*
	Start recording if the assigned signal is true.	

Start: 2 **. . .** **Start: 8**	Device Para / Recorders / Disturb rec	
-	- . . . Internal test state Table	*S.3*
	Start recording if the assigned signal is true.	

Auto overwriting	Device Para / Recorders / Disturb rec	
Active	Inactive, Active Table	*S.3*
	If there is no more free memory capacity left, the oldest file will be overwritten.	

Pre-trigger time	Device Para / Recorders / Disturb rec	
20%	0% . . . 99%	*S.3*
	The pre trigger time is set in percent of the »Max file size« value. It corresponds to the part of recording before the onset of the trigger event.	

Post-trigger time	Device Para / Recorders / Disturb rec	
20%	0% . . . 99%	*S.3*
	The post trigger time is set in percent of the »Max file size« value. It is the remaining time of the »Max file size«, depending on the »Pre-trigger time« setting and the duration of the trigger event, but at maximum the »Post-trigger time« set here.	

Max file size	Device Para / Recorders / Disturb rec	
2s	0.1s ... 15.0s	*S.3*
The maximum storage capacity per record, including pre-trigger and post-trigger time. The amount of records depends on the size of each record, on the max. file size (set here), and on the total storage capacity.		

12.2.2 Disturb rec: Direct Controls

Man Trigger	Operation / Recorders / Man Trigger	
False	False, True Table	*P.1*
Manual Trigger		

Res all rec	Operation / Reset	
Inactive	Inactive, Active Table	*P.1*
Reset all records		

12.2.3 Disturb rec: Input States

Start1-I ... **Start8-I** (Disturb rec . Start: 1)	Operation / Status Display / Recorders / Disturb rec
State of the module input:: Trigger event / start recording	

12.2.4 Disturb rec: Signals (Output States)

recording	Operation / Status Display / Recorders / Disturb rec
Signal: Recording	

memory full	Operation / Status Display / Recorders / Disturb rec
Signal: Memory full	

Clear fail	Operation / Status Display / Recorders / Disturb rec
Signal: Clear failure in memory	

Res all records	Operation / Status Display / Recorders / Disturb rec
⇧	*Signal: All records are being deleted. (Remark: Immediately afterwards, this signal becomes inactive again.)*

Res record	Operation / Status Display / Recorders / Disturb rec
⇧	*Signal: Delete record*

Man Trigger	Operation / Status Display / Recorders / Disturb rec
⇧	*Signal: Manual Trigger*

12.2.5 Disturb rec: Values

Rec state	Operation / Status Display / Recorders / Disturb rec
⟍	*Recording state*

Error code	Operation / Status Display / Recorders / Disturb rec
⟍	*Error code*

12.3 Fault rec

The values measured at the time of tripping are saved by the Fault Recorder.

Fault rec	
	The values measured at the time of tripping are saved by the Fault Recorder. This item represents a special dialog. (See the Technical Manual for details.)

12.3.1 Fault rec: Global Parameters

Record-Mode	Device Para / Recorders / Fault rec	
Trips only	Alarms and Trips, Trips only Table	*S.3*
	Recorder Mode (Set the behaviour of the recorder)	

t-meas-delay	Device Para / Recorders / Fault rec	
0ms	0ms ... 60ms	*S.3*
	After the Trip, the measurement will be delayed for this time.	

12.3.2 Fault rec: Direct Controls

Res all rec	Operation / Reset	
Inactive	Inactive, Active Table	*P.1*
	Reset all records	

12.3.3 Fault rec: Signals (Output States)

Res record	Operation / Status Display / Recorders / Fault rec
	Signal: Delete record

12.4 Trend rec

Trend Recorder

Trend rec	
	Trend Recorder This item represents a special dialog. (See the Technical Manual for details.)

12.4.1 Trend rec: Global Parameters

Resolution	Device Para / Recorders / Trend rec	
15 min	60 min, 30 min, 15 min, 10 min, 5 min, 1 min Table	*S.3*
	Resolution (recording frequency)	

Trend1	Device Para / Recorders / Trend rec	
VL1 RMS	- . . . VL31 THD Table	*S.3*
	Observed Value1	

Trend2	Device Para / Recorders / Trend rec	
VL2 RMS	- . . . VL31 THD Table	*S.3*
	Observed Value2	

Trend3	Device Para / Recorders / Trend rec	
VL3 RMS	- . . . VL31 THD Table	*S.3*
	Observed Value3	

Trend4	Device Para / Recorders / Trend rec	
VX meas RMS	- . . . VL31 THD Table	*S.3*
	Observed Value4	

Trend5	Device Para / Recorders / Trend rec	
VL12 RMS	- . . . VL31 THD Table	*S.3*
Observed Value5		

Trend6	Device Para / Recorders / Trend rec	
VL23 RMS	- . . . VL31 THD Table	*S.3*
Observed Value6		

Trend7	Device Para / Recorders / Trend rec	
VL31 RMS	- . . . VL31 THD Table	*S.3*
Observed Value7		

Trend8	Device Para / Recorders / Trend rec	
f	- . . . VL31 THD Table	*S.3*
Observed Value8		

Trend9	Device Para / Recorders / Trend rec	
V1	- . . . VL31 THD Table	*S.3*
Observed Value9		

Trend10	Device Para / Recorders / Trend rec	
V2	- . . . VL31 THD Table	*S.3*
Observed Value10		

12.4.2 Trend rec: Direct Controls

Res all rec	Operation / Reset	
Inactive	Inactive, Active Table	*P.1*
Reset all records		

12.4.3 Trend rec: Signals (Output States)

Res all records	Operation / Status Display / Recorders / Trend rec
Signal: All records are being deleted. (Remark: Immediately afterwards, this signal becomes inactive again.)	

12.4.4 Trend rec: Counters

Max avail Entries	Operation / Count and RevData / Trend rec
Maximum available entries in the current configuration	

13 Logic

13.1 Logics

Logic

13.1.1 Logics: Device Planning Parameters

No of Equations:	Device planning / Projected Elements	
20	0, 5, 10, 20, 40, 80 Table	*S.3*
Number of required Logic Equations:		

13.1.2 Logics . . . Logics

Logic

13.1.2.1 Logics . . . Logics: Global Parameters

LE1.Gate	Logics / LE 1	
AND	AND, OR, NAND, NOR Table	*S.3*
Logic gate		

LE1.Input1 . . . **LE1.Input4**	Logics / LE 1	
-	- . . . Internal test state Table	*S.3*
Assignment of the Input Signal		

LE1.Inverting1 . . . **LE1.Inverting4**	Logics / LE 1	
Inactive	Inactive, Active Table	*S.3*
Inverting the input signals.		

LE1.t-On Delay	Logics / LE 1	
0.00s	0.00s . . . 36000.00s	*S.3*
Switch On Delay		

LE1.t-Off Delay	Logics / LE 1	
0.00s	0.00s . . . 36000.00s	*S.3*
Switch Off Delay		

LE1.Reset Latched	Logics / LE 1	
-	- . . . Internal test state Table	*S.3*
Reset Signal for the Latching		

LE1.Inverting Reset	Logics / LE 1	
Inactive	Inactive, Active Table	*S.3*
Inverting Reset Signal for the Latching		

LE1.Inverting Set	Logics / LE 1	
Inactive	Inactive, Active Table	*S.3*
Inverting the Setting Signal for the Latching		

13.1.2.2 Logics . . . Logics: Input States

LE1.Gate In1-I **. . .** **LE1.Gate In4-I** **(Logics . LE1.Input1)**	Operation / Status Display / Logics
State of the module input: Assignment of the Input Signal	

LE1.Reset Latch-I **(Logics . LE1.Reset Latched)**	Operation / Status Display / Logics
State of the module input: Reset Signal for the Latching	

13.1.2.3 Logics . . . Logics: Signals (Output States)

LE1.Gate Out	Operation / Status Display / Logics
Signal: Output of the logic gate	

LE1.Timer Out	Operation / Status Display / Logics
Signal: Timer Output	

LE1.Out	Operation / Status Display / Logics
Signal: Latched Output (Q)	

LE1.Out inverted	Operation / Status Display / Logics
⇫	*Signal: Negated Latched Output (Q NOT)*

14 SelfSupervision

SelfSupervision

14.1 SSV: Direct Controls

Ack System LED	Operation / Acknowledge	
False	False, True Table	*P.1*
Acknowledge System LED (red/green flashing LED)		

Force SC	Service / Test - Prot inhib. / Force SC	
Inactive	Inactive, Active Table	*P.1*
Direct Command to force the device to drop SelfSuperVision Contact (SC) for 5 seconds (for testing purposes).		

14.2 SSV: Signals (Output States)

System Error	Operation / Self-Supervision / System State
Signal: Device Failure	

SelfSuperVision Contact	Operation / Self-Supervision / System State
Signal: SelfSuperVision Contact	

New error	Operation / Self-Supervision / System State
Signal: A new error message has been issued.	

New warning	Operation / Self-Supervision / System State
Signal: A new warning message has been issued.	

Test SC	Operation / Self-Supervision / System State
A drop of SelfSuperVision Contact (SC) has been triggered manually (for testing purposes).	

14.3 SSV: Counters

Cr No of free sockets	Operation / Self-Supervision / System State
Counter for network diagnosis. Number of free sockets.	

15 Service

15.1 Sgen

Sine wave generator

15.1.1 Sgen: Device Planning Parameters

Mode	Device planning / Projected Elements	
use	-, use Table	*S.3*
Sine wave generator, general operation mode		

15.1.2 Sgen: Global Parameters

PreFault	Service / Test - Prot inhib. / Sgen / Configuration / Times	
0.0s	0.00s ... 300.00s	*S.3*
Pre Fault Duration		

FaultSimulation	Service / Test - Prot inhib. / Sgen / Configuration / Times	
0.0s	0.00s ... 10800.00s	*S.3*
Duration of Fault Simulation		

PostFault	Service / Test - Prot inhib. / Sgen / Configuration / Times	
0.0s	0.00s ... 300.00s	*S.3*
Post Fault Duration		

TripCmd Mode	Service / Test - Prot inhib. / Sgen / Process	
No TripCmd	No TripCmd, With TripCmd Table	*S.3*
Trip Command Mode: Select between two operating modes for the Fault Simulator: "cold simulation" (without tripping the circuit breaker), or "hot simulation" (i.e. the simulation is authorized to trip the circuit breaker)		

Ex Start Simulation	Service / Test - Prot inhib. / Sgen / Process	
-	- ... Internal test state Table	*S.3*
External Start of Fault Simulation (Using the test parameters)		

ExBlo1	Service / Test - Prot inhib. / Sgen / Process	
Pos ON	- . . . Internal test state Table	*S.3*
External blocking of the module, if blocking is activated (allowed) within a parameter set and if the state of the assigned signal is true.1		

ExBlo2	Service / Test - Prot inhib. / Sgen / Process	
-	- . . . Internal test state Table	*S.3*
External blocking of the module, if blocking is activated (allowed) within a parameter set and if the state of the assigned signal is true.2		

Ex ForcePost	Service / Test - Prot inhib. / Sgen / Process	
-	- . . . Internal test state Table	*S.3*
Force Post state. Abort simulation.		

15.1.3 Sgen: Direct Controls

Start Simulation	Service / Test - Prot inhib. / Sgen / Process	
Inactive	Inactive, Active Table	*S.3*
Start Fault Simulation (Using the test parameters)		

Stop Simulation	Service / Test - Prot inhib. / Sgen / Process	
Inactive	Inactive, Active Table	*S.3*
Stopp Fault Simulation (Using the test parameters)		

15.1.4 Sgen: Input States

Ex Start Simulation-I **(Sgen . Ex Start Simulation)**	Operation / Status Display / Sgen
State of the module input:External Start of Fault Simulation (Using the test parameters)	

ExBlo1-I **(Sgen . ExBlo1)**	Operation / Status Display / Sgen Service / Test - Prot inhib. / Sgen / State
Module input state: External blocking1	

ExBlo2-I **(Sgen . ExBlo2)**	Operation / Status Display / Sgen Service / Test - Prot inhib. / Sgen / State
Module input state: External blocking2	

Ex ForcePost-I **(Sgen . Ex ForcePost)**	Operation / Status Display / Sgen Service / Test - Prot inhib. / Sgen / State
State of the module input:Force Post state. Abort simulation.	

15.1.5 Sgen: Signals (Output States)

Manual Start	Operation / Status Display / Sgen
Fault Simulation has been started manually.	

Manual Stop	Operation / Status Display / Sgen
Fault Simulation has been stopped manually.	

Running	Operation / Status Display / Sgen Service / Test - Prot inhib. / Sgen / State
Signal: Measuring value simulation is running	

Started	Operation / Status Display / Sgen
Fault Simulation has been started	

Stopped	Operation / Status Display / Sgen
Fault Simulation has been stopped	

State	Operation / Status Display / Sgen
Signal: Wave generation states: 0=Off, 1=PreFault, 2=Fault, 3=PostFault, 4=InitReset	

15.1.6 Sgen: Values

State	Service / Test - Prot inhib. / Sgen / State
Wave generation states: 0=Off, 1=PreFault, 2=Fault, 3=PostFault, 4=InitReset	

15.1.7 Sgen

Sine wave generator

15.1.7.1 Sgen: Global Parameters

VL1	Service / Test - Prot inhib. / Sgen / Configuration / PreFault / VT	
0.57Vn		*S.3*
Voltage Fundamental Magnitude in Pre State: phase L1		

VL2	Service / Test - Prot inhib. / Sgen / Configuration / PreFault / VT	
0.57Vn		*S.3*
Voltage Fundamental Magnitude in Pre State: phase L2		

VL3	Service / Test - Prot inhib. / Sgen / Configuration / PreFault / VT	
0.57Vn		*S.3*
Voltage Fundamental Magnitude in Pre State: phase L3		

VX	Service / Test - Prot inhib. / Sgen / Configuration / PreFault / VT	
0.0Vn		*S.3*
Voltage Fundamental Magnitude in Pre State: VX		

phi VL1	Service / Test - Prot inhib. / Sgen / Configuration / PreFault / VT	
0°	-360° ... 360°	*S.3*
Start Position respectively Start Angle of the Voltage Phasor during Pre-Phase:phase L1		

phi VL2	Service / Test - Prot inhib. / Sgen / Configuration / PreFault / VT	
240°	-360° ... 360°	*S.3*
Start Position respectively Start Angle of the Voltage Phasor during Pre-Phase:phase L2		

phi VL3	Service / Test - Prot inhib. / Sgen / Configuration / PreFault / VT	
120°	-360° ... 360°	*S.3*
Start Position respectively Start Angle of the Voltage Phasor during Pre-Phase:phase L3		

phi VX meas	Service / Test - Prot inhib. / Sgen / Configuration / PreFault / VT	
0°	-360° ... 360°	*S.3*
Start Position respectively Start Angle of the Voltage Phasor during Pre-Phase: VX		

VL1	Service / Test - Prot inhib. / Sgen / Configuration / FaultSimulation / VT	
0.29Vn		*S.3*
Voltage Fundamental Magnitude in Fault State: phase L1		

VL2	Service / Test - Prot inhib. / Sgen / Configuration / FaultSimulation / VT	
0.29Vn		*S.3*
Voltage Fundamental Magnitude in Fault State: phase L2		

VL3	Service / Test - Prot inhib. / Sgen / Configuration / FaultSimulation / VT	
0.29Vn		*S.3*
Voltage Fundamental Magnitude in Fault State: phase L3		

VX	Service / Test - Prot inhib. / Sgen / Configuration / FaultSimulation / VT	
0.29Vn		*S.3*
Voltage Fundamental Magnitude in Fault State: phase VX		

phi VL1	Service / Test - Prot inhib. / Sgen / Configuration / FaultSimulation / VT	
0°	-360° ... 360°	*S.3*
Start Position respectively Start Angle of the Voltage Phasor during Fault-Phase:phase L1		

phi VL2	Service / Test - Prot inhib. / Sgen / Configuration / FaultSimulation / VT	
240°	-360° ... 360°	*S.3*
Start Position respectively Start Angle of the Voltage Phasor during Fault-Phase:phase L2		

phi VL3	Service / Test - Prot inhib. / Sgen / Configuration / FaultSimulation / VT	
120°	-360° ... 360°	*S.3*
Start Position respectively Start Angle of the Voltage Phasor during Fault-Phase:phase L3		

phi VX meas	Service / Test - Prot inhib. / Sgen / Configuration / FaultSimulation / VT	
0°	-360° ... 360°	*S.3*
Start Position respectively Start Angle of the Voltage Phasor during Fault-Phase: VX		

VL1	Service / Test - Prot inhib. / Sgen / Configuration / PostFault / VT	
0.57Vn		*S.3*
Voltage Fundamental Magnitude during Post phase: phase L1		

VL2	Service / Test - Prot inhib. / Sgen / Configuration / PostFault / VT	
0.57Vn		*S.3*
	Voltage Fundamental Magnitude during Post phase: phase L2	

VL3	Service / Test - Prot inhib. / Sgen / Configuration / PostFault / VT	
0.57Vn		*S.3*
	Voltage Fundamental Magnitude during Post phase: phase L3	

VX	Service / Test - Prot inhib. / Sgen / Configuration / PostFault / VT	
0.0Vn		*S.3*
	Voltage Fundamental Magnitude during Post phase: phase VX	

phi VL1	Service / Test - Prot inhib. / Sgen / Configuration / PostFault / VT	
0°	-360° ... 360°	*S.3*
	Start Position respectively Start Angle of the Voltage Phasor during Post phase: phase L1	

phi VL2	Service / Test - Prot inhib. / Sgen / Configuration / PostFault / VT	
240°	-360° ... 360°	*S.3*
	Start Position respectively Start Angle of the Voltage Phasor during Post phase: phase L2	

phi VL3	Service / Test - Prot inhib. / Sgen / Configuration / PostFault / VT	
120°	-360° ... 360°	*S.3*
	Start Position respectively Start Angle of the Voltage Phasor during Post phase: phase L3	

phi VX meas	Service / Test - Prot inhib. / Sgen / Configuration / PostFault / VT	
0°	-360° ... 360°	*S.3*
	Start Position respectively Start Angle of the Voltage Phasor during Post phase: phase VX	

16 Statistics

16.1 Statistics: Global Parameters

ResFc Max	Device Para / Statistics / Min / Max	
-	- . . . Internal test state Table	*S.3*
Resetting of all Maximum values		

ResFc Min	Device Para / Statistics / Min / Max	
-	- . . . Internal test state Table	*S.3*
Resetting of all Minimum values		

Start Vavg via:	Device Para / Statistics / Vavg	
Duration	Duration, StartFct Table	*S.3*
Statistics: Start sliding supervision of the average voltage by the set trigger.		

Start Vavg Fc	Device Para / Statistics / Vavg	
• Only available if: Start Vavg via: = StartFct -	- . . . Internal test state Table	*S.3*
Start of the calculation, if the assigned signal becomes true.		

ResFc Vavg	Device Para / Statistics / Vavg	
-	- . . . Internal test state Table	*S.3*
Resetting of the sliding average calculation.		

Duration Vavg	Device Para / Statistics / Vavg	
• Only available if: Start Vavg via: = Duration 10 min	2 s . . . 30 d Table	*S.3*
Recording time		

Window Vavg	Device Para / Statistics / Vavg	
sliding	sliding, fixed Table	*S.3*
Window configuration		

16.2 Statistics: Direct Controls

ResFc all	Operation / Reset	
Inactive	Inactive, Active Table	*P.1*
Resetting of all Statistic values (Current Demand, Power Demand, Min, Max)		

ResFc Vavg	Operation / Reset	
Inactive	Inactive, Active Table	*P.1*
Resetting of the sliding average calculation.		

ResFc Min	Operation / Reset	
Inactive	Inactive, Active Table	*P.1*
Resetting of all Minimum values		

ResFc Max	Operation / Reset	
Inactive	Inactive, Active Table	*P.1*
Resetting of all Maximum values		

16.3 Statistics: Input States

StartFc Vavg-I	Operation / Status Display / Statistics
State of the module input: Start of Statistics Average Voltage	

16.4 Statistics: Signals (Output States)

ResFc all	Operation / Status Display / Statistics
Signal: Resetting of all Statistic values (Current Demand, Power Demand, Min, Max)	

ResFc Vavg	Operation / Status Display / Statistics
⇧	*Signal: Resetting of the sliding average calculation.*

ResFc Max	Operation / Status Display / Statistics
⇧	*Signal: Resetting of all Maximum values*

ResFc Min	Operation / Status Display / Statistics
⇧	*Signal: Resetting of all Minimum values*

16.5 Statistics: Counters

Res Cr V avg	Operation / Statistics / Vavg
#	*Number of resets since the last device restart. The timestamp shows date and time of the last reset.*

Res Cr Min values	Operation / Statistics / Min / Voltage
#	*Number of resets since the last device restart. The timestamp shows date and time of the last reset.*

Res Cr Max values	Operation / Statistics / Max / Voltage
#	*Number of resets since the last device restart. The timestamp shows date and time of the last reset.*

17 Selection Lists

17.1 yes/no

Selection list referenced by the following parameters:

- Sys . Reboot
- V[1] . Superv. only
- *[...]*

yes/no	Description
no	no
yes	yes

17.2 active/inactive

Selection list referenced by the following parameters:

- Prot . ExBlo Fc
- Prot . ExBlo TripCmd Fc
- V[1] . ExBlo Fc
- V[1] . ExBlo TripCmd Fc
- BO Slot X2 . DISARMED
- *[...]*

active/inactive	Description
Inactive	Inactive
Active	Active

17.3 Mode

Selection list referenced by the following parameters:

- Prot . Function
- Prot . Blo TripCmd
- Prot . Res FaultNo a GridFaultNo
- Sys . Ack BO LED Scd Trips
- Sys . Ack LED
- Sys . Ack BO
- *[. . .]*

Mode	Description
Inactive	Inactive
Active	Active

17.4 True or not true

Selection list referenced by the following parameters:

- Ctrl . Reset max values
- Disturb rec . Man Trigger
- SSV . Ack System LED

True or not true	Description
False	False
True	True

17.5 Scaling

Referenced by:

- Sys . Scaling

Scaling	Description
Per unit values	Per unit values
Primary values	Primary values
Secondary values	Secondary values

17.6 PSet-Switch

Referenced by:

- Sys . PSet-Switch

PSet-Switch	Description
PS1	The currently active Parameter Set is PS1
PS2	The currently active Parameter Set is PS2
PS3	The currently active Parameter Set is PS3
PS4	The currently active Parameter Set is PS4
PSS via Inp fct	Parameter Set Switch via input function
PSS via Scada	Parameter Set Switch via Scada. Write into this output byte the integer of the parameter set that should become active (e.g. 4 => Switch onto parameter set 4).

17.7 Mode

Referenced by:

- Sys . Maint Mode

Mode	Description
Inactive	Inactive
Activation Manually	Arc Flash Reduction Maintenance Manual Mode
Activation via SCADA	Arc Flash Reduction Maintenance SCADA Mode
Activation via DI	Arc Flash Reduction Maintenance Digital Input Mode

17.8 Ack via »C« key

Referenced by:

- Sys . Ack via »C« key

Ack via »C« key	Description
Nothing	No elements can be simply reset via pressing the »C« key for a long time (ca. 1 second). This has the consequence that pressing the »C« key is only a shortcut to the Acknowledge menu, from which the user has to select the elements to be reset.
Ack LEDs w/o passw.	All LEDs are acknowledged (reset) via pressing the »C« key for ca. 1 second. No password has to be entered for this. The reset activity can be recognized from the fact that it always includes an LED test, i.e. all LEDs flash in red color for a second, then flash in green color for a second.
Ack LEDs	All LEDs are reset via pressing the »C« key (for ca. 1 second). The reset activity can be recognized from the fact that it always includes an LED test, i.e. all LEDs flash in red color for a second, then flash in green color for a second.
Ack LEDs and relays	All LEDs and all acknowledgeable binary output relays are reset via pressing the »C« key (for ca. 1 second). The reset activity can be recognized from the fact that it always includes an LED test, i.e. all LEDs flash in red color for a second, then flash in green color for a second.
Ack Everything	All acknowledgeable elements are reset via pressing the »C« key (for ca. 1 second):\n- All LEDs, and\n- all binary output relays, and\n- all latched SCADA signals, and\n- the Trip command.\nThe reset activity can be recognized from the fact that it always includes an LED test, i.e. all LEDs flash in red color for a second, then flash in green color for a second.

17.9 fN

Referenced by:

- Field Para . f

fN	Description
50	Rated frequency
60	Rated frequency

17.10 Phase Sequence

Referenced by:

- Field Para . Phase Sequence

Phase Sequence	Description
ABC	rotating clockwise
ACB	Counter-clockwise phase sequence. Positive and negative phase sequence are exchanged and MTA is turned for 180°.

17.11 VT con

Referenced by:

- VT . VT con

VT con	Description
Phase to Phase	The phase voltage measuring inputs are fed with “Phase-to-Phase” voltages (Delta-Connection)
Phase to Ground	The phase voltage measuring inputs are fed with “Phase-to-Ground” voltages (Star-Connection)

17.12 Voltages to be synchronized

Referenced by:

- VT . V Sync

Voltages to be synchronized	Description
L1	Phase L1
L2	Phase L2
L3	Phase L3
L12	L12
L23	L23
L31	L31

17.13 delta phi - Mode

Referenced by:

- VT . delta phi - Mode

delta phi - Mode	Description
one phase	one phase
two phases	two phases
three phases	three phases

17.14 Switching Authority

Selection list referenced by the following parameters:

- Ctrl . Switching Authority
- Ctrl . Switching Authority

Switching Authority	Description
None	None
Local	Local
Remote	Remote
Local and Remote	Local and Remote

17.15 NonIL ResetMode

Referenced by:

- Ctrl . Res NonIL

NonIL ResetMode	Description
single Operation	single Operation
timeout	timeout
permanent	permanent

17.16 Manipulate Position

Referenced by:

- SG[1] . Manipulate Position

Manipulate Position	Description
Inactive	Inactive
Pos OFF	Signal: Circuit Breaker is in OFF-Position
Pos ON	Signal: Circuit Breaker is in ON-Position

17.17 Device planning

Selection list referenced by the following parameters:

- V[1] . Mode
- VG[1] . Mode

Device planning	Description
-	Do not use
V>	V>
V<	Pickup value

17.18 Alarm Mode

Selection list referenced by the following parameters:

- V[1] . Alarm Mode

Alarm Mode	Description
any one	any one: Trip Command, if the tripping criterion is fulfilled within at least one phase.
any two	any two
all	all: Trip Command for 3p-faults, i.e. if the tripping criterion is fulfilled in all three phases.

17.19 Measuring Mode

Selection list referenced by the following parameters:

- V[1] . Measuring Mode
- LVRT[1] . Measuring Mode

Measuring Mode	Description
Phase to Ground	The voltage transformers are connected to phase-to-ground voltages
Phase to Phase	The voltage transformers are connected to phase-to-phase voltages

17.20 Measuring method

Selection list referenced by the following parameters:

- V[1] . Measuring method
- ReCon[1] . Measuring method

Measuring method	Description
Fundamental	Protection is based on Fundamental (1st. Harmonic)
True RMS	Protection is based on root-mean-square value (True RMS)
Vavg	Sliding Voltage Average Supervision. Note: The settings for the average calculation have to be made within menu [Device Para/Statistics/Vavg].

17.21 Device planning

Selection list referenced by the following parameters:

- df/dt . Mode
- delta phi . Mode
- Intertripping . Mode
- LVRT[1] . Mode
- ExP[1] . Mode
- CBF . Mode
- TCS . Mode
- VTS . Mode

Device planning	Description
-	Do not use
use	use

17.22 Mode

Selection list referenced by the following parameters:

- df/dt . df/dt mode
- f[1] . df/dt mode

Mode	Description
absolute df/dt	positive and negative rise of frequency frequency
positive df/dt	positive rise of frequency
negative df/dt	negative rise of frequency frequency

17.23 Alarm Mode

Selection list referenced by the following parameters:

- LVRT[1] . Alarm Mode

Alarm Mode	Description
any one	any one: Trip Command, if the tripping criterion is fulfilled within at least one phase.
any two	any two: Trip Command only if the tripping criterion is fulfilled in minimum two phases.
all	all: Trip Command for 3p-faults, i.e. if the tripping criterion is fulfilled in all three phases.
only 2	only 2: Trip Command for 2p-faults, i.e. if the tripping criterion is fulfilled in exactly two phases.

17.24 Measuring method

Selection list referenced by the following parameters:

- LVRT[1] . Measuring method
- VG[1] . Measuring method

Measuring method	Description
Fundamental	Protection is based on Fundamental (1st. Harmonic)
True RMS	Protection is based on root-mean-square value (True RMS)

17.25 VG Source

Selection list referenced by the following parameters:

- VG[1] . VG Source

VG Source	Description
measured	VX/VG is measured at the 4th measuring input
calculated	VX/VG is calculated from the three phase-to-ground voltages.

17.26 Device planning

Selection list referenced by the following parameters:

- V012[1] . Mode

Device planning	Description
-	Do not use
V1>	Positive Phase Sequence Overvoltage
V1<	Positive Phase Sequence Undervoltage
V2>	Negative Phase Sequence Overvoltage

17.27 Device planning

Selection list referenced by the following parameters:

- f[1] . Mode

Device planning	Description
-	Do not use
f<	Underfrequency
f>	Overfrequency
f< and df/dt	Underfrequency and (instantaneous) rate of frequency change
f> and df/dt	Overfrequency and (instantaneous) rate of frequency change
f< and DF/DT	Underfrequency and (averaged) rate of frequency change
f> and DF/DT	Overfrequency and (averaged) rate of frequency change
df/dt	Measured value (calculated): Rate-of-frequency-change.
delta phi	Measured value (calculated): Vector surge

17.28 Mode

Selection list referenced by the following parameters:

- ReCon[1] . Mode
- Sync . Mode
- SysA . Mode
- Syslog . Mode
- IRIG-B . Mode
- SNTP . Mode
- Sgen . Mode

Mode	Description
-	Do not use
use	use

17.29 Reconnect. Release Cond

Selection list referenced by the following parameters:

- ReCon[1] . Reconnect. Release Cond

Reconnect. Release Cond	Description
V Internal Release	Release signal is being generated by internal voltage measuring values. The line-to-line voltage exceeds 95% Vn.
V Ext Release PCC	Release signal is being generated by the PCC (External Release). The line-to-line voltage exceeds 95% Vn.
Both	Both: Release signal is being generated by the PCC (External Release) and by internal voltage measuring values.

17.30 SyncMode

Referenced by:

- Sync . SyncMode

SyncMode	Description
System2System	SYSTEM2SYSTEM = SynchronCheck between two systems (Stand-Alone, no breaker info needed)
Generator2System	GENERATOR2SYSTEM = Synchronizing generator to system (breaker close initiate needed).

17.31 Trigger

Referenced by:

- CBF . Trigger

Trigger	Description
- . -	no assignment
All TripCmds	All trip commands that are assigned to this breaker (within the trip manager) will start the BF module.
External TripCmds	All external trip commands that are assigned to this breaker (within the trip manager) will start the BF module.

17.32 Mode

Referenced by:

- TCS . Mode

Mode	Description
Closed	Selects that the breaker is going to be monitored when the breaker is closed.
Either	Selects that the breaker is going to be monitored when the breaker is either closed or open.

17.33 Nom voltage

Selection list referenced by the following parameters:

- DI Slot X1 . Nom voltage
- DI Slot X1 . Nom voltage
- DI Slot X1 . Nom voltage

Nom voltage	Description
24 VDC	24 VDC
48 VDC	48 VDC
60 VDC	60 VDC
110 VDC	110 VDC
230 VDC	230 VDC
110 VAC	110 VAC
230 VAC	230 VAC

17.34 Debouncing time

Selection list referenced by the following parameters:

- DI Slot X1 . Debouncing time 1
- DI Slot X1 . Debouncing time 2
- DI Slot X1 . Debouncing time 3
- DI Slot X1 . Debouncing time 4
- DI Slot X1 . Debouncing time 5
- DI Slot X1 . Debouncing time 6
- *[. . .]*

Debouncing time	Description
no debouncing time	no debouncing time
20 ms	20 ms
50 ms	50 ms
100 ms	100 ms

17.35 Relay operating modes

Selection list referenced by the following parameters:

- BO Slot X2 . Force all Outs
- BO Slot X2 . Force OR1

Relay operating modes	Description
Normal	Normal
De-Energized	De-Energized
Energized	Energized

17.36 Mode

Selection list referenced by the following parameters:

- BO Slot X2 . Disarm Mode
- BO Slot X2 . Force Mode

Mode	Description
permanent	permanent
timeout	timeout

17.37 1...n Operating Modes

Selection list referenced by the following parameters:

- BO Slot X2 . Operating Mode
- BO Slot X2 . Operating Mode
- BO Slot X2 . Operating Mode
- BO Slot X2 . Operating Mode
- BO Slot X2 . Operating Mode

1...n Operating Modes	Description
Normally open (NO)	The working principle of the relay corresponds to a normally open contact.
Normally closed (NC)	The working principle of the relay corresponds to a normally closed contact.

17.38 Mode

Selection list referenced by the following parameters:

- LEDs group A . Latched
- LEDs group A . Latched
- LEDs group A . Latched
- LEDs group A . Latched
- LEDs group A . Latched
- LEDs group A . Latched
- *[...]*

Mode	Description
Inactive	Inactive
Active	Active
active, ack. by alarm	Latching of LEDs is active, but will be acknowledged (reset) automatically (by the »Prot« module) in case of a General Alarm.

17.39 LED active color

Selection list referenced by the following parameters:

- LEDs group A . LED active color
- LEDs group A . LED inactive color
- LEDs group A . LED active color
- LEDs group A . LED inactive color
- LEDs group A . LED active color
- LEDs group A . LED inactive color
- *[. . .]*

LED active color	Description
green	green
red	red
red flash	red flashing
green flash	green blinking
-	No assignment

17.40 Rec state

Referenced by:

- Disturb rec . Rec state

Rec state	Description
Ready	Ready
Recording	Recording
Writing file	Signal: Writing file
Trigger Blo	Trigger signal is still active - wait for fallback. A new record can only be started if and only the trigger signal that started the previous record has fallen back once. Therewith endless records are prevented.

17.41 Fault

Referenced by:

- Disturb rec . Error code

Fault	Description
OK	OK
Write err	Signal: Writing error in memory
Clear fail	Signal: Clear failure in memory
Calculation err	Calculation error
File not found	File not found
Auto overwriting off	If there is no more memory available the record is being stopped.

17.42 Record-Mode

Referenced by:

- Fault rec . Record-Mode

Record-Mode	Description
Alarms and Trips	A recording is started in case of an alarm or a trip.
Trips only	A recording is started only in case of a trip.

17.43 Resolution

Referenced by:

- Trend rec . Resolution

Resolution	Description
60 min	Add next entry: 60 min
30 min	Add next entry: 30 min
15 min	Add next entry: 15 min
10 min	Add next entry: 10 min
5 min	Add next entry: 5 min
1 min	Add next entry: 1 min

17.44 TLS Certificate

Referenced by:

- Sys . TLS Certificate

TLS Certificate	Description
Device-specific	The device uses a device-specific certificate for the encrypted communication. This corresponds to the highest security-level of the communication.
Basic	The device uses a basic certificate for the encrypted communication. Compared with a device-specific certificate, this means a slightly reduced security level.
Corrupt	The certificate for the encrypted communication is corrupt and therefore unusable.

17.45 Type of passw. def.

Selection list referenced by the following parameters:

- Sys . Passw.remote net.conn.
- Sys . Passw. for USB conn.

Type of passw. def.	Description
disabled	The password disabled.
default	The password is the same as the factory default, i.e. it has not been altered by the user. (However, for devices with a disabled default password the password type is displayed as “disabled”, not as “default”.)
def. by user	The password has been defined by the user. This corresponds to the highest security-level of the access to the device.

17.46 Conf. Dev. Reset

Selection list referenced by the following parameters:

- HMI . Conf. Dev. Reset
- HMI . Conf. Dev. Reset

Conf. Dev. Reset	Description
"Fact.def.", "PW rst"	Two Reset Options shall be available:\n- "Reset to factory defaults",\n- "Reset passwords".
Only “Fact.defaults”	Only one Reset Option shall be available:\n- "Reset to factory defaults".\nCAUTION: If this option has been chosen and the password should ever get lost then the only chance to recover control is to reset the protection device to factory defaults.
Reset deact.	The Reset Options shall be deactivated.\nCAUTION: If this option has been chosen and the password should ever get lost, then the protection device has to be sent to the manufacturer as a service request.

17.47 Mode

Referenced by:

- Red.Ethernet . Mode

Mode	Description
Switch	Switch
PRP	Parallel Redundancy Protocol
HSR	High-Availability Seamless Redundancy Protocol

17.48 Duplex mode

Selection list referenced by the following parameters:

- Red.Ethernet . Duplex mode A
- Red.Ethernet . Duplex mode B

Duplex mode	Description
Unknown	Unknown
Half	Full Duplex
Full	Full Duplex

17.49 Speed

Selection list referenced by the following parameters:

- Red.Ethernet . Speed A
- Red.Ethernet . Speed B

Speed	Description
Unknown	Unknown
10MBits	10MBits
100MBits	100MBits

17.50 Mode

Referenced by:

- PTP . Mode

Mode	Description
-	Do not use
Default E2E	Default profile and E2E path delay mechanism
Default P2P	Default profile and P2P path delay mechanism
IEEE C37.238	IEEE C37.238-2017 and IEC/IEEE 61850-9-3:2016
IEC 61850-9-3:2016	IEC/IEEE 61850-9-3:2016 Achtung: Die default Domain Number ist 93 und weicht vom voreingestellten Wert 0 ab.

17.51 Delay mech.

Referenced by:

- PTP . Delay mech.

Delay mech.	Description
Off	Off
End-to-End	End-to-End
Peer-to-Peer	Peer-to-Peer

17.52 Net.Trans.Prot.

Referenced by:

- PTP . Net.Trans.Prot.

Net.Trans.Prot.	Description
IEEE 802.3	IEEE 802.3
UDP IPv4	UDP IPv4

17.53 PeerInt.

Selection list referenced by the following parameters:

- PTP . PathDelay Intv.
- PTP . PeerPathDelay Intv.

PeerInt.	Description
1	1
2	2
4	4
8	8
16	16
32	32
64	64
128	128
256	256

17.54 Sync Status

Referenced by:

- PTP . Sync Status

Sync Status	Description
Init	Init
Faulty	Faulty
Disable	Disable
Listening	Listening
PerMaster	PerMaster
Master	Master
Passive	Passive
Uncalibrated	Uncalibrated
Slave	Slave

17.55 Vlan act.

Referenced by:

- PTP . Vlan act.

Vlan act.	Description
Inactive	Inactive
Active	Active

17.56 Baud rate

Referenced by:

- DNP3 . Baud rate

Baud rate	Description
1200	1200
2400	2400
4800	4800
9600	9600
19200	19200
38400	38400
57600	57600
115200	115200

17.57 Byte Frame

Selection list referenced by the following parameters:

- DNP3 . Frame Layout
- Modbus . Physical Settings
- IEC103 . Physical Settings

Byte Frame	Description
8E1	8 data bits, even parity, 1 stopbit.
8O1	8 data bits, odd, 1 stopbit.
8N1	8 data bits, no parity, 1 stopbit.
8N2	8 data bits, no parity, 2 stopbits.

17.58 Optical rest position

Selection list referenced by the following parameters:

- DNP3 . Optical rest position
- Modbus . Optical rest position

Optical rest position	Description
Light off	Light off
Light on	Light on

17.59 Communication Start Variants

Referenced by:

- DNP3 . DataLink confirm

Communication Start Variants	Description
Never	Option Never is recommended
Always	If this variable is set to Always then LinkLayer needs to establish a connection before sending any Frame.
On_Large	If set to On_Large then a connection needs to be established before sending the first Frame of a multi Term Message

17.60 _AL_ResponseType_k

Referenced by:

- DNP3 . AppLink confirm

_AL_ResponseType_k	Description
Never	Never
Always	Always
Event	Event

17.61 Scale Factor

Referenced by:

- DNP3 . Scale Factor 0
- *[. . .]*

Scale Factor	Description
0.001	0.001
0.01	0.01
0.1	0.1
1	1
10	10
100	100
1000	1000
10000	10000
100000	100000
1000000	1000000

17.62 Baud rate

Referenced by:

- Modbus . Baud rate

Baud rate	Description
1200	1200
2400	2400
4800	4800
9600	9600
19200	19200
38400	38400

17.63 Port selection

Selection list referenced by the following parameters:

- Modbus . TCP Port Config
- IEC104 . TCP Port Config

Port selection	Description
Default	Default Port
Private	Private Port

17.64 Type of SCADA mapping

Selection list referenced by the following parameters:

- Modbus . Type of SCADA mapping
- IEC103 . Type of SCADA mapping
- IEC104 . Type of SCADA mapping
- Profibus . Type of SCADA mapping

Type of SCADA mapping	Description
Standard	Default mapping of data objects
User-defined	User-defined mapping of data objects

17.65 Config status

Selection list referenced by the following parameters:

- Modbus . Config status
- IEC103 . Config status
- IEC104 . Config status
- Profibus . Config status

Config status	Description
Changing	New SCADA configuration is being loaded, but not active yet.
OK	The SCADA configuration is active.
Config. not avail.	The user-defined SCADA configuration is not available (e.g. has not been loaded into the device).
Error	Unexpected error. Please contact our service-team.

17.66 1..n, OnOffList

Referenced by:

- IEC 61850 . Function

1..n, OnOffList	Description
Inactive	Inactive
Active	Active

17.67 State

Selection list referenced by the following parameters:

- IEC 61850 . GoosePublisherState
- IEC 61850 . GooseSubscriberState
- IEC 61850 . MmsServerState

State	Description
Off	Off
On	On
Error	Error

17.68 Baud rate

Referenced by:

- IEC103 . Baud rate

Baud rate	Description
1200	1200
2400	2400
4800	4800
9600	9600
19200	19200
38400	38400
57600	57600

17.69 Timezone

Selection list referenced by the following parameters:

- IEC103 . Timezone
- IEC104 . Timezone

Timezone	Description
UTC	UTC
Local Time	Local time according to the »Time Zones« setting (in Device Parameters) (incl. daylight saving settings).

17.70 PNO Id

Referenced by:

- Profibus . PNO Id

PNO Id	Description
0C50h	PnodID for the Config file.

17.71 Baud rate

Referenced by:

- Profibus . Baud rate

Baud rate	Description
12 Mb/s	12 Mb/s
6 Mb/s	6 Mb/s
3 Mb/s	3 Mb/s
1.5 Mb/s	1.5 Mb/s
0.5 Mb/s	0.5 Mb/s
187500 baud	187500 baud
93750 baud	93750 baud
45450 baud	45450 baud
19200 baud	19200 baud
9600 baud	9600 baud
-.-	-.-

17.72 State

Referenced by:

- Profibus . Slave State

State	Description
Baud Search	No connection to the PROFIBUS-DP Master
Baud Found	The PROFIBUS DP Slave is connected to the bus. The Slave has not yet been addressed by the Master Device (and it was not yet addressed since the last break of the connection).
PRM OK	The slave was addressed by the master, the parameter setting message was received and is OK, a configuration message is expected from the master.
PRM REQ	The slave is no longer addressed by the master (modified parameters within the master without having the connection stopped, master software is tuned off but lower PROFIBUS layer is still active)
PRM Fault	An Error in the parameter setting message (e.g. wrong PNO identification number)
CFG Fault	Configuration error the number of input/output bytes parameterised in the master does not match the number parametrised in the device (slave).
Clear Data	Master sends a General Control command to clear the data.
Data exchange	Master and slave exchange data.

17.73 IRIG-B00X

Referenced by:

- IRIG-B . IRIG-B00X

IRIG-B00X	Description
IRIGB-000	Please refer to: IRIG STANDARD 200-04
IRIGB-001	Please refer to: IRIG STANDARD 200-04
IRIGB-002	Please refer to: IRIG STANDARD 200-04
IRIGB-003	Please refer to: IRIG STANDARD 200-04
IRIGB-004	Please refer to: IRIG STANDARD 200-04
IRIGB-005	Please refer to: IRIG STANDARD 200-04
IRIGB-006	Please refer to: IRIG STANDARD 200-04
IRIGB-007	Please refer to: IRIG STANDARD 200-04

17.74 Server State

Referenced by:

- SNTP . Used Server

Server State	Description
Server1	Server1 used.
Server2	Server2 used.
None	No Server used.

17.75 State

Selection list referenced by the following parameters:

- SNTP . ServerQlty
- SNTP . NetConn

State	Description
GOOD	GOOD
SUFFICIENT	SUFFICIENT
BAD	BAD
-	NO CONNECTION

17.76 Time Zones

Referenced by:

- TimeSync . Time Zones

Time Zones	Description
UTC+14 Kiritimati	UTC+14 Kiritimati
UTC+13 Rawaki	UTC+13 Rawaki
UTC+12.75 Chatham Island	UTC+12.75 Chatham Island
UTC+12 Wellington	UTC+12 Wellington
UTC+11.5 Kingston	UTC+11.5 Kingston
UTC+11 Port Vila	UTC+11 Port Vila
UTC+10.5 Lord Howe Island	UTC+10.5 Lord Howe Island
UTC+10 Sydney	UTC+10 Sydney
UTC+9.5 Adelaide	UTC+9.5 Adelaide
UTC+9 Tokyo	UTC+9 Tokyo
UTC+8 Hong Kong	UTC+8 Hong Kong
UTC+7 Bangkok	UTC+7 Bangkok

Time Zones	Description
UTC+6.5 Rangoon	UTC+6.5 Rangoon
UTC+6 Colombo	UTC+6 Colombo
UTC+5.75 Kathmandu	UTC+5.75 Kathmandu
UTC+5.5 New Delhi	UTC+5.5 New Delhi
UTC+5 Islamabad	UTC+5 Islamabad
UTC+4.5 Kabul	UTC+4.5 Kabul
UTC+4 Abu Dhabi	UTC+4 Abu Dhabi
UTC+3.5 Tehran	UTC+3.5 Tehran
UTC+3 Moscow	UTC+3 Moscow
UTC+2 Athens	UTC+2 Athens
UTC+1 Berlin	UTC+1 Berlin
UTC+0 London	UTC+0 London
UTC-1 Azores	UTC-1 Azores
UTC-2 Fern. d. Noronha	UTC-2 Fern. d. Noronha
UTC-3 Buenos Aires	UTC-3 Buenos Aires
UTC-3.5 St. John’s	UTC-3.5 St. John’s
UTC-4 Santiago	UTC-4 Santiago
UTC-5 New York	UTC-5 New York
UTC-6 Chicago	UTC-6 Chicago
UTC-7 Salt Lake City	UTC-7 Salt Lake City
UTC-8 Los Angeles	UTC-8 Los Angeles
UTC-9 Anchorage	UTC-9 Anchorage
UTC-9.5 Taiohae	UTC-9.5 Taiohae
UTC-10 Honolulu	UTC-10 Honolulu
UTC-11 Midway Islands	UTC-11 Midway Islands

17.77 Month of clock change

Selection list referenced by the following parameters:

- TimeSync . Summertime m
- TimeSync . Wintertime m

Month of clock change	Description
January	January
February	February
March	March
April	April
May	May
June	June
July	July
August	August
September	September
October	October
November	November
December	December

17.78 Date

Selection list referenced by the following parameters:

- TimeSync . Summertime d
- TimeSync . Wintertime d

Date	Description
Sunday	Sunday
Monday	Monday
Tuesday	Tuesday
Wednesday	Wednesday
Thursday	Thursday
Friday	Friday
Saturday	Saturday
General day	General day: Examples: first day of month, last day of month

17.79 Day of clock change

Selection list referenced by the following parameters:

- TimeSync . Summertime w
- TimeSync . Wintertime w

Day of clock change	Description
First	First week of the month
Second	Second week of the month
Third	Third week of the month
Fourth	Fourth week of the month
Last	Last week of the month

17.80 Duration

Referenced by:

- Statistics . Start Vavg via:

Duration	Description
Duration	Recording time
StartFct	Start function

17.81 Duration

Referenced by:

- Statistics . Duration Vavg

Duration	Description
2 s	s
5 s	s
10 s	s
15 s	seconds
30 s	seconds
1 min	minute
5 min	minute
10 min	minute
15 min	minute
30 min	minute
1 h	Hours
2 h	Hours

Duration	Description
6 h	Hours
12 h	Hours
1 d	days
2 d	days
5 d	days
7 d	days
10 d	days
30 d	days

17.82 Window configuration

Referenced by:

- Statistics . Window Vavg

Window configuration	Description
sliding	Moving mean: Continuously the newest measuring value is added and the oldest measuring value is removed from the moving mean (average value).
fixed	The average value is calculated for a fixed window.

17.83 No of Equations:

Referenced by:

- Logics . No of Equations:

No of Equations:	Description
0	0
5	5
10	10
20	20
40	40
80	80

17.84 LE1.Gate

Referenced by:

- Logics . LE1.Gate

LE1.Gate	Description
AND	AND Gate
OR	OR Gate
NAND	NAND Gate
NOR	NOR Gate

17.85 LE2.Gate

Referenced by:

LE2.Gate	Description
AND	AND Gate
OR	OR Gate
NAND	NAND Gate
NOR	NOR Gate

17.86 LE3.Gate

Referenced by:

LE3.Gate	Description
AND	AND Gate
OR	OR Gate
NAND	NAND Gate
NOR	NOR Gate

17.87 LE4.Gate

Referenced by:

LE4.Gate	Description
AND	AND Gate
OR	OR Gate
NAND	NAND Gate
NOR	NOR Gate

17.88 LE5.Gate

Referenced by:

LE5.Gate	Description
AND	AND Gate
OR	OR Gate
NAND	NAND Gate
NOR	NOR Gate

17.89 LE6.Gate

Referenced by:

LE6.Gate	Description
AND	AND Gate
OR	OR Gate
NAND	NAND Gate
NOR	NOR Gate

17.90 LE7.Gate

Referenced by:

LE7.Gate	Description
AND	AND Gate
OR	OR Gate
NAND	NAND Gate
NOR	NOR Gate

17.91 LE8.Gate

Referenced by:

LE8.Gate	Description
AND	AND Gate
OR	OR Gate
NAND	NAND Gate
NOR	NOR Gate

17.92 LE9.Gate

Referenced by:

LE9.Gate	Description
AND	AND Gate
OR	OR Gate
NAND	NAND Gate
NOR	NOR Gate

17.93 LE10.Gate

Referenced by:

LE10.Gate	Description
AND	AND Gate
OR	OR Gate
NAND	NAND Gate
NOR	NOR Gate

17.94 LE11.Gate

Referenced by:

LE11.Gate	Description
AND	AND Gate
OR	OR Gate
NAND	NAND Gate
NOR	NOR Gate

17.95 LE12.Gate

Referenced by:

LE12.Gate	Description
AND	AND Gate
OR	OR Gate
NAND	NAND Gate
NOR	NOR Gate

17.96 LE13.Gate

Referenced by:

LE13.Gate	Description
AND	AND Gate
OR	OR Gate
NAND	NAND Gate
NOR	NOR Gate

17.97 LE14.Gate

Referenced by:

LE14.Gate	Description
AND	AND Gate
OR	OR Gate
NAND	NAND Gate
NOR	NOR Gate

17.98 LE15.Gate

Referenced by:

LE15.Gate	Description
AND	AND Gate
OR	OR Gate
NAND	NAND Gate
NOR	NOR Gate

17.99 LE16.Gate

Referenced by:

LE16.Gate	Description
AND	AND Gate
OR	OR Gate
NAND	NAND Gate
NOR	NOR Gate

17.100 LE17.Gate

Referenced by:

LE17.Gate	Description
AND	AND Gate
OR	OR Gate
NAND	NAND Gate
NOR	NOR Gate

17.101 LE18.Gate

Referenced by:

LE18.Gate	Description
AND	AND Gate
OR	OR Gate
NAND	NAND Gate
NOR	NOR Gate

17.102 LE19.Gate

Referenced by:

LE19.Gate	Description
AND	AND Gate
OR	OR Gate
NAND	NAND Gate
NOR	NOR Gate

17.103 LE20.Gate

Referenced by:

LE20.Gate	Description
AND	AND Gate
OR	OR Gate
NAND	NAND Gate
NOR	NOR Gate

17.104 LE21.Gate

Referenced by:

LE21.Gate	Description
AND	AND Gate
OR	OR Gate
NAND	NAND Gate
NOR	NOR Gate

17.105 LE22.Gate

Referenced by:

LE22.Gate	Description
AND	AND Gate
OR	OR Gate
NAND	NAND Gate
NOR	NOR Gate

17.106 LE23.Gate

Referenced by:

LE23.Gate	Description
AND	AND Gate
OR	OR Gate
NAND	NAND Gate
NOR	NOR Gate

17.107 LE24.Gate

Referenced by:

LE24.Gate	Description
AND	AND Gate
OR	OR Gate
NAND	NAND Gate
NOR	NOR Gate

17.108 LE25.Gate

Referenced by:

LE25.Gate	Description
AND	AND Gate
OR	OR Gate
NAND	NAND Gate
NOR	NOR Gate

17.109 LE26.Gate

Referenced by:

LE26.Gate	Description
AND	AND Gate
OR	OR Gate
NAND	NAND Gate
NOR	NOR Gate

17.110 LE27.Gate

Referenced by:

LE27.Gate	Description
AND	AND Gate
OR	OR Gate
NAND	NAND Gate
NOR	NOR Gate

17.111 LE28.Gate

Referenced by:

LE28.Gate	Description
AND	AND Gate
OR	OR Gate
NAND	NAND Gate
NOR	NOR Gate

17.112 LE29.Gate

Referenced by:

LE29.Gate	Description
AND	AND Gate
OR	OR Gate
NAND	NAND Gate
NOR	NOR Gate

17.113 LE30.Gate

Referenced by:

LE30.Gate	Description
AND	AND Gate
OR	OR Gate
NAND	NAND Gate
NOR	NOR Gate

17.114 LE31.Gate

Referenced by:

LE31.Gate	Description
AND	AND Gate
OR	OR Gate
NAND	NAND Gate
NOR	NOR Gate

17.115 LE32.Gate

Referenced by:

LE32.Gate	Description
AND	AND Gate
OR	OR Gate
NAND	NAND Gate
NOR	NOR Gate

17.116 LE33.Gate

Referenced by:

LE33.Gate	Description
AND	AND Gate
OR	OR Gate
NAND	NAND Gate
NOR	NOR Gate

17.117 LE34.Gate

Referenced by:

LE34.Gate	Description
AND	AND Gate
OR	OR Gate
NAND	NAND Gate
NOR	NOR Gate

17.118 LE35.Gate

Referenced by:

LE35.Gate	Description
AND	AND Gate
OR	OR Gate
NAND	NAND Gate
NOR	NOR Gate

17.119 LE36.Gate

Referenced by:

LE36.Gate	Description
AND	AND Gate
OR	OR Gate
NAND	NAND Gate
NOR	NOR Gate

17.120 LE37.Gate

Referenced by:

LE37.Gate	Description
AND	AND Gate
OR	OR Gate
NAND	NAND Gate
NOR	NOR Gate

17.121 LE38.Gate

Referenced by:

LE38.Gate	Description
AND	AND Gate
OR	OR Gate
NAND	NAND Gate
NOR	NOR Gate

17.122 LE39.Gate

Referenced by:

LE39.Gate	Description
AND	AND Gate
OR	OR Gate
NAND	NAND Gate
NOR	NOR Gate

17.123 LE40.Gate

Referenced by:

LE40.Gate	Description
AND	AND Gate
OR	OR Gate
NAND	NAND Gate
NOR	NOR Gate

17.124 LE41.Gate

Referenced by:

LE41.Gate	Description
AND	AND Gate
OR	OR Gate
NAND	NAND Gate
NOR	NOR Gate

17.125 LE42.Gate

Referenced by:

LE42.Gate	Description
AND	AND Gate
OR	OR Gate
NAND	NAND Gate
NOR	NOR Gate

17.126 LE43.Gate

Referenced by:

LE43.Gate	Description
AND	AND Gate
OR	OR Gate
NAND	NAND Gate
NOR	NOR Gate

17.127 LE44.Gate

Referenced by:

LE44.Gate	Description
AND	AND Gate
OR	OR Gate
NAND	NAND Gate
NOR	NOR Gate

17.128 LE45.Gate

Referenced by:

LE45.Gate	Description
AND	AND Gate
OR	OR Gate
NAND	NAND Gate
NOR	NOR Gate

17.129 LE46.Gate

Referenced by:

LE46.Gate	Description
AND	AND Gate
OR	OR Gate
NAND	NAND Gate
NOR	NOR Gate

17.130 LE47.Gate

Referenced by:

LE47.Gate	Description
AND	AND Gate
OR	OR Gate
NAND	NAND Gate
NOR	NOR Gate

17.131 LE48.Gate

Referenced by:

LE48.Gate	Description
AND	AND Gate
OR	OR Gate
NAND	NAND Gate
NOR	NOR Gate

17.132 LE49.Gate

Referenced by:

LE49.Gate	Description
AND	AND Gate
OR	OR Gate
NAND	NAND Gate
NOR	NOR Gate

17.133 LE50.Gate

Referenced by:

LE50.Gate	Description
AND	AND Gate
OR	OR Gate
NAND	NAND Gate
NOR	NOR Gate

17.134 LE51.Gate

Referenced by:

LE51.Gate	Description
AND	AND Gate
OR	OR Gate
NAND	NAND Gate
NOR	NOR Gate

17.135 LE52.Gate

Referenced by:

LE52.Gate	Description
AND	AND Gate
OR	OR Gate
NAND	NAND Gate
NOR	NOR Gate

17.136 LE53.Gate

Referenced by:

LE53.Gate	Description
AND	AND Gate
OR	OR Gate
NAND	NAND Gate
NOR	NOR Gate

17.137 LE54.Gate

Referenced by:

LE54.Gate	Description
AND	AND Gate
OR	OR Gate
NAND	NAND Gate
NOR	NOR Gate

17.138 LE55.Gate

Referenced by:

LE55.Gate	Description
AND	AND Gate
OR	OR Gate
NAND	NAND Gate
NOR	NOR Gate

17.139 LE56.Gate

Referenced by:

LE56.Gate	Description
AND	AND Gate
OR	OR Gate
NAND	NAND Gate
NOR	NOR Gate

17.140 LE57.Gate

Referenced by:

LE57.Gate	Description
AND	AND Gate
OR	OR Gate
NAND	NAND Gate
NOR	NOR Gate

17.141 LE58.Gate

Referenced by:

LE58.Gate	Description
AND	AND Gate
OR	OR Gate
NAND	NAND Gate
NOR	NOR Gate

17.142 LE59.Gate

Referenced by:

LE59.Gate	Description
AND	AND Gate
OR	OR Gate
NAND	NAND Gate
NOR	NOR Gate

17.143 LE60.Gate

Referenced by:

LE60.Gate	Description
AND	AND Gate
OR	OR Gate
NAND	NAND Gate
NOR	NOR Gate

17.144 LE61.Gate

Referenced by:

LE61.Gate	Description
AND	AND Gate
OR	OR Gate
NAND	NAND Gate
NOR	NOR Gate

17.145 LE62.Gate

Referenced by:

LE62.Gate	Description
AND	AND Gate
OR	OR Gate
NAND	NAND Gate
NOR	NOR Gate

17.146 LE63.Gate

Referenced by:

LE63.Gate	Description
AND	AND Gate
OR	OR Gate
NAND	NAND Gate
NOR	NOR Gate

17.147 LE64.Gate

Referenced by:

LE64.Gate	Description
AND	AND Gate
OR	OR Gate
NAND	NAND Gate
NOR	NOR Gate

17.148 LE65.Gate

Referenced by:

LE65.Gate	Description
AND	AND Gate
OR	OR Gate
NAND	NAND Gate
NOR	NOR Gate

17.149 LE66.Gate

Referenced by:

LE66.Gate	Description
AND	AND Gate
OR	OR Gate
NAND	NAND Gate
NOR	NOR Gate

17.150 LE67.Gate

Referenced by:

LE67.Gate	Description
AND	AND Gate
OR	OR Gate
NAND	NAND Gate
NOR	NOR Gate

17.151 LE68.Gate

Referenced by:

LE68.Gate	Description
AND	AND Gate
OR	OR Gate
NAND	NAND Gate
NOR	NOR Gate

17.152 LE69.Gate

Referenced by:

LE69.Gate	Description
AND	AND Gate
OR	OR Gate
NAND	NAND Gate
NOR	NOR Gate

17.153 LE70.Gate

Referenced by:

LE70.Gate	Description
AND	AND Gate
OR	OR Gate
NAND	NAND Gate
NOR	NOR Gate

17.154 LE71.Gate

Referenced by:

LE71.Gate	Description
AND	AND Gate
OR	OR Gate
NAND	NAND Gate
NOR	NOR Gate

17.155 LE72.Gate

Referenced by:

LE72.Gate	Description
AND	AND Gate
OR	OR Gate
NAND	NAND Gate
NOR	NOR Gate

17.156 LE73.Gate

Referenced by:

LE73.Gate	Description
AND	AND Gate
OR	OR Gate
NAND	NAND Gate
NOR	NOR Gate

17.157 LE74.Gate

Referenced by:

LE74.Gate	Description
AND	AND Gate
OR	OR Gate
NAND	NAND Gate
NOR	NOR Gate

17.158 LE75.Gate

Referenced by:

LE75.Gate	Description
AND	AND Gate
OR	OR Gate
NAND	NAND Gate
NOR	NOR Gate

17.159 LE76.Gate

Referenced by:

LE76.Gate	Description
AND	AND Gate
OR	OR Gate
NAND	NAND Gate
NOR	NOR Gate

17.160 LE77.Gate

Referenced by:

LE77.Gate	Description
AND	AND Gate
OR	OR Gate
NAND	NAND Gate
NOR	NOR Gate

17.161 LE78.Gate

Referenced by:

LE78.Gate	Description
AND	AND Gate
OR	OR Gate
NAND	NAND Gate
NOR	NOR Gate

17.162 LE79.Gate

Referenced by:

LE79.Gate	Description
AND	AND Gate
OR	OR Gate
NAND	NAND Gate
NOR	NOR Gate

17.163 LE80.Gate

Referenced by:

LE80.Gate	Description
AND	AND Gate
OR	OR Gate
NAND	NAND Gate
NOR	NOR Gate

17.164 TripCmd Mode

Referenced by:

- Sgen . TripCmd Mode

TripCmd Mode	Description
No TripCmd	No Trip Command: The TripCmd of all protection functions is blocked. The protection function will possibly trip but not generate a TripCmd.
With TripCmd	With Trip Command: The trip of a protection function generates a TripCmd, that can open the circuit breaker.

17.165 State

Referenced by:

- Sgen . State

State	Description
Off	Off
PreFault	Pre Fault Duration
FaultSimulation	Duration of Fault Simulation
PostFault	Post Fault Duration
Init Res	Init Reset

17.166 1..n, Assignment List

Selection list referenced by the following parameters:

- Prot . ExBlo1
- Prot . ExBlo TripCmd
- Sys . Ack LED
- Sys . Ack BO
- Sys . Ack Scada
- *[...]*

1..n, Assignment List	Description
-	No assignment
available	Signal: Protection is available
Active	Signal: active
ExBlo	Signal: External Blocking
Blo TripCmd	Signal: Trip Command blocked
ExBlo TripCmd	Signal: External Blocking of the Trip Command

1..n, Assignment List	Description
Alarm L1	Signal: General-Alarm L1
Alarm L2	Signal: General-Alarm L2
Alarm L3	Signal: General-Alarm L3
Alarm G	Signal: General-Alarm - Earth fault
Alarm	Signal: General Alarm
Trip L1	Signal: General Trip L1
Trip L2	Signal: General Trip L2
Trip L3	Signal: General Trip L3
Trip G	Signal: General Trip Ground fault
Trip	Signal: General Trip
Res FaultNo a GridFaultNo	Signal: Resetting of fault number and grid fault number.
ExBlo1-I	Module input state: External blocking1
ExBlo2-I	Module input state: External blocking2
ExBlo TripCmd-I	Module input state: External Blocking of the Trip Command
Phase seq. wrong	Signal that the device has detected a phase sequence (L1-L2-L3 / L1-L3-L2) that is different from the one that had been set at [Field settings / General Settings] »Phase Sequence«.
Local	Switching Authority: Local
Remote	Switching Authority: Remote
NonInterl	Non-Interlocking is active
SG Indeterm	(At least one) Switchgear is moving (Position cannot be determined).
SG Disturb	(At least one) Switchgear is disturbed.
NonInterl-I	Non-Interlocking
SI SingleContactInd	Signal: The Position of the Switchgear is detected by one auxiliary contact (pole) only. Thus indeterminate and disturbed Positions cannot be detected.
Pos not ON	Signal: Pos not ON
Pos ON	Signal: Circuit Breaker is in ON-Position
Pos OFF	Signal: Circuit Breaker is in OFF-Position
Pos Indeterm	Signal: Circuit Breaker is in Indeterminate Position
Pos Disturb	Signal: Circuit Breaker Disturbed - Undefined Breaker Position. The Position Indicators contradict themselves. After expiring of a supervision timer this signal becomes true.
Ready	Signal: Circuit breaker is ready for operation.
t-Dwell	Signal: Dwell time
Removed	Signal: The withdrawable circuit breaker is Removed
Interl ON	Signal: One or more IL_On inputs are active.
Interl OFF	Signal: One or more IL_Off inputs are active.
CES succesf	Signal: Command Execution Supervision: Switching command executed successfully.
CES Disturbed	Signal: Command Execution Supervision: Switching Command unsuccessful. Switchgear in disturbed position.
CES Fail TripCmd	Signal: Command Execution Supervision: Command execution failed because trip command is pending.

1..n, Assignment List	Description
CES SwitchDir	Signal: Command Execution Supervision respectively Switching Direction Control: This signal becomes true, if a switch command is issued even though the switchgear is already in the requested position. Example: A switchgear that is already OFF should be switched OFF again (doubly). The same applies to CLOSE commands.
CES ON d OFF	Signal: Command Execution Supervision: On Command during a pending OFF Command.
CES SG not ready	Signal: Command Execution Supervision: Switchgear not ready
CES Fiel Interl	Signal: Command Execution Supervision: Switching Command not executed because of field interlocking.
CES SyncTimeout	Signal: Command Execution Supervision: Switching Command not executed. No Synchronization signal while t-sync was running.
CES SG removed	Signal: Command Execution Supervision: Switching Command unsuccessful, Switchgear removed.
Prot ON	Signal: ON Command issued by the Prot module
TripCmd	Signal: Trip Command
Ack TripCmd	Signal: Acknowledge Trip Command
ON incl Prot ON	Signal: The ON Command includes the ON Command issued by the Protection module.
OFF incl TripCmd	Signal: The OFF Command includes the OFF Command issued by the Protection module.
Position Ind manipul	Signal: Position Indicators faked
SGwear Slow SG	Signal: Alarm, the circuit breaker (load-break switch) becomes slower
Res SGwear Sl SG	Signal: Resetting the slow Switchgear Alarm
ON Cmd	Signal: ON Command issued to the switchgear. Depending on the setting the signal may include the ON command of the Prot module.
OFF Cmd	Signal: OFF Command issued to the switchgear. Depending on the setting the signal may include the OFF command of the Prot module.
ON Cmd manual	Signal: ON Cmd manual
OFF Cmd manual	Signal: OFF Cmd manual
Sync ON request	Signal: Synchronous ON request
Test Trip Cmd	A trip command has been triggered manually (for testing purposes).
Aux ON-I	Module Input State: Position indicator/check-back signal of the CB (52a)
Aux OFF-I	Module input state: Position indicator/check-back signal of the CB (52b)
Ready-I	Module input state: CB ready
Sys-in-Sync-I	State of the module input: This signals has to become true within the synchronization time. If not, switching is unsuccessful.
Removed-I	State of the module input: The withdrawable circuit breaker is Removed
Ack TripCmd-I	State of the module input: Acknowledgement Signal (for the Trip Command) Module input signal
Interl ON1-I	State of the module input: Interlocking of the ON command
Interl ON2-I	State of the module input: Interlocking of the ON command
Interl ON3-I	State of the module input: Interlocking of the ON command
Interl OFF1-I	State of the module input: Interlocking of the OFF command
Interl OFF2-I	State of the module input: Interlocking of the OFF command
Interl OFF3-I	State of the module input: Interlocking of the OFF command

1..n, Assignment List	Description
SCmd ON-I	State of the module input: Switching ON Command, e.g. the state of the Logics or the state of the digital input
SCmd OFF-I	State of the module input: Switching OFF Command, e.g. the state of the Logics or the state of the digital input
Operations Alarm	Signal: Too many Operations. (The operations counter »TripCmd Cr« has exceeded the limit set at »Operations Alarm«.)
Res TripCmd Cr	Signal: Resetting of the Counter: Total number of trips of the switchgear
Active	Signal: active
ExBlo	Signal: External Blocking
Blo TripCmd	Signal: Trip Command blocked
ExBlo TripCmd	Signal: External Blocking of the Trip Command
Alarm L1	Signal: Alarm L1
Alarm L2	Signal: Alarm L2
Alarm L3	Signal: Alarm L3
Alarm	Signal: Alarm voltage stage
Trip L1	Signal: General Trip Phase L1
Trip L2	Signal: General Trip Phase L2
Trip L3	Signal: General Trip Phase L3
Trip	Signal: Trip
TripCmd	Signal: Trip Command
ExBlo1-I	Module input state: External blocking1
ExBlo2-I	Module input state: External blocking2
ExBlo TripCmd-I	Module input state: External Blocking of the Trip Command
Active	Signal: active
ExBlo	Signal: External Blocking
Blo TripCmd	Signal: Trip Command blocked
ExBlo TripCmd	Signal: External Blocking of the Trip Command
Alarm L1	Signal: Alarm L1
Alarm L2	Signal: Alarm L2
Alarm L3	Signal: Alarm L3
Alarm	Signal: Alarm voltage stage
Trip L1	Signal: General Trip Phase L1
Trip L2	Signal: General Trip Phase L2
Trip L3	Signal: General Trip Phase L3
Trip	Signal: Trip
TripCmd	Signal: Trip Command
ExBlo1-I	Module input state: External blocking1
ExBlo2-I	Module input state: External blocking2
ExBlo TripCmd-I	Module input state: External Blocking of the Trip Command

1..n, Assignment List	Description
Active	Signal: active
ExBlo	Signal: External Blocking
Blo TripCmd	Signal: Trip Command blocked
ExBlo TripCmd	Signal: External Blocking of the Trip Command
Alarm L1	Signal: Alarm L1
Alarm L2	Signal: Alarm L2
Alarm L3	Signal: Alarm L3
Alarm	Signal: Alarm voltage stage
Trip L1	Signal: General Trip Phase L1
Trip L2	Signal: General Trip Phase L2
Trip L3	Signal: General Trip Phase L3
Trip	Signal: Trip
TripCmd	Signal: Trip Command
ExBlo1-I	Module input state: External blocking1
ExBlo2-I	Module input state: External blocking2
ExBlo TripCmd-I	Module input state: External Blocking of the Trip Command
Active	Signal: active
ExBlo	Signal: External Blocking
Blo TripCmd	Signal: Trip Command blocked
ExBlo TripCmd	Signal: External Blocking of the Trip Command
Alarm L1	Signal: Alarm L1
Alarm L2	Signal: Alarm L2
Alarm L3	Signal: Alarm L3
Alarm	Signal: Alarm voltage stage
Trip L1	Signal: General Trip Phase L1
Trip L2	Signal: General Trip Phase L2
Trip L3	Signal: General Trip Phase L3
Trip	Signal: Trip
TripCmd	Signal: Trip Command
ExBlo1-I	Module input state: External blocking1
ExBlo2-I	Module input state: External blocking2
ExBlo TripCmd-I	Module input state: External Blocking of the Trip Command
Active	Signal: active
ExBlo	Signal: External Blocking
Blo TripCmd	Signal: Trip Command blocked
ExBlo TripCmd	Signal: External Blocking of the Trip Command
Alarm L1	Signal: Alarm L1
Alarm L2	Signal: Alarm L2

1..n, Assignment List	Description
Alarm L3	Signal: Alarm L3
Alarm	Signal: Alarm voltage stage
Trip L1	Signal: General Trip Phase L1
Trip L2	Signal: General Trip Phase L2
Trip L3	Signal: General Trip Phase L3
Trip	Signal: Trip
TripCmd	Signal: Trip Command
ExBlo1-I	Module input state: External blocking1
ExBlo2-I	Module input state: External blocking2
ExBlo TripCmd-I	Module input state: External Blocking of the Trip Command
Active	Signal: active
ExBlo	Signal: External Blocking
Blo TripCmd	Signal: Trip Command blocked
ExBlo TripCmd	Signal: External Blocking of the Trip Command
Alarm L1	Signal: Alarm L1
Alarm L2	Signal: Alarm L2
Alarm L3	Signal: Alarm L3
Alarm	Signal: Alarm voltage stage
Trip L1	Signal: General Trip Phase L1
Trip L2	Signal: General Trip Phase L2
Trip L3	Signal: General Trip Phase L3
Trip	Signal: Trip
TripCmd	Signal: Trip Command
ExBlo1-I	Module input state: External blocking1
ExBlo2-I	Module input state: External blocking2
ExBlo TripCmd-I	Module input state: External Blocking of the Trip Command
Active	Signal: active
ExBlo	Signal: External Blocking
Blo by V<	Signal: Module is blocked by undervoltage.
Blo TripCmd	Signal: Trip Command blocked
ExBlo TripCmd	Signal: External Blocking of the Trip Command
Alarm	Signal: Alarm Frequency Protection (collective signal)
Trip	Signal: Trip Frequency Protection (collective signal)
TripCmd	Signal: Trip Command
ExBlo1-I	Module input state: External blocking1
ExBlo2-I	Module input state: External blocking2
ExBlo TripCmd-I	Module input state: External Blocking of the Trip Command
Active	Signal: active

1..n, Assignment List	Description
ExBlo	Signal: External Blocking
Blo by V<	Signal: Module is blocked by undervoltage.
Blo TripCmd	Signal: Trip Command blocked
ExBlo TripCmd	Signal: External Blocking of the Trip Command
Alarm	Signal: Alarm Frequency Protection (collective signal)
Trip	Signal: Trip Frequency Protection (collective signal)
TripCmd	Signal: Trip Command
ExBlo1-I	Module input state: External blocking1
ExBlo2-I	Module input state: External blocking2
ExBlo TripCmd-I	Module input state: External Blocking of the Trip Command
Active	Signal: active
ExBlo	Signal: External Blocking
Blo TripCmd	Signal: Trip Command blocked
ExBlo TripCmd	Signal: External Blocking of the Trip Command
Alarm	Signal: Alarm
Trip	Signal: Trip
TripCmd	Signal: Trip Command
ExBlo1-I	Module input state: External blocking1
ExBlo2-I	Module input state: External blocking2
ExBlo TripCmd-I	Module input state: External Blocking of the Trip Command
Alarm-I	Module input state: Alarm
Trip-I	Module input state: Trip
Active	Signal: active
ExBlo	Signal: External Blocking
Blo TripCmd	Signal: Trip Command blocked
ExBlo TripCmd	Signal: External Blocking of the Trip Command
Alarm L1	Signal: Alarm L1
Alarm L2	Signal: Alarm L2
Alarm L3	Signal: Alarm L3
Alarm	Signal: Alarm voltage stage
Trip L1	Signal: General Trip Phase L1
Trip L2	Signal: General Trip Phase L2
Trip L3	Signal: General Trip Phase L3
Trip	Signal: Trip
TripCmd	Signal: Trip Command
t-LVRT is running	Signal: t-LVRT is running
ExBlo1-I	Module input state: External blocking1
ExBlo2-I	Module input state: External blocking2

1..n, Assignment List	Description
ExBlo TripCmd-I	Module input state: External Blocking of the Trip Command
Active	Signal: active
ExBlo	Signal: External Blocking
Blo TripCmd	Signal: Trip Command blocked
ExBlo TripCmd	Signal: External Blocking of the Trip Command
Alarm L1	Signal: Alarm L1
Alarm L2	Signal: Alarm L2
Alarm L3	Signal: Alarm L3
Alarm	Signal: Alarm voltage stage
Trip L1	Signal: General Trip Phase L1
Trip L2	Signal: General Trip Phase L2
Trip L3	Signal: General Trip Phase L3
Trip	Signal: Trip
TripCmd	Signal: Trip Command
t-LVRT is running	Signal: t-LVRT is running
ExBlo1-I	Module input state: External blocking1
ExBlo2-I	Module input state: External blocking2
ExBlo TripCmd-I	Module input state: External Blocking of the Trip Command
Active	Signal: active
ExBlo	Signal: External Blocking
Blo TripCmd	Signal: Trip Command blocked
ExBlo TripCmd	Signal: External Blocking of the Trip Command
Alarm	Signal: Alarm Residual Voltage Supervision-stage
Trip	Signal: Trip
TripCmd	Signal: Trip Command
ExBlo1-I	Module input state: External blocking1
ExBlo2-I	Module input state: External blocking2
ExBlo TripCmd-I	Module input state: External Blocking of the Trip Command
Active	Signal: active
ExBlo	Signal: External Blocking
Blo TripCmd	Signal: Trip Command blocked
ExBlo TripCmd	Signal: External Blocking of the Trip Command
Alarm	Signal: Alarm Residual Voltage Supervision-stage
Trip	Signal: Trip
TripCmd	Signal: Trip Command
ExBlo1-I	Module input state: External blocking1
ExBlo2-I	Module input state: External blocking2
ExBlo TripCmd-I	Module input state: External Blocking of the Trip Command

1..n, Assignment List	Description
Active	Signal: active
ExBlo	Signal: External Blocking
Blo TripCmd	Signal: Trip Command blocked
ExBlo TripCmd	Signal: External Blocking of the Trip Command
Alarm	Signal: Alarm voltage asymmetry
Trip	Signal: Trip
TripCmd	Signal: Trip Command
ExBlo1-I	Module input state: External blocking1
ExBlo2-I	Module input state: External blocking2
ExBlo TripCmd-I	Module input state: External Blocking of the Trip Command
Active	Signal: active
ExBlo	Signal: External Blocking
Blo TripCmd	Signal: Trip Command blocked
ExBlo TripCmd	Signal: External Blocking of the Trip Command
Alarm	Signal: Alarm voltage asymmetry
Trip	Signal: Trip
TripCmd	Signal: Trip Command
ExBlo1-I	Module input state: External blocking1
ExBlo2-I	Module input state: External blocking2
ExBlo TripCmd-I	Module input state: External Blocking of the Trip Command
Active	Signal: active
ExBlo	Signal: External Blocking
Blo TripCmd	Signal: Trip Command blocked
ExBlo TripCmd	Signal: External Blocking of the Trip Command
Alarm	Signal: Alarm voltage asymmetry
Trip	Signal: Trip
TripCmd	Signal: Trip Command
ExBlo1-I	Module input state: External blocking1
ExBlo2-I	Module input state: External blocking2
ExBlo TripCmd-I	Module input state: External Blocking of the Trip Command
Active	Signal: active
ExBlo	Signal: External Blocking
Blo TripCmd	Signal: Trip Command blocked
ExBlo TripCmd	Signal: External Blocking of the Trip Command
Alarm	Signal: Alarm voltage asymmetry
Trip	Signal: Trip
TripCmd	Signal: Trip Command
ExBlo1-I	Module input state: External blocking1

1..n, Assignment List	Description
ExBlo2-I	Module input state: External blocking2
ExBlo TripCmd-I	Module input state: External Blocking of the Trip Command
Active	Signal: active
ExBlo	Signal: External Blocking
Blo TripCmd	Signal: Trip Command blocked
ExBlo TripCmd	Signal: External Blocking of the Trip Command
Alarm	Signal: Alarm voltage asymmetry
Trip	Signal: Trip
TripCmd	Signal: Trip Command
ExBlo1-I	Module input state: External blocking1
ExBlo2-I	Module input state: External blocking2
ExBlo TripCmd-I	Module input state: External Blocking of the Trip Command
Active	Signal: active
ExBlo	Signal: External Blocking
Blo TripCmd	Signal: Trip Command blocked
ExBlo TripCmd	Signal: External Blocking of the Trip Command
Alarm	Signal: Alarm voltage asymmetry
Trip	Signal: Trip
TripCmd	Signal: Trip Command
ExBlo1-I	Module input state: External blocking1
ExBlo2-I	Module input state: External blocking2
ExBlo TripCmd-I	Module input state: External Blocking of the Trip Command
Active	Signal: active
ExBlo	Signal: External Blocking
Blo by V<	Signal: Module is blocked by undervoltage.
Blo TripCmd	Signal: Trip Command blocked
ExBlo TripCmd	Signal: External Blocking of the Trip Command
Alarm f	Signal: Alarm Frequency Protection
Alarm df/dt | DF/DT	Alarm instantaneous or average value of the rate-of-frequency-change
Alarm delta phi	Signal: Alarm Vector Surge
Alarm	Signal: Alarm Frequency Protection (collective signal)
Trip f	Signal: Frequency has exceeded the limit.
Trip df/dt | DF/DT	Signal: Trip df/dt or DF/DT
Trip delta phi	Signal: Trip Vector Surge
Trip	Signal: Trip Frequency Protection (collective signal)
TripCmd	Signal: Trip Command
ExBlo1-I	Module input state: External blocking1
ExBlo2-I	Module input state: External blocking2

1..n, Assignment List	Description
ExBlo TripCmd-I	Module input state: External Blocking of the Trip Command
Active	Signal: active
ExBlo	Signal: External Blocking
Blo by V<	Signal: Module is blocked by undervoltage.
Blo TripCmd	Signal: Trip Command blocked
ExBlo TripCmd	Signal: External Blocking of the Trip Command
Alarm f	Signal: Alarm Frequency Protection
Alarm df/dt | DF/DT	Alarm instantaneous or average value of the rate-of-frequency-change
Alarm delta phi	Signal: Alarm Vector Surge
Alarm	Signal: Alarm Frequency Protection (collective signal)
Trip f	Signal: Frequency has exceeded the limit.
Trip df/dt | DF/DT	Signal: Trip df/dt or DF/DT
Trip delta phi	Signal: Trip Vector Surge
Trip	Signal: Trip Frequency Protection (collective signal)
TripCmd	Signal: Trip Command
ExBlo1-I	Module input state: External blocking1
ExBlo2-I	Module input state: External blocking2
ExBlo TripCmd-I	Module input state: External Blocking of the Trip Command
Active	Signal: active
ExBlo	Signal: External Blocking
Blo by V<	Signal: Module is blocked by undervoltage.
Blo TripCmd	Signal: Trip Command blocked
ExBlo TripCmd	Signal: External Blocking of the Trip Command
Alarm f	Signal: Alarm Frequency Protection
Alarm df/dt | DF/DT	Alarm instantaneous or average value of the rate-of-frequency-change
Alarm delta phi	Signal: Alarm Vector Surge
Alarm	Signal: Alarm Frequency Protection (collective signal)
Trip f	Signal: Frequency has exceeded the limit.
Trip df/dt | DF/DT	Signal: Trip df/dt or DF/DT
Trip delta phi	Signal: Trip Vector Surge
Trip	Signal: Trip Frequency Protection (collective signal)
TripCmd	Signal: Trip Command
ExBlo1-I	Module input state: External blocking1
ExBlo2-I	Module input state: External blocking2
ExBlo TripCmd-I	Module input state: External Blocking of the Trip Command
Active	Signal: active
ExBlo	Signal: External Blocking
Blo by V<	Signal: Module is blocked by undervoltage.

1..n, Assignment List	Description
Blo TripCmd	Signal: Trip Command blocked
ExBlo TripCmd	Signal: External Blocking of the Trip Command
Alarm f	Signal: Alarm Frequency Protection
Alarm df/dt | DF/DT	Alarm instantaneous or average value of the rate-of-frequency-change
Alarm delta phi	Signal: Alarm Vector Surge
Alarm	Signal: Alarm Frequency Protection (collective signal)
Trip f	Signal: Frequency has exceeded the limit.
Trip df/dt | DF/DT	Signal: Trip df/dt or DF/DT
Trip delta phi	Signal: Trip Vector Surge
Trip	Signal: Trip Frequency Protection (collective signal)
TripCmd	Signal: Trip Command
ExBlo1-I	Module input state: External blocking1
ExBlo2-I	Module input state: External blocking2
ExBlo TripCmd-I	Module input state: External Blocking of the Trip Command
Active	Signal: active
ExBlo	Signal: External Blocking
Blo by V<	Signal: Module is blocked by undervoltage.
Blo TripCmd	Signal: Trip Command blocked
ExBlo TripCmd	Signal: External Blocking of the Trip Command
Alarm f	Signal: Alarm Frequency Protection
Alarm df/dt | DF/DT	Alarm instantaneous or average value of the rate-of-frequency-change
Alarm delta phi	Signal: Alarm Vector Surge
Alarm	Signal: Alarm Frequency Protection (collective signal)
Trip f	Signal: Frequency has exceeded the limit.
Trip df/dt | DF/DT	Signal: Trip df/dt or DF/DT
Trip delta phi	Signal: Trip Vector Surge
Trip	Signal: Trip Frequency Protection (collective signal)
TripCmd	Signal: Trip Command
ExBlo1-I	Module input state: External blocking1
ExBlo2-I	Module input state: External blocking2
ExBlo TripCmd-I	Module input state: External Blocking of the Trip Command
Active	Signal: active
ExBlo	Signal: External Blocking
Blo by V<	Signal: Module is blocked by undervoltage.
Blo TripCmd	Signal: Trip Command blocked
ExBlo TripCmd	Signal: External Blocking of the Trip Command
Alarm f	Signal: Alarm Frequency Protection
Alarm df/dt | DF/DT	Alarm instantaneous or average value of the rate-of-frequency-change

1..n, Assignment List	Description
Alarm delta phi	Signal: Alarm Vector Surge
Alarm	Signal: Alarm Frequency Protection (collective signal)
Trip f	Signal: Frequency has exceeded the limit.
Trip df/dt | DF/DT	Signal: Trip df/dt or DF/DT
Trip delta phi	Signal: Trip Vector Surge
Trip	Signal: Trip Frequency Protection (collective signal)
TripCmd	Signal: Trip Command
ExBlo1-I	Module input state: External blocking1
ExBlo2-I	Module input state: External blocking2
ExBlo TripCmd-I	Module input state: External Blocking of the Trip Command
Active	Signal: active
ExBlo	Signal: External Blocking
Blo by Meas Circ Superv	Signal: Module blocked by measuring cirucuit supervision
Eval Recon-Conditions	Signal: Evaluation of reconnection conditions after decoupling event
t-Release running	Signal: The timer "t-Release" is running. Thus, all conditions for reconnection are fulfilled. After the timer has expired reconnection release will be issued.
Release Energy Res.	Signal: Signal: Release Energy Resource.
V out of range	Signal: Reconnection release is blocked because voltage is out of range
f out ouf range	Signal: Reconnection release is blocked because frequency is out of range
ExBlo1-I	Module input state: External blocking1
ExBlo2-I	Module input state: External blocking2
V Ext Release PCC-I	Module input state: Release signal is being generated by the PCC (External Release)
PCC Fuse Fail VT-I	State of the module input: Blocking if the fuse of a voltage transformer has tripped at the PCC.
reconnected-I	This signal indicates the state "reconnected" (mains parallel).
Decoupling1-I	Decoupling function, that triggers the reconnection.
Decoupling2-I	Decoupling function, that triggers the reconnection.
Decoupling3-I	Decoupling function, that triggers the reconnection.
Decoupling4-I	Decoupling function, that triggers the reconnection.
Decoupling5-I	Decoupling function, that triggers the reconnection.
Decoupling6-I	Decoupling function, that triggers the reconnection.
Active	Signal: active
ExBlo	Signal: External Blocking
Blo by Meas Circ Superv	Signal: Module blocked by measuring cirucuit supervision
Eval Recon-Conditions	Signal: Evaluation of reconnection conditions after decoupling event
t-Release running	Signal: The timer "t-Release" is running. Thus, all conditions for reconnection are fulfilled. After the timer has expired reconnection release will be issued.
Release Energy Res.	Signal: Signal: Release Energy Resource.
V out of range	Signal: Reconnection release is blocked because voltage is out of range

1..n, Assignment List	Description
f out ouf range	Signal: Reconnection release is blocked because frequency is out of range
ExBlo1-I	Module input state: External blocking1
ExBlo2-I	Module input state: External blocking2
V Ext Release PCC-I	Module input state: Release signal is being generated by the PCC (External Release)
PCC Fuse Fail VT-I	State of the module input: Blocking if the fuse of a voltage transformer has tripped at the PCC.
reconnected-I	This signal indicates the state "reconnected" (mains parallel).
Decoupling1-I	Decoupling function, that triggers the reconnection.
Decoupling2-I	Decoupling function, that triggers the reconnection.
Decoupling3-I	Decoupling function, that triggers the reconnection.
Decoupling4-I	Decoupling function, that triggers the reconnection.
Decoupling5-I	Decoupling function, that triggers the reconnection.
Decoupling6-I	Decoupling function, that triggers the reconnection.
Active	Signal: active
ExBlo	Signal: External Blocking
LiveBus	Signal: Live-Bus flag: 1=Live-Bus, 0=Voltage is below the LiveBus threshold
LiveLine	Signal: Live Line flag: 1=Live-Line, 0=Voltage is below the LiveLine threshold
SynchronRunTiming	Signal: Synchron-Run-timer is timing (This timer starts when Close-Initiate is coming and stops if breaker is closed. Timeout means synchronizing failed.)
SynchronFailed	Signal: This signal indicates a failed synchronization. It is set for 5s when the circuit breaker is still open after the Synchron-Run-timer has timed out.
SyncOverridden	Signal:Synchronism Check is overridden because one of the Synchronism overriding conditions (DB/DL or ExtBypass) is met.
VDiffTooHigh	Signal: Voltage difference between bus and line too high.
SlipTooHigh	Signal: Frequency difference (slip frequency) between bus and line voltages too high.
AngleDiffTooHigh	Signal: Phase Angle difference between bus and line voltages too high.
Sys-in-Sync	Signal: Bus and line voltages are in synchronism according to the system synchronism criteria.
Ready to Close	Signal: Ready to Close
ExBlo1-I	Module input state: External blocking1
ExBlo2-I	Module input state: External blocking2
Bypass-I	State of the module input: The Synchrocheck will be bypassed if the state of the assigned signal (logic input) becomes true.
CBCloseInitiate-I	State of the module input: Breaker Close Initiate with synchronism check from any control sources (e.g. HMI / SCADA). If the state of the assigned signal becomes true, a Breaker Close will be initiated (Trigger Source).
Active	Signal: active
ExBlo	Signal: External Blocking
Blo TripCmd	Signal: Trip Command blocked
ExBlo TripCmd	Signal: External Blocking of the Trip Command
Alarm	Signal: Alarm
Trip	Signal: Trip

1..n, Assignment List	Description
TripCmd	Signal: Trip Command
ExBlo1-I	Module input state: External blocking1
ExBlo2-I	Module input state: External blocking2
ExBlo TripCmd-I	Module input state: External Blocking of the Trip Command
Alarm-I	Module input state: Alarm
Trip-I	Module input state: Trip
Active	Signal: active
ExBlo	Signal: External Blocking
Blo TripCmd	Signal: Trip Command blocked
ExBlo TripCmd	Signal: External Blocking of the Trip Command
Alarm	Signal: Alarm
Trip	Signal: Trip
TripCmd	Signal: Trip Command
ExBlo1-I	Module input state: External blocking1
ExBlo2-I	Module input state: External blocking2
ExBlo TripCmd-I	Module input state: External Blocking of the Trip Command
Alarm-I	Module input state: Alarm
Trip-I	Module input state: Trip
Active	Signal: active
ExBlo	Signal: External Blocking
Blo TripCmd	Signal: Trip Command blocked
ExBlo TripCmd	Signal: External Blocking of the Trip Command
Alarm	Signal: Alarm
Trip	Signal: Trip
TripCmd	Signal: Trip Command
ExBlo1-I	Module input state: External blocking1
ExBlo2-I	Module input state: External blocking2
ExBlo TripCmd-I	Module input state: External Blocking of the Trip Command
Alarm-I	Module input state: Alarm
Trip-I	Module input state: Trip
Active	Signal: active
ExBlo	Signal: External Blocking
Blo TripCmd	Signal: Trip Command blocked
ExBlo TripCmd	Signal: External Blocking of the Trip Command
Alarm	Signal: Alarm
Trip	Signal: Trip
TripCmd	Signal: Trip Command
ExBlo1-I	Module input state: External blocking1

1..n, Assignment List	Description
ExBlo2-I	Module input state: External blocking2
ExBlo TripCmd-I	Module input state: External Blocking of the Trip Command
Alarm-I	Module input state: Alarm
Trip-I	Module input state: Trip
Active	Signal: active
ExBlo	Signal: External Blocking
Waiting for Trigger	Waiting for Trigger
running	Signal: CBF-Module started
Alarm	Signal: Circuit Breaker Failure
Lockout	Signal: Lockout
Res Lockout	Signal: Reset Lockout
ExBlo1-I	Module input state: External blocking1
ExBlo2-I	Module input state: External blocking2
Trigger1-I	Module Input: Trigger that will start the CBF
Trigger2-I	Module Input: Trigger that will start the CBF
Trigger3-I	Module Input: Trigger that will start the CBF
Active	Signal: active
ExBlo	Signal: External Blocking
Alarm	Signal: Alarm Trip Circuit Supervision
Not Possible	Not possible because no state indicator assigned to the breaker.
Aux ON-I	Module Input State: Position indicator/check-back signal of the CB (52a)
Aux OFF-I	Module input state: Position indicator/check-back signal of the CB (52b)
ExBlo1-I	Module input state: External blocking1
ExBlo2-I	Module input state: External blocking2
Active	Signal: active
ExBlo	Signal: External Blocking
Alarm ΔV	Signal: Alarm ΔV Voltage Transformer Measuring Circuit Supervision
Alarm	Signal: Alarm Voltage Transformer Measuring Circuit Supervision
Ex FF VT	Signal: Ex FF VT
Ex FF EVT	Signal: Alarm Fuse Failure Earth Voltage Transformers
Ex Fuse Fail VT-I	Module input state: External fuse failure voltage transformers
Ex Fuse Fail EVT-I	Module input state: External fuse failure earth voltage transformer
ExBlo1-I	Module input state: External blocking1
ExBlo2-I	Module input state: External blocking2
Active	Signal: active
ExBlo	Signal: External Blocking
Alarm V THD	Signal: Alarm Total Harmonic Distortion Voltage
Trip V THD	Signal: Trip Total Harmonic Distortion Voltage

1..n, Assignment List	Description
ExBlo-I	Module input state: External blocking
DI 1	Signal: Digital Input
DI 2	Signal: Digital Input
DI 3	Signal: Digital Input
DI 4	Signal: Digital Input
DI 5	Signal: Digital Input
DI 6	Signal: Digital Input
DI 7	Signal: Digital Input
DI 8	Signal: Digital Input
BO 1	Signal: Binary Output Relay
BO 2	Signal: Binary Output Relay
BO 3	Signal: Binary Output Relay
BO 4	Signal: Binary Output Relay
BO 5	Signal: Binary Output Relay
DISARMED!	Signal: CAUTION! RELAYS DISARMED in order to safely perform maintenance while eliminating the risk of taking an entire process off-line. (Note: The Self Supervision Contact cannot be disarmed). YOU MUST ENSURE that the relays are ARMED AGAIN after maintenance
Outs forced	Signal: The State of at least one Relay Output has been set by force. That means that the state of at least one Relay is forced and hence does not show the state of the assigned signals.
Res all records	Signal: All records are being deleted. (Remark: Immediately afterwards, this signal becomes inactive again.)
recording	Signal: Recording
memory full	Signal: Memory full
Clear fail	Signal: Clear failure in memory
Res all records	Signal: All records are being deleted. (Remark: Immediately afterwards, this signal becomes inactive again.)
Res record	Signal: Delete record
Man Trigger	Signal: Manual Trigger
Start1-I	State of the module input:: Trigger event / start recording
Start2-I	State of the module input:: Trigger event / start recording
Start3-I	State of the module input:: Trigger event / start recording
Start4-I	State of the module input:: Trigger event / start recording
Start5-I	State of the module input:: Trigger event / start recording
Start6-I	State of the module input:: Trigger event / start recording
Start7-I	State of the module input:: Trigger event / start recording
Start8-I	State of the module input:: Trigger event / start recording
Res record	Signal: Delete record
Res all records	Signal: All records are being deleted. (Remark: Immediately afterwards, this signal becomes inactive again.)
System Error	Signal: Device Failure

1..n, Assignment List	Description
New error	Signal: A new error message has been issued.
New warning	Signal: A new warning message has been issued.
Test SC	A drop of SelfSuperVision Contact (SC) has been triggered manually (for testing purposes).
Active	Signal: active
Smart view via USB	Information whether or not the Smart view access via the USB interface is activated (allowed).
Smart view via Eth	Information whether or not the Smart view access via the Ethernet interface is activated (allowed).
SCADA connected	At least one SCADA System is connected to the device.
SCADA not connected	No SCADA System is connected to the device
Uplink A	Uplink A
OpenRingA	Open HSR ring detected on port A. A
Uplink B	Uplink B
OpenRingB	Open HSR ring detected on port A. B
PTP active	PTP active
busy	This message is set if the protocol is started. It will be reset if the protocol is shut down.
ready	The message will be set if the protocol is successfully started and ready for data exchange.
Active	The communication with the Master (SCADA) is active.\nNote that for TCP/UDP, this state is permanently “Low” unless »DataLink confirm« is set to “Always”.
BinaryOutput0	Virtual Digital Output (DNP). This corresponds to a virtual binary input of the protective device.
BinaryOutput1	Virtual Digital Output (DNP). This corresponds to a virtual binary input of the protective device.
BinaryOutput2	Virtual Digital Output (DNP). This corresponds to a virtual binary input of the protective device.
BinaryOutput3	Virtual Digital Output (DNP). This corresponds to a virtual binary input of the protective device.
BinaryOutput4	Virtual Digital Output (DNP). This corresponds to a virtual binary input of the protective device.
BinaryOutput5	Virtual Digital Output (DNP). This corresponds to a virtual binary input of the protective device.
BinaryOutput6	Virtual Digital Output (DNP). This corresponds to a virtual binary input of the protective device.
BinaryOutput7	Virtual Digital Output (DNP). This corresponds to a virtual binary input of the protective device.
BinaryOutput8	Virtual Digital Output (DNP). This corresponds to a virtual binary input of the protective device.
BinaryOutput9	Virtual Digital Output (DNP). This corresponds to a virtual binary input of the protective device.
BinaryOutput10	Virtual Digital Output (DNP). This corresponds to a virtual binary input of the protective device.
BinaryOutput11	Virtual Digital Output (DNP). This corresponds to a virtual binary input of the protective device.

1..n, Assignment List	Description
BinaryOutput12	Virtual Digital Output (DNP). This corresponds to a virtual binary input of the protective device.
BinaryOutput13	Virtual Digital Output (DNP). This corresponds to a virtual binary input of the protective device.
BinaryOutput14	Virtual Digital Output (DNP). This corresponds to a virtual binary input of the protective device.
BinaryOutput15	Virtual Digital Output (DNP). This corresponds to a virtual binary input of the protective device.
BinaryOutput16	Virtual Digital Output (DNP). This corresponds to a virtual binary input of the protective device.
BinaryOutput17	Virtual Digital Output (DNP). This corresponds to a virtual binary input of the protective device.
BinaryOutput18	Virtual Digital Output (DNP). This corresponds to a virtual binary input of the protective device.
BinaryOutput19	Virtual Digital Output (DNP). This corresponds to a virtual binary input of the protective device.
BinaryOutput20	Virtual Digital Output (DNP). This corresponds to a virtual binary input of the protective device.
BinaryOutput21	Virtual Digital Output (DNP). This corresponds to a virtual binary input of the protective device.
BinaryOutput22	Virtual Digital Output (DNP). This corresponds to a virtual binary input of the protective device.
BinaryOutput23	Virtual Digital Output (DNP). This corresponds to a virtual binary input of the protective device.
BinaryOutput24	Virtual Digital Output (DNP). This corresponds to a virtual binary input of the protective device.
BinaryOutput25	Virtual Digital Output (DNP). This corresponds to a virtual binary input of the protective device.
BinaryOutput26	Virtual Digital Output (DNP). This corresponds to a virtual binary input of the protective device.
BinaryOutput27	Virtual Digital Output (DNP). This corresponds to a virtual binary input of the protective device.
BinaryOutput28	Virtual Digital Output (DNP). This corresponds to a virtual binary input of the protective device.
BinaryOutput29	Virtual Digital Output (DNP). This corresponds to a virtual binary input of the protective device.
BinaryOutput30	Virtual Digital Output (DNP). This corresponds to a virtual binary input of the protective device.
BinaryOutput31	Virtual Digital Output (DNP). This corresponds to a virtual binary input of the protective device.
BinaryInput0-I	Virtual Digital Input (DNP). This corresponds to a virtual binary output of the protective device.
BinaryInput1-I	Virtual Digital Input (DNP). This corresponds to a virtual binary output of the protective device.
BinaryInput2-I	Virtual Digital Input (DNP). This corresponds to a virtual binary output of the protective device.
BinaryInput3-I	Virtual Digital Input (DNP). This corresponds to a virtual binary output of the protective device.
BinaryInput4-I	Virtual Digital Input (DNP). This corresponds to a virtual binary output of the protective device.

1..n, Assignment List	Description
BinaryInput5-I	Virtual Digital Input (DNP). This corresponds to a virtual binary output of the protective device.
BinaryInput6-I	Virtual Digital Input (DNP). This corresponds to a virtual binary output of the protective device.
BinaryInput7-I	Virtual Digital Input (DNP). This corresponds to a virtual binary output of the protective device.
BinaryInput8-I	Virtual Digital Input (DNP). This corresponds to a virtual binary output of the protective device.
BinaryInput9-I	Virtual Digital Input (DNP). This corresponds to a virtual binary output of the protective device.
BinaryInput10-I	Virtual Digital Input (DNP). This corresponds to a virtual binary output of the protective device.
BinaryInput11-I	Virtual Digital Input (DNP). This corresponds to a virtual binary output of the protective device.
BinaryInput12-I	Virtual Digital Input (DNP). This corresponds to a virtual binary output of the protective device.
BinaryInput13-I	Virtual Digital Input (DNP). This corresponds to a virtual binary output of the protective device.
BinaryInput14-I	Virtual Digital Input (DNP). This corresponds to a virtual binary output of the protective device.
BinaryInput15-I	Virtual Digital Input (DNP). This corresponds to a virtual binary output of the protective device.
BinaryInput16-I	Virtual Digital Input (DNP). This corresponds to a virtual binary output of the protective device.
BinaryInput17-I	Virtual Digital Input (DNP). This corresponds to a virtual binary output of the protective device.
BinaryInput18-I	Virtual Digital Input (DNP). This corresponds to a virtual binary output of the protective device.
BinaryInput19-I	Virtual Digital Input (DNP). This corresponds to a virtual binary output of the protective device.
BinaryInput20-I	Virtual Digital Input (DNP). This corresponds to a virtual binary output of the protective device.
BinaryInput21-I	Virtual Digital Input (DNP). This corresponds to a virtual binary output of the protective device.
BinaryInput22-I	Virtual Digital Input (DNP). This corresponds to a virtual binary output of the protective device.
BinaryInput23-I	Virtual Digital Input (DNP). This corresponds to a virtual binary output of the protective device.
BinaryInput24-I	Virtual Digital Input (DNP). This corresponds to a virtual binary output of the protective device.
BinaryInput25-I	Virtual Digital Input (DNP). This corresponds to a virtual binary output of the protective device.
BinaryInput26-I	Virtual Digital Input (DNP). This corresponds to a virtual binary output of the protective device.
BinaryInput27-I	Virtual Digital Input (DNP). This corresponds to a virtual binary output of the protective device.
BinaryInput28-I	Virtual Digital Input (DNP). This corresponds to a virtual binary output of the protective device.
BinaryInput29-I	Virtual Digital Input (DNP). This corresponds to a virtual binary output of the protective device.

1..n, Assignment List	Description
BinaryInput30-I	Virtual Digital Input (DNP). This corresponds to a virtual binary output of the protective device.
BinaryInput31-I	Virtual Digital Input (DNP). This corresponds to a virtual binary output of the protective device.
BinaryInput32-I	Virtual Digital Input (DNP). This corresponds to a virtual binary output of the protective device.
BinaryInput33-I	Virtual Digital Input (DNP). This corresponds to a virtual binary output of the protective device.
BinaryInput34-I	Virtual Digital Input (DNP). This corresponds to a virtual binary output of the protective device.
BinaryInput35-I	Virtual Digital Input (DNP). This corresponds to a virtual binary output of the protective device.
BinaryInput36-I	Virtual Digital Input (DNP). This corresponds to a virtual binary output of the protective device.
BinaryInput37-I	Virtual Digital Input (DNP). This corresponds to a virtual binary output of the protective device.
BinaryInput38-I	Virtual Digital Input (DNP). This corresponds to a virtual binary output of the protective device.
BinaryInput39-I	Virtual Digital Input (DNP). This corresponds to a virtual binary output of the protective device.
BinaryInput40-I	Virtual Digital Input (DNP). This corresponds to a virtual binary output of the protective device.
BinaryInput41-I	Virtual Digital Input (DNP). This corresponds to a virtual binary output of the protective device.
BinaryInput42-I	Virtual Digital Input (DNP). This corresponds to a virtual binary output of the protective device.
BinaryInput43-I	Virtual Digital Input (DNP). This corresponds to a virtual binary output of the protective device.
BinaryInput44-I	Virtual Digital Input (DNP). This corresponds to a virtual binary output of the protective device.
BinaryInput45-I	Virtual Digital Input (DNP). This corresponds to a virtual binary output of the protective device.
BinaryInput46-I	Virtual Digital Input (DNP). This corresponds to a virtual binary output of the protective device.
BinaryInput47-I	Virtual Digital Input (DNP). This corresponds to a virtual binary output of the protective device.
BinaryInput48-I	Virtual Digital Input (DNP). This corresponds to a virtual binary output of the protective device.
BinaryInput49-I	Virtual Digital Input (DNP). This corresponds to a virtual binary output of the protective device.
BinaryInput50-I	Virtual Digital Input (DNP). This corresponds to a virtual binary output of the protective device.
BinaryInput51-I	Virtual Digital Input (DNP). This corresponds to a virtual binary output of the protective device.
BinaryInput52-I	Virtual Digital Input (DNP). This corresponds to a virtual binary output of the protective device.
BinaryInput53-I	Virtual Digital Input (DNP). This corresponds to a virtual binary output of the protective device.
BinaryInput54-I	Virtual Digital Input (DNP). This corresponds to a virtual binary output of the protective device.

1..n, Assignment List	Description
BinaryInput55-I	Virtual Digital Input (DNP). This corresponds to a virtual binary output of the protective device.
BinaryInput56-I	Virtual Digital Input (DNP). This corresponds to a virtual binary output of the protective device.
BinaryInput57-I	Virtual Digital Input (DNP). This corresponds to a virtual binary output of the protective device.
BinaryInput58-I	Virtual Digital Input (DNP). This corresponds to a virtual binary output of the protective device.
BinaryInput59-I	Virtual Digital Input (DNP). This corresponds to a virtual binary output of the protective device.
BinaryInput60-I	Virtual Digital Input (DNP). This corresponds to a virtual binary output of the protective device.
BinaryInput61-I	Virtual Digital Input (DNP). This corresponds to a virtual binary output of the protective device.
BinaryInput62-I	Virtual Digital Input (DNP). This corresponds to a virtual binary output of the protective device.
BinaryInput63-I	Virtual Digital Input (DNP). This corresponds to a virtual binary output of the protective device.
Transmission RTU	Signal: SCADA active
Transmission TCP	Signal: SCADA active
Scada Cmd 1	Scada Command
Scada Cmd 2	Scada Command
Scada Cmd 3	Scada Command
Scada Cmd 4	Scada Command
Scada Cmd 5	Scada Command
Scada Cmd 6	Scada Command
Scada Cmd 7	Scada Command
Scada Cmd 8	Scada Command
Scada Cmd 9	Scada Command
Scada Cmd 10	Scada Command
Scada Cmd 11	Scada Command
Scada Cmd 12	Scada Command
Scada Cmd 13	Scada Command
Scada Cmd 14	Scada Command
Scada Cmd 15	Scada Command
Scada Cmd 16	Scada Command
Config Bin Inp1-I	State of the module input: Config Bin Inp
Config Bin Inp2-I	State of the module input: Config Bin Inp
Config Bin Inp3-I	State of the module input: Config Bin Inp
Config Bin Inp4-I	State of the module input: Config Bin Inp
Config Bin Inp5-I	State of the module input: Config Bin Inp
Config Bin Inp6-I	State of the module input: Config Bin Inp

1..n, Assignment List	Description
Config Bin Inp7-I	State of the module input: Config Bin Inp
Config Bin Inp8-I	State of the module input: Config Bin Inp
Config Bin Inp9-I	State of the module input: Config Bin Inp
Config Bin Inp10-I	State of the module input: Config Bin Inp
Config Bin Inp11-I	State of the module input: Config Bin Inp
Config Bin Inp12-I	State of the module input: Config Bin Inp
Config Bin Inp13-I	State of the module input: Config Bin Inp
Config Bin Inp14-I	State of the module input: Config Bin Inp
Config Bin Inp15-I	State of the module input: Config Bin Inp
Config Bin Inp16-I	State of the module input: Config Bin Inp
Config Bin Inp17-I	State of the module input: Config Bin Inp
Config Bin Inp18-I	State of the module input: Config Bin Inp
Config Bin Inp19-I	State of the module input: Config Bin Inp
Config Bin Inp20-I	State of the module input: Config Bin Inp
Config Bin Inp21-I	State of the module input: Config Bin Inp
Config Bin Inp22-I	State of the module input: Config Bin Inp
Config Bin Inp23-I	State of the module input: Config Bin Inp
Config Bin Inp24-I	State of the module input: Config Bin Inp
Config Bin Inp25-I	State of the module input: Config Bin Inp
Config Bin Inp26-I	State of the module input: Config Bin Inp
Config Bin Inp27-I	State of the module input: Config Bin Inp
Config Bin Inp28-I	State of the module input: Config Bin Inp
Config Bin Inp29-I	State of the module input: Config Bin Inp
Config Bin Inp30-I	State of the module input: Config Bin Inp
Config Bin Inp31-I	State of the module input: Config Bin Inp
Config Bin Inp32-I	State of the module input: Config Bin Inp
MMS Client connected	At least one MMS client is connected to the device
All Goose Subscriber active	All Goose subscriber in the device are working
GOSINGGIO1.Ind1.stVal	Signal: Virtual Input (IEC61850 GGIO Ind): State
GOSINGGIO1.Ind2.stVal	Signal: Virtual Input (IEC61850 GGIO Ind): State
GOSINGGIO1.Ind3.stVal	Signal: Virtual Input (IEC61850 GGIO Ind): State
GOSINGGIO1.Ind4.stVal	Signal: Virtual Input (IEC61850 GGIO Ind): State
GOSINGGIO1.Ind5.stVal	Signal: Virtual Input (IEC61850 GGIO Ind): State
GOSINGGIO1.Ind6.stVal	Signal: Virtual Input (IEC61850 GGIO Ind): State
GOSINGGIO1.Ind7.stVal	Signal: Virtual Input (IEC61850 GGIO Ind): State
GOSINGGIO1.Ind8.stVal	Signal: Virtual Input (IEC61850 GGIO Ind): State
GOSINGGIO1.Ind9.stVal	Signal: Virtual Input (IEC61850 GGIO Ind): State
GOSINGGIO1.Ind10.stVal	Signal: Virtual Input (IEC61850 GGIO Ind): State

1..n, Assignment List	Description
GOSINGGIO1.Ind11.stVal	Signal: Virtual Input (IEC61850 GGIO Ind): State
GOSINGGIO1.Ind12.stVal	Signal: Virtual Input (IEC61850 GGIO Ind): State
GOSINGGIO1.Ind13.stVal	Signal: Virtual Input (IEC61850 GGIO Ind): State
GOSINGGIO1.Ind14.stVal	Signal: Virtual Input (IEC61850 GGIO Ind): State
GOSINGGIO1.Ind15.stVal	Signal: Virtual Input (IEC61850 GGIO Ind): State
GOSINGGIO1.Ind16.stVal	Signal: Virtual Input (IEC61850 GGIO Ind): State
GOSINGGIO1.Ind17.stVal	Signal: Virtual Input (IEC61850 GGIO Ind): State
GOSINGGIO1.Ind18.stVal	Signal: Virtual Input (IEC61850 GGIO Ind): State
GOSINGGIO1.Ind19.stVal	Signal: Virtual Input (IEC61850 GGIO Ind): State
GOSINGGIO1.Ind20.stVal	Signal: Virtual Input (IEC61850 GGIO Ind): State
GOSINGGIO1.Ind21.stVal	Signal: Virtual Input (IEC61850 GGIO Ind): State
GOSINGGIO1.Ind22.stVal	Signal: Virtual Input (IEC61850 GGIO Ind): State
GOSINGGIO1.Ind23.stVal	Signal: Virtual Input (IEC61850 GGIO Ind): State
GOSINGGIO1.Ind24.stVal	Signal: Virtual Input (IEC61850 GGIO Ind): State
GOSINGGIO1.Ind25.stVal	Signal: Virtual Input (IEC61850 GGIO Ind): State
GOSINGGIO1.Ind26.stVal	Signal: Virtual Input (IEC61850 GGIO Ind): State
GOSINGGIO1.Ind27.stVal	Signal: Virtual Input (IEC61850 GGIO Ind): State
GOSINGGIO1.Ind28.stVal	Signal: Virtual Input (IEC61850 GGIO Ind): State
GOSINGGIO1.Ind29.stVal	Signal: Virtual Input (IEC61850 GGIO Ind): State
GOSINGGIO1.Ind30.stVal	Signal: Virtual Input (IEC61850 GGIO Ind): State
GOSINGGIO1.Ind31.stVal	Signal: Virtual Input (IEC61850 GGIO Ind): State
GOSINGGIO1.Ind32.stVal	Signal: Virtual Input (IEC61850 GGIO Ind): State
GOSINGGIO2.Ind1.stVal	Signal: Virtual Input (IEC61850 GGIO Ind): State
GOSINGGIO2.Ind2.stVal	Signal: Virtual Input (IEC61850 GGIO Ind): State
GOSINGGIO2.Ind3.stVal	Signal: Virtual Input (IEC61850 GGIO Ind): State
GOSINGGIO2.Ind4.stVal	Signal: Virtual Input (IEC61850 GGIO Ind): State
GOSINGGIO2.Ind5.stVal	Signal: Virtual Input (IEC61850 GGIO Ind): State
GOSINGGIO2.Ind6.stVal	Signal: Virtual Input (IEC61850 GGIO Ind): State
GOSINGGIO2.Ind7.stVal	Signal: Virtual Input (IEC61850 GGIO Ind): State
GOSINGGIO2.Ind8.stVal	Signal: Virtual Input (IEC61850 GGIO Ind): State
GOSINGGIO2.Ind9.stVal	Signal: Virtual Input (IEC61850 GGIO Ind): State
GOSINGGIO2.Ind10.stVal	Signal: Virtual Input (IEC61850 GGIO Ind): State
GOSINGGIO2.Ind11.stVal	Signal: Virtual Input (IEC61850 GGIO Ind): State
GOSINGGIO2.Ind12.stVal	Signal: Virtual Input (IEC61850 GGIO Ind): State
GOSINGGIO2.Ind13.stVal	Signal: Virtual Input (IEC61850 GGIO Ind): State
GOSINGGIO2.Ind14.stVal	Signal: Virtual Input (IEC61850 GGIO Ind): State
GOSINGGIO2.Ind15.stVal	Signal: Virtual Input (IEC61850 GGIO Ind): State
GOSINGGIO2.Ind16.stVal	Signal: Virtual Input (IEC61850 GGIO Ind): State

1..n, Assignment List	Description
GOSINGGIO2.Ind17.stVal	Signal: Virtual Input (IEC61850 GGIO Ind): State
GOSINGGIO2.Ind18.stVal	Signal: Virtual Input (IEC61850 GGIO Ind): State
GOSINGGIO2.Ind19.stVal	Signal: Virtual Input (IEC61850 GGIO Ind): State
GOSINGGIO2.Ind20.stVal	Signal: Virtual Input (IEC61850 GGIO Ind): State
GOSINGGIO2.Ind21.stVal	Signal: Virtual Input (IEC61850 GGIO Ind): State
GOSINGGIO2.Ind22.stVal	Signal: Virtual Input (IEC61850 GGIO Ind): State
GOSINGGIO2.Ind23.stVal	Signal: Virtual Input (IEC61850 GGIO Ind): State
GOSINGGIO2.Ind24.stVal	Signal: Virtual Input (IEC61850 GGIO Ind): State
GOSINGGIO2.Ind25.stVal	Signal: Virtual Input (IEC61850 GGIO Ind): State
GOSINGGIO2.Ind26.stVal	Signal: Virtual Input (IEC61850 GGIO Ind): State
GOSINGGIO2.Ind27.stVal	Signal: Virtual Input (IEC61850 GGIO Ind): State
GOSINGGIO2.Ind28.stVal	Signal: Virtual Input (IEC61850 GGIO Ind): State
GOSINGGIO2.Ind29.stVal	Signal: Virtual Input (IEC61850 GGIO Ind): State
GOSINGGIO2.Ind30.stVal	Signal: Virtual Input (IEC61850 GGIO Ind): State
GOSINGGIO2.Ind31.stVal	Signal: Virtual Input (IEC61850 GGIO Ind): State
GOSINGGIO2.Ind32.stVal	Signal: Virtual Input (IEC61850 GGIO Ind): State
GOSINGGIO1.Ind1.q	Signal: Virtual Input (IEC61850 GGIO Ind): Self-Supervision of the GGIO Input
GOSINGGIO1.Ind2.q	Signal: Virtual Input (IEC61850 GGIO Ind): Self-Supervision of the GGIO Input
GOSINGGIO1.Ind3.q	Signal: Virtual Input (IEC61850 GGIO Ind): Self-Supervision of the GGIO Input
GOSINGGIO1.Ind4.q	Signal: Virtual Input (IEC61850 GGIO Ind): Self-Supervision of the GGIO Input
GOSINGGIO1.Ind5.q	Signal: Virtual Input (IEC61850 GGIO Ind): Self-Supervision of the GGIO Input
GOSINGGIO1.Ind6.q	Signal: Virtual Input (IEC61850 GGIO Ind): Self-Supervision of the GGIO Input
GOSINGGIO1.Ind7.q	Signal: Virtual Input (IEC61850 GGIO Ind): Self-Supervision of the GGIO Input
GOSINGGIO1.Ind8.q	Signal: Virtual Input (IEC61850 GGIO Ind): Self-Supervision of the GGIO Input
GOSINGGIO1.Ind9.q	Signal: Virtual Input (IEC61850 GGIO Ind): Self-Supervision of the GGIO Input
GOSINGGIO1.Ind10.q	Signal: Virtual Input (IEC61850 GGIO Ind): Self-Supervision of the GGIO Input
GOSINGGIO1.Ind11.q	Signal: Virtual Input (IEC61850 GGIO Ind): Self-Supervision of the GGIO Input
GOSINGGIO1.Ind12.q	Signal: Virtual Input (IEC61850 GGIO Ind): Self-Supervision of the GGIO Input
GOSINGGIO1.Ind13.q	Signal: Virtual Input (IEC61850 GGIO Ind): Self-Supervision of the GGIO Input
GOSINGGIO1.Ind14.q	Signal: Virtual Input (IEC61850 GGIO Ind): Self-Supervision of the GGIO Input
GOSINGGIO1.Ind15.q	Signal: Virtual Input (IEC61850 GGIO Ind): Self-Supervision of the GGIO Input
GOSINGGIO1.Ind16.q	Signal: Virtual Input (IEC61850 GGIO Ind): Self-Supervision of the GGIO Input
GOSINGGIO1.Ind17.q	Signal: Virtual Input (IEC61850 GGIO Ind): Self-Supervision of the GGIO Input
GOSINGGIO1.Ind18.q	Signal: Virtual Input (IEC61850 GGIO Ind): Self-Supervision of the GGIO Input
GOSINGGIO1.Ind19.q	Signal: Virtual Input (IEC61850 GGIO Ind): Self-Supervision of the GGIO Input
GOSINGGIO1.Ind20.q	Signal: Virtual Input (IEC61850 GGIO Ind): Self-Supervision of the GGIO Input
GOSINGGIO1.Ind21.q	Signal: Virtual Input (IEC61850 GGIO Ind): Self-Supervision of the GGIO Input
GOSINGGIO1.Ind22.q	Signal: Virtual Input (IEC61850 GGIO Ind): Self-Supervision of the GGIO Input

1..n, Assignment List	Description
GOSINGGIO1.Ind23.q	Signal: Virtual Input (IEC61850 GGIO Ind): Self-Supervision of the GGIO Input
GOSINGGIO1.Ind24.q	Signal: Virtual Input (IEC61850 GGIO Ind): Self-Supervision of the GGIO Input
GOSINGGIO1.Ind25.q	Signal: Virtual Input (IEC61850 GGIO Ind): Self-Supervision of the GGIO Input
GOSINGGIO1.Ind26.q	Signal: Virtual Input (IEC61850 GGIO Ind): Self-Supervision of the GGIO Input
GOSINGGIO1.Ind27.q	Signal: Virtual Input (IEC61850 GGIO Ind): Self-Supervision of the GGIO Input
GOSINGGIO1.Ind28.q	Signal: Virtual Input (IEC61850 GGIO Ind): Self-Supervision of the GGIO Input
GOSINGGIO1.Ind29.q	Signal: Virtual Input (IEC61850 GGIO Ind): Self-Supervision of the GGIO Input
GOSINGGIO1.Ind30.q	Signal: Virtual Input (IEC61850 GGIO Ind): Self-Supervision of the GGIO Input
GOSINGGIO1.Ind31.q	Signal: Virtual Input (IEC61850 GGIO Ind): Self-Supervision of the GGIO Input
GOSINGGIO1.Ind32.q	Signal: Virtual Input (IEC61850 GGIO Ind): Self-Supervision of the GGIO Input
GOSINGGIO2.Ind1.q	Signal: Virtual Input (IEC61850 GGIO Ind): Self-Supervision of the GGIO Input
GOSINGGIO2.Ind2.q	Signal: Virtual Input (IEC61850 GGIO Ind): Self-Supervision of the GGIO Input
GOSINGGIO2.Ind3.q	Signal: Virtual Input (IEC61850 GGIO Ind): Self-Supervision of the GGIO Input
GOSINGGIO2.Ind4.q	Signal: Virtual Input (IEC61850 GGIO Ind): Self-Supervision of the GGIO Input
GOSINGGIO2.Ind5.q	Signal: Virtual Input (IEC61850 GGIO Ind): Self-Supervision of the GGIO Input
GOSINGGIO2.Ind6.q	Signal: Virtual Input (IEC61850 GGIO Ind): Self-Supervision of the GGIO Input
GOSINGGIO2.Ind7.q	Signal: Virtual Input (IEC61850 GGIO Ind): Self-Supervision of the GGIO Input
GOSINGGIO2.Ind8.q	Signal: Virtual Input (IEC61850 GGIO Ind): Self-Supervision of the GGIO Input
GOSINGGIO2.Ind9.q	Signal: Virtual Input (IEC61850 GGIO Ind): Self-Supervision of the GGIO Input
GOSINGGIO2.Ind10.q	Signal: Virtual Input (IEC61850 GGIO Ind): Self-Supervision of the GGIO Input
GOSINGGIO2.Ind11.q	Signal: Virtual Input (IEC61850 GGIO Ind): Self-Supervision of the GGIO Input
GOSINGGIO2.Ind12.q	Signal: Virtual Input (IEC61850 GGIO Ind): Self-Supervision of the GGIO Input
GOSINGGIO2.Ind13.q	Signal: Virtual Input (IEC61850 GGIO Ind): Self-Supervision of the GGIO Input
GOSINGGIO2.Ind14.q	Signal: Virtual Input (IEC61850 GGIO Ind): Self-Supervision of the GGIO Input
GOSINGGIO2.Ind15.q	Signal: Virtual Input (IEC61850 GGIO Ind): Self-Supervision of the GGIO Input
GOSINGGIO2.Ind16.q	Signal: Virtual Input (IEC61850 GGIO Ind): Self-Supervision of the GGIO Input
GOSINGGIO2.Ind17.q	Signal: Virtual Input (IEC61850 GGIO Ind): Self-Supervision of the GGIO Input
GOSINGGIO2.Ind18.q	Signal: Virtual Input (IEC61850 GGIO Ind): Self-Supervision of the GGIO Input
GOSINGGIO2.Ind19.q	Signal: Virtual Input (IEC61850 GGIO Ind): Self-Supervision of the GGIO Input
GOSINGGIO2.Ind20.q	Signal: Virtual Input (IEC61850 GGIO Ind): Self-Supervision of the GGIO Input
GOSINGGIO2.Ind21.q	Signal: Virtual Input (IEC61850 GGIO Ind): Self-Supervision of the GGIO Input
GOSINGGIO2.Ind22.q	Signal: Virtual Input (IEC61850 GGIO Ind): Self-Supervision of the GGIO Input
GOSINGGIO2.Ind23.q	Signal: Virtual Input (IEC61850 GGIO Ind): Self-Supervision of the GGIO Input
GOSINGGIO2.Ind24.q	Signal: Virtual Input (IEC61850 GGIO Ind): Self-Supervision of the GGIO Input
GOSINGGIO2.Ind25.q	Signal: Virtual Input (IEC61850 GGIO Ind): Self-Supervision of the GGIO Input
GOSINGGIO2.Ind26.q	Signal: Virtual Input (IEC61850 GGIO Ind): Self-Supervision of the GGIO Input
GOSINGGIO2.Ind27.q	Signal: Virtual Input (IEC61850 GGIO Ind): Self-Supervision of the GGIO Input
GOSINGGIO2.Ind28.q	Signal: Virtual Input (IEC61850 GGIO Ind): Self-Supervision of the GGIO Input

1..n, Assignment List	Description
GOSINGGIO2.Ind29.q	Signal: Virtual Input (IEC61850 GGIO Ind): Self-Supervision of the GGIO Input
GOSINGGIO2.Ind30.q	Signal: Virtual Input (IEC61850 GGIO Ind): Self-Supervision of the GGIO Input
GOSINGGIO2.Ind31.q	Signal: Virtual Input (IEC61850 GGIO Ind): Self-Supervision of the GGIO Input
GOSINGGIO2.Ind32.q	Signal: Virtual Input (IEC61850 GGIO Ind): Self-Supervision of the GGIO Input
CTLGGIO1.SPCSO1.stVal	Status bit that can be set by clients like e.g. SCADA (Single Point Controllable Status Output).
CTLGGIO1.SPCSO2.stVal	Status bit that can be set by clients like e.g. SCADA (Single Point Controllable Status Output).
CTLGGIO1.SPCSO3.stVal	Status bit that can be set by clients like e.g. SCADA (Single Point Controllable Status Output).
CTLGGIO1.SPCSO4.stVal	Status bit that can be set by clients like e.g. SCADA (Single Point Controllable Status Output).
CTLGGIO1.SPCSO5.stVal	Status bit that can be set by clients like e.g. SCADA (Single Point Controllable Status Output).
CTLGGIO1.SPCSO6.stVal	Status bit that can be set by clients like e.g. SCADA (Single Point Controllable Status Output).
CTLGGIO1.SPCSO7.stVal	Status bit that can be set by clients like e.g. SCADA (Single Point Controllable Status Output).
CTLGGIO1.SPCSO8.stVal	Status bit that can be set by clients like e.g. SCADA (Single Point Controllable Status Output).
CTLGGIO1.SPCSO9.stVal	Status bit that can be set by clients like e.g. SCADA (Single Point Controllable Status Output).
CTLGGIO1.SPCSO10.stVal	Status bit that can be set by clients like e.g. SCADA (Single Point Controllable Status Output).
CTLGGIO1.SPCSO11.stVal	Status bit that can be set by clients like e.g. SCADA (Single Point Controllable Status Output).
CTLGGIO1.SPCSO12.stVal	Status bit that can be set by clients like e.g. SCADA (Single Point Controllable Status Output).
CTLGGIO1.SPCSO13.stVal	Status bit that can be set by clients like e.g. SCADA (Single Point Controllable Status Output).
CTLGGIO1.SPCSO14.stVal	Status bit that can be set by clients like e.g. SCADA (Single Point Controllable Status Output).
CTLGGIO1.SPCSO15.stVal	Status bit that can be set by clients like e.g. SCADA (Single Point Controllable Status Output).
CTLGGIO1.SPCSO16.stVal	Status bit that can be set by clients like e.g. SCADA (Single Point Controllable Status Output).
CTLGGIO1.SPCSO17.stVal	Status bit that can be set by clients like e.g. SCADA (Single Point Controllable Status Output).
CTLGGIO1.SPCSO18.stVal	Status bit that can be set by clients like e.g. SCADA (Single Point Controllable Status Output).
CTLGGIO1.SPCSO19.stVal	Status bit that can be set by clients like e.g. SCADA (Single Point Controllable Status Output).
CTLGGIO1.SPCSO20.stVal	Status bit that can be set by clients like e.g. SCADA (Single Point Controllable Status Output).
CTLGGIO1.SPCSO21.stVal	Status bit that can be set by clients like e.g. SCADA (Single Point Controllable Status Output).
CTLGGIO1.SPCSO22.stVal	Status bit that can be set by clients like e.g. SCADA (Single Point Controllable Status Output).

1..n, Assignment List	Description
CTLGGIO1.SPCSO23.stVal	Status bit that can be set by clients like e.g. SCADA (Single Point Controllable Status Output).
CTLGGIO1.SPCSO24.stVal	Status bit that can be set by clients like e.g. SCADA (Single Point Controllable Status Output).
CTLGGIO1.SPCSO25.stVal	Status bit that can be set by clients like e.g. SCADA (Single Point Controllable Status Output).
CTLGGIO1.SPCSO26.stVal	Status bit that can be set by clients like e.g. SCADA (Single Point Controllable Status Output).
CTLGGIO1.SPCSO27.stVal	Status bit that can be set by clients like e.g. SCADA (Single Point Controllable Status Output).
CTLGGIO1.SPCSO28.stVal	Status bit that can be set by clients like e.g. SCADA (Single Point Controllable Status Output).
CTLGGIO1.SPCSO29.stVal	Status bit that can be set by clients like e.g. SCADA (Single Point Controllable Status Output).
CTLGGIO1.SPCSO30.stVal	Status bit that can be set by clients like e.g. SCADA (Single Point Controllable Status Output).
CTLGGIO1.SPCSO31.stVal	Status bit that can be set by clients like e.g. SCADA (Single Point Controllable Status Output).
CTLGGIO1.SPCSO32.stVal	Status bit that can be set by clients like e.g. SCADA (Single Point Controllable Status Output).
Scada Cmd 1	Scada Command
Scada Cmd 2	Scada Command
Scada Cmd 3	Scada Command
Scada Cmd 4	Scada Command
Scada Cmd 5	Scada Command
Scada Cmd 6	Scada Command
Scada Cmd 7	Scada Command
Scada Cmd 8	Scada Command
Scada Cmd 9	Scada Command
Scada Cmd 10	Scada Command
Transmission	Signal: SCADA active
Failure Event lost	Failure event lost
Test mode active	Signal: IEC103 communication has been switched over into Test Mode.
Block MD active	Signal: The blocking of IEC103 transmission in monitor direction has been activated.
Ex activate test mode-I	Module input state: Test Mode of the IEC103 communication.
Ex activate Block MD-I	Module input state: Activation of the blocking of IEC103 transmission in monitor direction.
busy	This message is set if the protocol is started. It will be reset if the protocol is shut down.
ready	The message will be set if the protocol is successfully started and ready for data exchange.
Transmission	Signal: SCADA active
Failure Event lost	Failure event lost
Scada Cmd 1	Scada Command
Scada Cmd 2	Scada Command

1..n, Assignment List	Description
Scada Cmd 3	Scada Command
Scada Cmd 4	Scada Command
Scada Cmd 5	Scada Command
Scada Cmd 6	Scada Command
Scada Cmd 7	Scada Command
Scada Cmd 8	Scada Command
Scada Cmd 9	Scada Command
Scada Cmd 10	Scada Command
Scada Cmd 11	Scada Command
Scada Cmd 12	Scada Command
Scada Cmd 13	Scada Command
Scada Cmd 14	Scada Command
Scada Cmd 15	Scada Command
Scada Cmd 16	Scada Command
Data OK	Data within the Input field are OK (Yes=1)
SubModul Err	Assignable Signal, Failure in Sub-Module, Communication Failure.
Connection active	Connection active
Scada Cmd 1	Scada Command
Scada Cmd 2	Scada Command
Scada Cmd 3	Scada Command
Scada Cmd 4	Scada Command
Scada Cmd 5	Scada Command
Scada Cmd 6	Scada Command
Scada Cmd 7	Scada Command
Scada Cmd 8	Scada Command
Scada Cmd 9	Scada Command
Scada Cmd 10	Scada Command
Scada Cmd 11	Scada Command
Scada Cmd 12	Scada Command
Scada Cmd 13	Scada Command
Scada Cmd 14	Scada Command
Scada Cmd 15	Scada Command
Scada Cmd 16	Scada Command
IRIG-B active	Signal: If there is no valid IRIG-B signal for 60 sec, IRIG-B is regarded as inactive.
High-Low Invert	Signal: The High and Low signals of the IRIG-B are inverted. This does NOT mean that the wiring is faulty. If the wiring is faulty no IRIG-B signal will be detected.
Control Signal1	Signal: IRIG-B Control Signal. The external IRIG-B generator can set these signals. They can be used for further control procedures inside the device (e.g. logic funtions).

1..n, Assignment List	Description
Control Signal2	Signal: IRIG-B Control Signal. The external IRIG-B generator can set these signals. They can be used for further control procedures inside the device (e.g. logic funtions).
Control Signal3	Signal: IRIG-B Control Signal. The external IRIG-B generator can set these signals. They can be used for further control procedures inside the device (e.g. logic funtions).
Control Signal4	Signal: IRIG-B Control Signal. The external IRIG-B generator can set these signals. They can be used for further control procedures inside the device (e.g. logic funtions).
Control Signal5	Signal: IRIG-B Control Signal. The external IRIG-B generator can set these signals. They can be used for further control procedures inside the device (e.g. logic funtions).
Control Signal6	Signal: IRIG-B Control Signal. The external IRIG-B generator can set these signals. They can be used for further control procedures inside the device (e.g. logic funtions).
Control Signal7	Signal: IRIG-B Control Signal. The external IRIG-B generator can set these signals. They can be used for further control procedures inside the device (e.g. logic funtions).
Control Signal8	Signal: IRIG-B Control Signal. The external IRIG-B generator can set these signals. They can be used for further control procedures inside the device (e.g. logic funtions).
Control Signal9	Signal: IRIG-B Control Signal. The external IRIG-B generator can set these signals. They can be used for further control procedures inside the device (e.g. logic funtions).
Control Signal10	Signal: IRIG-B Control Signal. The external IRIG-B generator can set these signals. They can be used for further control procedures inside the device (e.g. logic funtions).
Control Signal11	Signal: IRIG-B Control Signal. The external IRIG-B generator can set these signals. They can be used for further control procedures inside the device (e.g. logic funtions).
Control Signal12	Signal: IRIG-B Control Signal. The external IRIG-B generator can set these signals. They can be used for further control procedures inside the device (e.g. logic funtions).
Control Signal13	Signal: IRIG-B Control Signal. The external IRIG-B generator can set these signals. They can be used for further control procedures inside the device (e.g. logic funtions).
Control Signal14	Signal: IRIG-B Control Signal. The external IRIG-B generator can set these signals. They can be used for further control procedures inside the device (e.g. logic funtions).
Control Signal15	Signal: IRIG-B Control Signal. The external IRIG-B generator can set these signals. They can be used for further control procedures inside the device (e.g. logic funtions).
Control Signal16	Signal: IRIG-B Control Signal. The external IRIG-B generator can set these signals. They can be used for further control procedures inside the device (e.g. logic funtions).
Control Signal17	Signal: IRIG-B Control Signal. The external IRIG-B generator can set these signals. They can be used for further control procedures inside the device (e.g. logic funtions).
Control Signal18	Signal: IRIG-B Control Signal. The external IRIG-B generator can set these signals. They can be used for further control procedures inside the device (e.g. logic funtions).
SNTP active	Signal: If there is no valid SNTP signal for 120 sec, SNTP is regarded as inactive.
synchronized	Clock is synchronized.
ResFc all	Signal: Resetting of all Statistic values (Current Demand, Power Demand, Min, Max)
ResFc Vavg	Signal: Resetting of the sliding average calculation.
ResFc Max	Signal: Resetting of all Maximum values
ResFc Min	Signal: Resetting of all Minimum values
StartFc Vavg-I	State of the module input: Start of Statistics Average Voltage
LE1.Gate Out	Signal: Output of the logic gate
LE1.Timer Out	Signal: Timer Output
LE1.Out	Signal: Latched Output (Q)
LE1.Out inverted	Signal: Negated Latched Output (Q NOT)
LE1.Gate In1-I	State of the module input: Assignment of the Input Signal

1..n, Assignment List	Description
LE1.Gate In2-I	State of the module input: Assignment of the Input Signal
LE1.Gate In3-I	State of the module input: Assignment of the Input Signal
LE1.Gate In4-I	State of the module input: Assignment of the Input Signal
LE1.Reset Latch-I	State of the module input: Reset Signal for the Latching
LE2.Gate Out	Signal: Output of the logic gate
LE2.Timer Out	Signal: Timer Output
LE2.Out	Signal: Latched Output (Q)
LE2.Out inverted	Signal: Negated Latched Output (Q NOT)
LE2.Gate In1-I	State of the module input: Assignment of the Input Signal
LE2.Gate In2-I	State of the module input: Assignment of the Input Signal
LE2.Gate In3-I	State of the module input: Assignment of the Input Signal
LE2.Gate In4-I	State of the module input: Assignment of the Input Signal
LE2.Reset Latch-I	State of the module input: Reset Signal for the Latching
LE3.Gate Out	Signal: Output of the logic gate
LE3.Timer Out	Signal: Timer Output
LE3.Out	Signal: Latched Output (Q)
LE3.Out inverted	Signal: Negated Latched Output (Q NOT)
LE3.Gate In1-I	State of the module input: Assignment of the Input Signal
LE3.Gate In2-I	State of the module input: Assignment of the Input Signal
LE3.Gate In3-I	State of the module input: Assignment of the Input Signal
LE3.Gate In4-I	State of the module input: Assignment of the Input Signal
LE3.Reset Latch-I	State of the module input: Reset Signal for the Latching
LE4.Gate Out	Signal: Output of the logic gate
LE4.Timer Out	Signal: Timer Output
LE4.Out	Signal: Latched Output (Q)
LE4.Out inverted	Signal: Negated Latched Output (Q NOT)
LE4.Gate In1-I	State of the module input: Assignment of the Input Signal
LE4.Gate In2-I	State of the module input: Assignment of the Input Signal
LE4.Gate In3-I	State of the module input: Assignment of the Input Signal
LE4.Gate In4-I	State of the module input: Assignment of the Input Signal
LE4.Reset Latch-I	State of the module input: Reset Signal for the Latching
LE5.Gate Out	Signal: Output of the logic gate
LE5.Timer Out	Signal: Timer Output
LE5.Out	Signal: Latched Output (Q)
LE5.Out inverted	Signal: Negated Latched Output (Q NOT)
LE5.Gate In1-I	State of the module input: Assignment of the Input Signal
LE5.Gate In2-I	State of the module input: Assignment of the Input Signal
LE5.Gate In3-I	State of the module input: Assignment of the Input Signal

1..n, Assignment List	Description
LE5.Gate In4-I	State of the module input: Assignment of the Input Signal
LE5.Reset Latch-I	State of the module input: Reset Signal for the Latching
LE6.Gate Out	Signal: Output of the logic gate
LE6.Timer Out	Signal: Timer Output
LE6.Out	Signal: Latched Output (Q)
LE6.Out inverted	Signal: Negated Latched Output (Q NOT)
LE6.Gate In1-I	State of the module input: Assignment of the Input Signal
LE6.Gate In2-I	State of the module input: Assignment of the Input Signal
LE6.Gate In3-I	State of the module input: Assignment of the Input Signal
LE6.Gate In4-I	State of the module input: Assignment of the Input Signal
LE6.Reset Latch-I	State of the module input: Reset Signal for the Latching
LE7.Gate Out	Signal: Output of the logic gate
LE7.Timer Out	Signal: Timer Output
LE7.Out	Signal: Latched Output (Q)
LE7.Out inverted	Signal: Negated Latched Output (Q NOT)
LE7.Gate In1-I	State of the module input: Assignment of the Input Signal
LE7.Gate In2-I	State of the module input: Assignment of the Input Signal
LE7.Gate In3-I	State of the module input: Assignment of the Input Signal
LE7.Gate In4-I	State of the module input: Assignment of the Input Signal
LE7.Reset Latch-I	State of the module input: Reset Signal for the Latching
LE8.Gate Out	Signal: Output of the logic gate
LE8.Timer Out	Signal: Timer Output
LE8.Out	Signal: Latched Output (Q)
LE8.Out inverted	Signal: Negated Latched Output (Q NOT)
LE8.Gate In1-I	State of the module input: Assignment of the Input Signal
LE8.Gate In2-I	State of the module input: Assignment of the Input Signal
LE8.Gate In3-I	State of the module input: Assignment of the Input Signal
LE8.Gate In4-I	State of the module input: Assignment of the Input Signal
LE8.Reset Latch-I	State of the module input: Reset Signal for the Latching
LE9.Gate Out	Signal: Output of the logic gate
LE9.Timer Out	Signal: Timer Output
LE9.Out	Signal: Latched Output (Q)
LE9.Out inverted	Signal: Negated Latched Output (Q NOT)
LE9.Gate In1-I	State of the module input: Assignment of the Input Signal
LE9.Gate In2-I	State of the module input: Assignment of the Input Signal
LE9.Gate In3-I	State of the module input: Assignment of the Input Signal
LE9.Gate In4-I	State of the module input: Assignment of the Input Signal
LE9.Reset Latch-I	State of the module input: Reset Signal for the Latching

1..n, Assignment List	Description
LE10.Gate Out	Signal: Output of the logic gate
LE10.Timer Out	Signal: Timer Output
LE10.Out	Signal: Latched Output (Q)
LE10.Out inverted	Signal: Negated Latched Output (Q NOT)
LE10.Gate In1-I	State of the module input: Assignment of the Input Signal
LE10.Gate In2-I	State of the module input: Assignment of the Input Signal
LE10.Gate In3-I	State of the module input: Assignment of the Input Signal
LE10.Gate In4-I	State of the module input: Assignment of the Input Signal
LE10.Reset Latch-I	State of the module input: Reset Signal for the Latching
LE11.Gate Out	Signal: Output of the logic gate
LE11.Timer Out	Signal: Timer Output
LE11.Out	Signal: Latched Output (Q)
LE11.Out inverted	Signal: Negated Latched Output (Q NOT)
LE11.Gate In1-I	State of the module input: Assignment of the Input Signal
LE11.Gate In2-I	State of the module input: Assignment of the Input Signal
LE11.Gate In3-I	State of the module input: Assignment of the Input Signal
LE11.Gate In4-I	State of the module input: Assignment of the Input Signal
LE11.Reset Latch-I	State of the module input: Reset Signal for the Latching
LE12.Gate Out	Signal: Output of the logic gate
LE12.Timer Out	Signal: Timer Output
LE12.Out	Signal: Latched Output (Q)
LE12.Out inverted	Signal: Negated Latched Output (Q NOT)
LE12.Gate In1-I	State of the module input: Assignment of the Input Signal
LE12.Gate In2-I	State of the module input: Assignment of the Input Signal
LE12.Gate In3-I	State of the module input: Assignment of the Input Signal
LE12.Gate In4-I	State of the module input: Assignment of the Input Signal
LE12.Reset Latch-I	State of the module input: Reset Signal for the Latching
LE13.Gate Out	Signal: Output of the logic gate
LE13.Timer Out	Signal: Timer Output
LE13.Out	Signal: Latched Output (Q)
LE13.Out inverted	Signal: Negated Latched Output (Q NOT)
LE13.Gate In1-I	State of the module input: Assignment of the Input Signal
LE13.Gate In2-I	State of the module input: Assignment of the Input Signal
LE13.Gate In3-I	State of the module input: Assignment of the Input Signal
LE13.Gate In4-I	State of the module input: Assignment of the Input Signal
LE13.Reset Latch-I	State of the module input: Reset Signal for the Latching
LE14.Gate Out	Signal: Output of the logic gate
LE14.Timer Out	Signal: Timer Output

1..n, Assignment List	Description
LE14.Out	Signal: Latched Output (Q)
LE14.Out inverted	Signal: Negated Latched Output (Q NOT)
LE14.Gate In1-I	State of the module input: Assignment of the Input Signal
LE14.Gate In2-I	State of the module input: Assignment of the Input Signal
LE14.Gate In3-I	State of the module input: Assignment of the Input Signal
LE14.Gate In4-I	State of the module input: Assignment of the Input Signal
LE14.Reset Latch-I	State of the module input: Reset Signal for the Latching
LE15.Gate Out	Signal: Output of the logic gate
LE15.Timer Out	Signal: Timer Output
LE15.Out	Signal: Latched Output (Q)
LE15.Out inverted	Signal: Negated Latched Output (Q NOT)
LE15.Gate In1-I	State of the module input: Assignment of the Input Signal
LE15.Gate In2-I	State of the module input: Assignment of the Input Signal
LE15.Gate In3-I	State of the module input: Assignment of the Input Signal
LE15.Gate In4-I	State of the module input: Assignment of the Input Signal
LE15.Reset Latch-I	State of the module input: Reset Signal for the Latching
LE16.Gate Out	Signal: Output of the logic gate
LE16.Timer Out	Signal: Timer Output
LE16.Out	Signal: Latched Output (Q)
LE16.Out inverted	Signal: Negated Latched Output (Q NOT)
LE16.Gate In1-I	State of the module input: Assignment of the Input Signal
LE16.Gate In2-I	State of the module input: Assignment of the Input Signal
LE16.Gate In3-I	State of the module input: Assignment of the Input Signal
LE16.Gate In4-I	State of the module input: Assignment of the Input Signal
LE16.Reset Latch-I	State of the module input: Reset Signal for the Latching
LE17.Gate Out	Signal: Output of the logic gate
LE17.Timer Out	Signal: Timer Output
LE17.Out	Signal: Latched Output (Q)
LE17.Out inverted	Signal: Negated Latched Output (Q NOT)
LE17.Gate In1-I	State of the module input: Assignment of the Input Signal
LE17.Gate In2-I	State of the module input: Assignment of the Input Signal
LE17.Gate In3-I	State of the module input: Assignment of the Input Signal
LE17.Gate In4-I	State of the module input: Assignment of the Input Signal
LE17.Reset Latch-I	State of the module input: Reset Signal for the Latching
LE18.Gate Out	Signal: Output of the logic gate
LE18.Timer Out	Signal: Timer Output
LE18.Out	Signal: Latched Output (Q)
LE18.Out inverted	Signal: Negated Latched Output (Q NOT)

1..n, Assignment List	Description
LE18.Gate In1-I	State of the module input: Assignment of the Input Signal
LE18.Gate In2-I	State of the module input: Assignment of the Input Signal
LE18.Gate In3-I	State of the module input: Assignment of the Input Signal
LE18.Gate In4-I	State of the module input: Assignment of the Input Signal
LE18.Reset Latch-I	State of the module input: Reset Signal for the Latching
LE19.Gate Out	Signal: Output of the logic gate
LE19.Timer Out	Signal: Timer Output
LE19.Out	Signal: Latched Output (Q)
LE19.Out inverted	Signal: Negated Latched Output (Q NOT)
LE19.Gate In1-I	State of the module input: Assignment of the Input Signal
LE19.Gate In2-I	State of the module input: Assignment of the Input Signal
LE19.Gate In3-I	State of the module input: Assignment of the Input Signal
LE19.Gate In4-I	State of the module input: Assignment of the Input Signal
LE19.Reset Latch-I	State of the module input: Reset Signal for the Latching
LE20.Gate Out	Signal: Output of the logic gate
LE20.Timer Out	Signal: Timer Output
LE20.Out	Signal: Latched Output (Q)
LE20.Out inverted	Signal: Negated Latched Output (Q NOT)
LE20.Gate In1-I	State of the module input: Assignment of the Input Signal
LE20.Gate In2-I	State of the module input: Assignment of the Input Signal
LE20.Gate In3-I	State of the module input: Assignment of the Input Signal
LE20.Gate In4-I	State of the module input: Assignment of the Input Signal
LE20.Reset Latch-I	State of the module input: Reset Signal for the Latching
LE21.Gate Out	Signal: Output of the logic gate
LE21.Timer Out	Signal: Timer Output
LE21.Out	Signal: Latched Output (Q)
LE21.Out inverted	Signal: Negated Latched Output (Q NOT)
LE21.Gate In1-I	State of the module input: Assignment of the Input Signal
LE21.Gate In2-I	State of the module input: Assignment of the Input Signal
LE21.Gate In3-I	State of the module input: Assignment of the Input Signal
LE21.Gate In4-I	State of the module input: Assignment of the Input Signal
LE21.Reset Latch-I	State of the module input: Reset Signal for the Latching
LE22.Gate Out	Signal: Output of the logic gate
LE22.Timer Out	Signal: Timer Output
LE22.Out	Signal: Latched Output (Q)
LE22.Out inverted	Signal: Negated Latched Output (Q NOT)
LE22.Gate In1-I	State of the module input: Assignment of the Input Signal
LE22.Gate In2-I	State of the module input: Assignment of the Input Signal

1..n, Assignment List	Description
LE22.Gate In3-I	State of the module input: Assignment of the Input Signal
LE22.Gate In4-I	State of the module input: Assignment of the Input Signal
LE22.Reset Latch-I	State of the module input: Reset Signal for the Latching
LE23.Gate Out	Signal: Output of the logic gate
LE23.Timer Out	Signal: Timer Output
LE23.Out	Signal: Latched Output (Q)
LE23.Out inverted	Signal: Negated Latched Output (Q NOT)
LE23.Gate In1-I	State of the module input: Assignment of the Input Signal
LE23.Gate In2-I	State of the module input: Assignment of the Input Signal
LE23.Gate In3-I	State of the module input: Assignment of the Input Signal
LE23.Gate In4-I	State of the module input: Assignment of the Input Signal
LE23.Reset Latch-I	State of the module input: Reset Signal for the Latching
LE24.Gate Out	Signal: Output of the logic gate
LE24.Timer Out	Signal: Timer Output
LE24.Out	Signal: Latched Output (Q)
LE24.Out inverted	Signal: Negated Latched Output (Q NOT)
LE24.Gate In1-I	State of the module input: Assignment of the Input Signal
LE24.Gate In2-I	State of the module input: Assignment of the Input Signal
LE24.Gate In3-I	State of the module input: Assignment of the Input Signal
LE24.Gate In4-I	State of the module input: Assignment of the Input Signal
LE24.Reset Latch-I	State of the module input: Reset Signal for the Latching
LE25.Gate Out	Signal: Output of the logic gate
LE25.Timer Out	Signal: Timer Output
LE25.Out	Signal: Latched Output (Q)
LE25.Out inverted	Signal: Negated Latched Output (Q NOT)
LE25.Gate In1-I	State of the module input: Assignment of the Input Signal
LE25.Gate In2-I	State of the module input: Assignment of the Input Signal
LE25.Gate In3-I	State of the module input: Assignment of the Input Signal
LE25.Gate In4-I	State of the module input: Assignment of the Input Signal
LE25.Reset Latch-I	State of the module input: Reset Signal for the Latching
LE26.Gate Out	Signal: Output of the logic gate
LE26.Timer Out	Signal: Timer Output
LE26.Out	Signal: Latched Output (Q)
LE26.Out inverted	Signal: Negated Latched Output (Q NOT)
LE26.Gate In1-I	State of the module input: Assignment of the Input Signal
LE26.Gate In2-I	State of the module input: Assignment of the Input Signal
LE26.Gate In3-I	State of the module input: Assignment of the Input Signal
LE26.Gate In4-I	State of the module input: Assignment of the Input Signal

1..n, Assignment List	Description
LE26.Reset Latch-I	State of the module input: Reset Signal for the Latching
LE27.Gate Out	Signal: Output of the logic gate
LE27.Timer Out	Signal: Timer Output
LE27.Out	Signal: Latched Output (Q)
LE27.Out inverted	Signal: Negated Latched Output (Q NOT)
LE27.Gate In1-I	State of the module input: Assignment of the Input Signal
LE27.Gate In2-I	State of the module input: Assignment of the Input Signal
LE27.Gate In3-I	State of the module input: Assignment of the Input Signal
LE27.Gate In4-I	State of the module input: Assignment of the Input Signal
LE27.Reset Latch-I	State of the module input: Reset Signal for the Latching
LE28.Gate Out	Signal: Output of the logic gate
LE28.Timer Out	Signal: Timer Output
LE28.Out	Signal: Latched Output (Q)
LE28.Out inverted	Signal: Negated Latched Output (Q NOT)
LE28.Gate In1-I	State of the module input: Assignment of the Input Signal
LE28.Gate In2-I	State of the module input: Assignment of the Input Signal
LE28.Gate In3-I	State of the module input: Assignment of the Input Signal
LE28.Gate In4-I	State of the module input: Assignment of the Input Signal
LE28.Reset Latch-I	State of the module input: Reset Signal for the Latching
LE29.Gate Out	Signal: Output of the logic gate
LE29.Timer Out	Signal: Timer Output
LE29.Out	Signal: Latched Output (Q)
LE29.Out inverted	Signal: Negated Latched Output (Q NOT)
LE29.Gate In1-I	State of the module input: Assignment of the Input Signal
LE29.Gate In2-I	State of the module input: Assignment of the Input Signal
LE29.Gate In3-I	State of the module input: Assignment of the Input Signal
LE29.Gate In4-I	State of the module input: Assignment of the Input Signal
LE29.Reset Latch-I	State of the module input: Reset Signal for the Latching
LE30.Gate Out	Signal: Output of the logic gate
LE30.Timer Out	Signal: Timer Output
LE30.Out	Signal: Latched Output (Q)
LE30.Out inverted	Signal: Negated Latched Output (Q NOT)
LE30.Gate In1-I	State of the module input: Assignment of the Input Signal
LE30.Gate In2-I	State of the module input: Assignment of the Input Signal
LE30.Gate In3-I	State of the module input: Assignment of the Input Signal
LE30.Gate In4-I	State of the module input: Assignment of the Input Signal
LE30.Reset Latch-I	State of the module input: Reset Signal for the Latching
LE31.Gate Out	Signal: Output of the logic gate

1..n, Assignment List	Description
LE31.Timer Out	Signal: Timer Output
LE31.Out	Signal: Latched Output (Q)
LE31.Out inverted	Signal: Negated Latched Output (Q NOT)
LE31.Gate In1-I	State of the module input: Assignment of the Input Signal
LE31.Gate In2-I	State of the module input: Assignment of the Input Signal
LE31.Gate In3-I	State of the module input: Assignment of the Input Signal
LE31.Gate In4-I	State of the module input: Assignment of the Input Signal
LE31.Reset Latch-I	State of the module input: Reset Signal for the Latching
LE32.Gate Out	Signal: Output of the logic gate
LE32.Timer Out	Signal: Timer Output
LE32.Out	Signal: Latched Output (Q)
LE32.Out inverted	Signal: Negated Latched Output (Q NOT)
LE32.Gate In1-I	State of the module input: Assignment of the Input Signal
LE32.Gate In2-I	State of the module input: Assignment of the Input Signal
LE32.Gate In3-I	State of the module input: Assignment of the Input Signal
LE32.Gate In4-I	State of the module input: Assignment of the Input Signal
LE32.Reset Latch-I	State of the module input: Reset Signal for the Latching
LE33.Gate Out	Signal: Output of the logic gate
LE33.Timer Out	Signal: Timer Output
LE33.Out	Signal: Latched Output (Q)
LE33.Out inverted	Signal: Negated Latched Output (Q NOT)
LE33.Gate In1-I	State of the module input: Assignment of the Input Signal
LE33.Gate In2-I	State of the module input: Assignment of the Input Signal
LE33.Gate In3-I	State of the module input: Assignment of the Input Signal
LE33.Gate In4-I	State of the module input: Assignment of the Input Signal
LE33.Reset Latch-I	State of the module input: Reset Signal for the Latching
LE34.Gate Out	Signal: Output of the logic gate
LE34.Timer Out	Signal: Timer Output
LE34.Out	Signal: Latched Output (Q)
LE34.Out inverted	Signal: Negated Latched Output (Q NOT)
LE34.Gate In1-I	State of the module input: Assignment of the Input Signal
LE34.Gate In2-I	State of the module input: Assignment of the Input Signal
LE34.Gate In3-I	State of the module input: Assignment of the Input Signal
LE34.Gate In4-I	State of the module input: Assignment of the Input Signal
LE34.Reset Latch-I	State of the module input: Reset Signal for the Latching
LE35.Gate Out	Signal: Output of the logic gate
LE35.Timer Out	Signal: Timer Output
LE35.Out	Signal: Latched Output (Q)

1..n, Assignment List	Description
LE35.Out inverted	Signal: Negated Latched Output (Q NOT)
LE35.Gate In1-I	State of the module input: Assignment of the Input Signal
LE35.Gate In2-I	State of the module input: Assignment of the Input Signal
LE35.Gate In3-I	State of the module input: Assignment of the Input Signal
LE35.Gate In4-I	State of the module input: Assignment of the Input Signal
LE35.Reset Latch-I	State of the module input: Reset Signal for the Latching
LE36.Gate Out	Signal: Output of the logic gate
LE36.Timer Out	Signal: Timer Output
LE36.Out	Signal: Latched Output (Q)
LE36.Out inverted	Signal: Negated Latched Output (Q NOT)
LE36.Gate In1-I	State of the module input: Assignment of the Input Signal
LE36.Gate In2-I	State of the module input: Assignment of the Input Signal
LE36.Gate In3-I	State of the module input: Assignment of the Input Signal
LE36.Gate In4-I	State of the module input: Assignment of the Input Signal
LE36.Reset Latch-I	State of the module input: Reset Signal for the Latching
LE37.Gate Out	Signal: Output of the logic gate
LE37.Timer Out	Signal: Timer Output
LE37.Out	Signal: Latched Output (Q)
LE37.Out inverted	Signal: Negated Latched Output (Q NOT)
LE37.Gate In1-I	State of the module input: Assignment of the Input Signal
LE37.Gate In2-I	State of the module input: Assignment of the Input Signal
LE37.Gate In3-I	State of the module input: Assignment of the Input Signal
LE37.Gate In4-I	State of the module input: Assignment of the Input Signal
LE37.Reset Latch-I	State of the module input: Reset Signal for the Latching
LE38.Gate Out	Signal: Output of the logic gate
LE38.Timer Out	Signal: Timer Output
LE38.Out	Signal: Latched Output (Q)
LE38.Out inverted	Signal: Negated Latched Output (Q NOT)
LE38.Gate In1-I	State of the module input: Assignment of the Input Signal
LE38.Gate In2-I	State of the module input: Assignment of the Input Signal
LE38.Gate In3-I	State of the module input: Assignment of the Input Signal
LE38.Gate In4-I	State of the module input: Assignment of the Input Signal
LE38.Reset Latch-I	State of the module input: Reset Signal for the Latching
LE39.Gate Out	Signal: Output of the logic gate
LE39.Timer Out	Signal: Timer Output
LE39.Out	Signal: Latched Output (Q)
LE39.Out inverted	Signal: Negated Latched Output (Q NOT)
LE39.Gate In1-I	State of the module input: Assignment of the Input Signal

1..n, Assignment List	Description
LE39.Gate In2-I	State of the module input: Assignment of the Input Signal
LE39.Gate In3-I	State of the module input: Assignment of the Input Signal
LE39.Gate In4-I	State of the module input: Assignment of the Input Signal
LE39.Reset Latch-I	State of the module input: Reset Signal for the Latching
LE40.Gate Out	Signal: Output of the logic gate
LE40.Timer Out	Signal: Timer Output
LE40.Out	Signal: Latched Output (Q)
LE40.Out inverted	Signal: Negated Latched Output (Q NOT)
LE40.Gate In1-I	State of the module input: Assignment of the Input Signal
LE40.Gate In2-I	State of the module input: Assignment of the Input Signal
LE40.Gate In3-I	State of the module input: Assignment of the Input Signal
LE40.Gate In4-I	State of the module input: Assignment of the Input Signal
LE40.Reset Latch-I	State of the module input: Reset Signal for the Latching
LE41.Gate Out	Signal: Output of the logic gate
LE41.Timer Out	Signal: Timer Output
LE41.Out	Signal: Latched Output (Q)
LE41.Out inverted	Signal: Negated Latched Output (Q NOT)
LE41.Gate In1-I	State of the module input: Assignment of the Input Signal
LE41.Gate In2-I	State of the module input: Assignment of the Input Signal
LE41.Gate In3-I	State of the module input: Assignment of the Input Signal
LE41.Gate In4-I	State of the module input: Assignment of the Input Signal
LE41.Reset Latch-I	State of the module input: Reset Signal for the Latching
LE42.Gate Out	Signal: Output of the logic gate
LE42.Timer Out	Signal: Timer Output
LE42.Out	Signal: Latched Output (Q)
LE42.Out inverted	Signal: Negated Latched Output (Q NOT)
LE42.Gate In1-I	State of the module input: Assignment of the Input Signal
LE42.Gate In2-I	State of the module input: Assignment of the Input Signal
LE42.Gate In3-I	State of the module input: Assignment of the Input Signal
LE42.Gate In4-I	State of the module input: Assignment of the Input Signal
LE42.Reset Latch-I	State of the module input: Reset Signal for the Latching
LE43.Gate Out	Signal: Output of the logic gate
LE43.Timer Out	Signal: Timer Output
LE43.Out	Signal: Latched Output (Q)
LE43.Out inverted	Signal: Negated Latched Output (Q NOT)
LE43.Gate In1-I	State of the module input: Assignment of the Input Signal
LE43.Gate In2-I	State of the module input: Assignment of the Input Signal
LE43.Gate In3-I	State of the module input: Assignment of the Input Signal

1..n, Assignment List	Description
LE43.Gate In4-I	State of the module input: Assignment of the Input Signal
LE43.Reset Latch-I	State of the module input: Reset Signal for the Latching
LE44.Gate Out	Signal: Output of the logic gate
LE44.Timer Out	Signal: Timer Output
LE44.Out	Signal: Latched Output (Q)
LE44.Out inverted	Signal: Negated Latched Output (Q NOT)
LE44.Gate In1-I	State of the module input: Assignment of the Input Signal
LE44.Gate In2-I	State of the module input: Assignment of the Input Signal
LE44.Gate In3-I	State of the module input: Assignment of the Input Signal
LE44.Gate In4-I	State of the module input: Assignment of the Input Signal
LE44.Reset Latch-I	State of the module input: Reset Signal for the Latching
LE45.Gate Out	Signal: Output of the logic gate
LE45.Timer Out	Signal: Timer Output
LE45.Out	Signal: Latched Output (Q)
LE45.Out inverted	Signal: Negated Latched Output (Q NOT)
LE45.Gate In1-I	State of the module input: Assignment of the Input Signal
LE45.Gate In2-I	State of the module input: Assignment of the Input Signal
LE45.Gate In3-I	State of the module input: Assignment of the Input Signal
LE45.Gate In4-I	State of the module input: Assignment of the Input Signal
LE45.Reset Latch-I	State of the module input: Reset Signal for the Latching
LE46.Gate Out	Signal: Output of the logic gate
LE46.Timer Out	Signal: Timer Output
LE46.Out	Signal: Latched Output (Q)
LE46.Out inverted	Signal: Negated Latched Output (Q NOT)
LE46.Gate In1-I	State of the module input: Assignment of the Input Signal
LE46.Gate In2-I	State of the module input: Assignment of the Input Signal
LE46.Gate In3-I	State of the module input: Assignment of the Input Signal
LE46.Gate In4-I	State of the module input: Assignment of the Input Signal
LE46.Reset Latch-I	State of the module input: Reset Signal for the Latching
LE47.Gate Out	Signal: Output of the logic gate
LE47.Timer Out	Signal: Timer Output
LE47.Out	Signal: Latched Output (Q)
LE47.Out inverted	Signal: Negated Latched Output (Q NOT)
LE47.Gate In1-I	State of the module input: Assignment of the Input Signal
LE47.Gate In2-I	State of the module input: Assignment of the Input Signal
LE47.Gate In3-I	State of the module input: Assignment of the Input Signal
LE47.Gate In4-I	State of the module input: Assignment of the Input Signal
LE47.Reset Latch-I	State of the module input: Reset Signal for the Latching

1..n, Assignment List	Description
LE48.Gate Out	Signal: Output of the logic gate
LE48.Timer Out	Signal: Timer Output
LE48.Out	Signal: Latched Output (Q)
LE48.Out inverted	Signal: Negated Latched Output (Q NOT)
LE48.Gate In1-I	State of the module input: Assignment of the Input Signal
LE48.Gate In2-I	State of the module input: Assignment of the Input Signal
LE48.Gate In3-I	State of the module input: Assignment of the Input Signal
LE48.Gate In4-I	State of the module input: Assignment of the Input Signal
LE48.Reset Latch-I	State of the module input: Reset Signal for the Latching
LE49.Gate Out	Signal: Output of the logic gate
LE49.Timer Out	Signal: Timer Output
LE49.Out	Signal: Latched Output (Q)
LE49.Out inverted	Signal: Negated Latched Output (Q NOT)
LE49.Gate In1-I	State of the module input: Assignment of the Input Signal
LE49.Gate In2-I	State of the module input: Assignment of the Input Signal
LE49.Gate In3-I	State of the module input: Assignment of the Input Signal
LE49.Gate In4-I	State of the module input: Assignment of the Input Signal
LE49.Reset Latch-I	State of the module input: Reset Signal for the Latching
LE50.Gate Out	Signal: Output of the logic gate
LE50.Timer Out	Signal: Timer Output
LE50.Out	Signal: Latched Output (Q)
LE50.Out inverted	Signal: Negated Latched Output (Q NOT)
LE50.Gate In1-I	State of the module input: Assignment of the Input Signal
LE50.Gate In2-I	State of the module input: Assignment of the Input Signal
LE50.Gate In3-I	State of the module input: Assignment of the Input Signal
LE50.Gate In4-I	State of the module input: Assignment of the Input Signal
LE50.Reset Latch-I	State of the module input: Reset Signal for the Latching
LE51.Gate Out	Signal: Output of the logic gate
LE51.Timer Out	Signal: Timer Output
LE51.Out	Signal: Latched Output (Q)
LE51.Out inverted	Signal: Negated Latched Output (Q NOT)
LE51.Gate In1-I	State of the module input: Assignment of the Input Signal
LE51.Gate In2-I	State of the module input: Assignment of the Input Signal
LE51.Gate In3-I	State of the module input: Assignment of the Input Signal
LE51.Gate In4-I	State of the module input: Assignment of the Input Signal
LE51.Reset Latch-I	State of the module input: Reset Signal for the Latching
LE52.Gate Out	Signal: Output of the logic gate
LE52.Timer Out	Signal: Timer Output

1..n, Assignment List	Description
LE52.Out	Signal: Latched Output (Q)
LE52.Out inverted	Signal: Negated Latched Output (Q NOT)
LE52.Gate In1-I	State of the module input: Assignment of the Input Signal
LE52.Gate In2-I	State of the module input: Assignment of the Input Signal
LE52.Gate In3-I	State of the module input: Assignment of the Input Signal
LE52.Gate In4-I	State of the module input: Assignment of the Input Signal
LE52.Reset Latch-I	State of the module input: Reset Signal for the Latching
LE53.Gate Out	Signal: Output of the logic gate
LE53.Timer Out	Signal: Timer Output
LE53.Out	Signal: Latched Output (Q)
LE53.Out inverted	Signal: Negated Latched Output (Q NOT)
LE53.Gate In1-I	State of the module input: Assignment of the Input Signal
LE53.Gate In2-I	State of the module input: Assignment of the Input Signal
LE53.Gate In3-I	State of the module input: Assignment of the Input Signal
LE53.Gate In4-I	State of the module input: Assignment of the Input Signal
LE53.Reset Latch-I	State of the module input: Reset Signal for the Latching
LE54.Gate Out	Signal: Output of the logic gate
LE54.Timer Out	Signal: Timer Output
LE54.Out	Signal: Latched Output (Q)
LE54.Out inverted	Signal: Negated Latched Output (Q NOT)
LE54.Gate In1-I	State of the module input: Assignment of the Input Signal
LE54.Gate In2-I	State of the module input: Assignment of the Input Signal
LE54.Gate In3-I	State of the module input: Assignment of the Input Signal
LE54.Gate In4-I	State of the module input: Assignment of the Input Signal
LE54.Reset Latch-I	State of the module input: Reset Signal for the Latching
LE55.Gate Out	Signal: Output of the logic gate
LE55.Timer Out	Signal: Timer Output
LE55.Out	Signal: Latched Output (Q)
LE55.Out inverted	Signal: Negated Latched Output (Q NOT)
LE55.Gate In1-I	State of the module input: Assignment of the Input Signal
LE55.Gate In2-I	State of the module input: Assignment of the Input Signal
LE55.Gate In3-I	State of the module input: Assignment of the Input Signal
LE55.Gate In4-I	State of the module input: Assignment of the Input Signal
LE55.Reset Latch-I	State of the module input: Reset Signal for the Latching
LE56.Gate Out	Signal: Output of the logic gate
LE56.Timer Out	Signal: Timer Output
LE56.Out	Signal: Latched Output (Q)
LE56.Out inverted	Signal: Negated Latched Output (Q NOT)

1..n, Assignment List	Description
LE56.Gate In1-I	State of the module input: Assignment of the Input Signal
LE56.Gate In2-I	State of the module input: Assignment of the Input Signal
LE56.Gate In3-I	State of the module input: Assignment of the Input Signal
LE56.Gate In4-I	State of the module input: Assignment of the Input Signal
LE56.Reset Latch-I	State of the module input: Reset Signal for the Latching
LE57.Gate Out	Signal: Output of the logic gate
LE57.Timer Out	Signal: Timer Output
LE57.Out	Signal: Latched Output (Q)
LE57.Out inverted	Signal: Negated Latched Output (Q NOT)
LE57.Gate In1-I	State of the module input: Assignment of the Input Signal
LE57.Gate In2-I	State of the module input: Assignment of the Input Signal
LE57.Gate In3-I	State of the module input: Assignment of the Input Signal
LE57.Gate In4-I	State of the module input: Assignment of the Input Signal
LE57.Reset Latch-I	State of the module input: Reset Signal for the Latching
LE58.Gate Out	Signal: Output of the logic gate
LE58.Timer Out	Signal: Timer Output
LE58.Out	Signal: Latched Output (Q)
LE58.Out inverted	Signal: Negated Latched Output (Q NOT)
LE58.Gate In1-I	State of the module input: Assignment of the Input Signal
LE58.Gate In2-I	State of the module input: Assignment of the Input Signal
LE58.Gate In3-I	State of the module input: Assignment of the Input Signal
LE58.Gate In4-I	State of the module input: Assignment of the Input Signal
LE58.Reset Latch-I	State of the module input: Reset Signal for the Latching
LE59.Gate Out	Signal: Output of the logic gate
LE59.Timer Out	Signal: Timer Output
LE59.Out	Signal: Latched Output (Q)
LE59.Out inverted	Signal: Negated Latched Output (Q NOT)
LE59.Gate In1-I	State of the module input: Assignment of the Input Signal
LE59.Gate In2-I	State of the module input: Assignment of the Input Signal
LE59.Gate In3-I	State of the module input: Assignment of the Input Signal
LE59.Gate In4-I	State of the module input: Assignment of the Input Signal
LE59.Reset Latch-I	State of the module input: Reset Signal for the Latching
LE60.Gate Out	Signal: Output of the logic gate
LE60.Timer Out	Signal: Timer Output
LE60.Out	Signal: Latched Output (Q)
LE60.Out inverted	Signal: Negated Latched Output (Q NOT)
LE60.Gate In1-I	State of the module input: Assignment of the Input Signal
LE60.Gate In2-I	State of the module input: Assignment of the Input Signal

1..n, Assignment List	Description
LE60.Gate In3-I	State of the module input: Assignment of the Input Signal
LE60.Gate In4-I	State of the module input: Assignment of the Input Signal
LE60.Reset Latch-I	State of the module input: Reset Signal for the Latching
LE61.Gate Out	Signal: Output of the logic gate
LE61.Timer Out	Signal: Timer Output
LE61.Out	Signal: Latched Output (Q)
LE61.Out inverted	Signal: Negated Latched Output (Q NOT)
LE61.Gate In1-I	State of the module input: Assignment of the Input Signal
LE61.Gate In2-I	State of the module input: Assignment of the Input Signal
LE61.Gate In3-I	State of the module input: Assignment of the Input Signal
LE61.Gate In4-I	State of the module input: Assignment of the Input Signal
LE61.Reset Latch-I	State of the module input: Reset Signal for the Latching
LE62.Gate Out	Signal: Output of the logic gate
LE62.Timer Out	Signal: Timer Output
LE62.Out	Signal: Latched Output (Q)
LE62.Out inverted	Signal: Negated Latched Output (Q NOT)
LE62.Gate In1-I	State of the module input: Assignment of the Input Signal
LE62.Gate In2-I	State of the module input: Assignment of the Input Signal
LE62.Gate In3-I	State of the module input: Assignment of the Input Signal
LE62.Gate In4-I	State of the module input: Assignment of the Input Signal
LE62.Reset Latch-I	State of the module input: Reset Signal for the Latching
LE63.Gate Out	Signal: Output of the logic gate
LE63.Timer Out	Signal: Timer Output
LE63.Out	Signal: Latched Output (Q)
LE63.Out inverted	Signal: Negated Latched Output (Q NOT)
LE63.Gate In1-I	State of the module input: Assignment of the Input Signal
LE63.Gate In2-I	State of the module input: Assignment of the Input Signal
LE63.Gate In3-I	State of the module input: Assignment of the Input Signal
LE63.Gate In4-I	State of the module input: Assignment of the Input Signal
LE63.Reset Latch-I	State of the module input: Reset Signal for the Latching
LE64.Gate Out	Signal: Output of the logic gate
LE64.Timer Out	Signal: Timer Output
LE64.Out	Signal: Latched Output (Q)
LE64.Out inverted	Signal: Negated Latched Output (Q NOT)
LE64.Gate In1-I	State of the module input: Assignment of the Input Signal
LE64.Gate In2-I	State of the module input: Assignment of the Input Signal
LE64.Gate In3-I	State of the module input: Assignment of the Input Signal
LE64.Gate In4-I	State of the module input: Assignment of the Input Signal

1..n, Assignment List	Description
LE64.Reset Latch-I	State of the module input: Reset Signal for the Latching
LE65.Gate Out	Signal: Output of the logic gate
LE65.Timer Out	Signal: Timer Output
LE65.Out	Signal: Latched Output (Q)
LE65.Out inverted	Signal: Negated Latched Output (Q NOT)
LE65.Gate In1-I	State of the module input: Assignment of the Input Signal
LE65.Gate In2-I	State of the module input: Assignment of the Input Signal
LE65.Gate In3-I	State of the module input: Assignment of the Input Signal
LE65.Gate In4-I	State of the module input: Assignment of the Input Signal
LE65.Reset Latch-I	State of the module input: Reset Signal for the Latching
LE66.Gate Out	Signal: Output of the logic gate
LE66.Timer Out	Signal: Timer Output
LE66.Out	Signal: Latched Output (Q)
LE66.Out inverted	Signal: Negated Latched Output (Q NOT)
LE66.Gate In1-I	State of the module input: Assignment of the Input Signal
LE66.Gate In2-I	State of the module input: Assignment of the Input Signal
LE66.Gate In3-I	State of the module input: Assignment of the Input Signal
LE66.Gate In4-I	State of the module input: Assignment of the Input Signal
LE66.Reset Latch-I	State of the module input: Reset Signal for the Latching
LE67.Gate Out	Signal: Output of the logic gate
LE67.Timer Out	Signal: Timer Output
LE67.Out	Signal: Latched Output (Q)
LE67.Out inverted	Signal: Negated Latched Output (Q NOT)
LE67.Gate In1-I	State of the module input: Assignment of the Input Signal
LE67.Gate In2-I	State of the module input: Assignment of the Input Signal
LE67.Gate In3-I	State of the module input: Assignment of the Input Signal
LE67.Gate In4-I	State of the module input: Assignment of the Input Signal
LE67.Reset Latch-I	State of the module input: Reset Signal for the Latching
LE68.Gate Out	Signal: Output of the logic gate
LE68.Timer Out	Signal: Timer Output
LE68.Out	Signal: Latched Output (Q)
LE68.Out inverted	Signal: Negated Latched Output (Q NOT)
LE68.Gate In1-I	State of the module input: Assignment of the Input Signal
LE68.Gate In2-I	State of the module input: Assignment of the Input Signal
LE68.Gate In3-I	State of the module input: Assignment of the Input Signal
LE68.Gate In4-I	State of the module input: Assignment of the Input Signal
LE68.Reset Latch-I	State of the module input: Reset Signal for the Latching
LE69.Gate Out	Signal: Output of the logic gate

1..n, Assignment List	Description
LE69.Timer Out	Signal: Timer Output
LE69.Out	Signal: Latched Output (Q)
LE69.Out inverted	Signal: Negated Latched Output (Q NOT)
LE69.Gate In1-I	State of the module input: Assignment of the Input Signal
LE69.Gate In2-I	State of the module input: Assignment of the Input Signal
LE69.Gate In3-I	State of the module input: Assignment of the Input Signal
LE69.Gate In4-I	State of the module input: Assignment of the Input Signal
LE69.Reset Latch-I	State of the module input: Reset Signal for the Latching
LE70.Gate Out	Signal: Output of the logic gate
LE70.Timer Out	Signal: Timer Output
LE70.Out	Signal: Latched Output (Q)
LE70.Out inverted	Signal: Negated Latched Output (Q NOT)
LE70.Gate In1-I	State of the module input: Assignment of the Input Signal
LE70.Gate In2-I	State of the module input: Assignment of the Input Signal
LE70.Gate In3-I	State of the module input: Assignment of the Input Signal
LE70.Gate In4-I	State of the module input: Assignment of the Input Signal
LE70.Reset Latch-I	State of the module input: Reset Signal for the Latching
LE71.Gate Out	Signal: Output of the logic gate
LE71.Timer Out	Signal: Timer Output
LE71.Out	Signal: Latched Output (Q)
LE71.Out inverted	Signal: Negated Latched Output (Q NOT)
LE71.Gate In1-I	State of the module input: Assignment of the Input Signal
LE71.Gate In2-I	State of the module input: Assignment of the Input Signal
LE71.Gate In3-I	State of the module input: Assignment of the Input Signal
LE71.Gate In4-I	State of the module input: Assignment of the Input Signal
LE71.Reset Latch-I	State of the module input: Reset Signal for the Latching
LE72.Gate Out	Signal: Output of the logic gate
LE72.Timer Out	Signal: Timer Output
LE72.Out	Signal: Latched Output (Q)
LE72.Out inverted	Signal: Negated Latched Output (Q NOT)
LE72.Gate In1-I	State of the module input: Assignment of the Input Signal
LE72.Gate In2-I	State of the module input: Assignment of the Input Signal
LE72.Gate In3-I	State of the module input: Assignment of the Input Signal
LE72.Gate In4-I	State of the module input: Assignment of the Input Signal
LE72.Reset Latch-I	State of the module input: Reset Signal for the Latching
LE73.Gate Out	Signal: Output of the logic gate
LE73.Timer Out	Signal: Timer Output
LE73.Out	Signal: Latched Output (Q)

1..n, Assignment List	Description
LE73.Out inverted	Signal: Negated Latched Output (Q NOT)
LE73.Gate In1-I	State of the module input: Assignment of the Input Signal
LE73.Gate In2-I	State of the module input: Assignment of the Input Signal
LE73.Gate In3-I	State of the module input: Assignment of the Input Signal
LE73.Gate In4-I	State of the module input: Assignment of the Input Signal
LE73.Reset Latch-I	State of the module input: Reset Signal for the Latching
LE74.Gate Out	Signal: Output of the logic gate
LE74.Timer Out	Signal: Timer Output
LE74.Out	Signal: Latched Output (Q)
LE74.Out inverted	Signal: Negated Latched Output (Q NOT)
LE74.Gate In1-I	State of the module input: Assignment of the Input Signal
LE74.Gate In2-I	State of the module input: Assignment of the Input Signal
LE74.Gate In3-I	State of the module input: Assignment of the Input Signal
LE74.Gate In4-I	State of the module input: Assignment of the Input Signal
LE74.Reset Latch-I	State of the module input: Reset Signal for the Latching
LE75.Gate Out	Signal: Output of the logic gate
LE75.Timer Out	Signal: Timer Output
LE75.Out	Signal: Latched Output (Q)
LE75.Out inverted	Signal: Negated Latched Output (Q NOT)
LE75.Gate In1-I	State of the module input: Assignment of the Input Signal
LE75.Gate In2-I	State of the module input: Assignment of the Input Signal
LE75.Gate In3-I	State of the module input: Assignment of the Input Signal
LE75.Gate In4-I	State of the module input: Assignment of the Input Signal
LE75.Reset Latch-I	State of the module input: Reset Signal for the Latching
LE76.Gate Out	Signal: Output of the logic gate
LE76.Timer Out	Signal: Timer Output
LE76.Out	Signal: Latched Output (Q)
LE76.Out inverted	Signal: Negated Latched Output (Q NOT)
LE76.Gate In1-I	State of the module input: Assignment of the Input Signal
LE76.Gate In2-I	State of the module input: Assignment of the Input Signal
LE76.Gate In3-I	State of the module input: Assignment of the Input Signal
LE76.Gate In4-I	State of the module input: Assignment of the Input Signal
LE76.Reset Latch-I	State of the module input: Reset Signal for the Latching
LE77.Gate Out	Signal: Output of the logic gate
LE77.Timer Out	Signal: Timer Output
LE77.Out	Signal: Latched Output (Q)
LE77.Out inverted	Signal: Negated Latched Output (Q NOT)
LE77.Gate In1-I	State of the module input: Assignment of the Input Signal

1..n, Assignment List	Description
LE77.Gate In2-I	State of the module input: Assignment of the Input Signal
LE77.Gate In3-I	State of the module input: Assignment of the Input Signal
LE77.Gate In4-I	State of the module input: Assignment of the Input Signal
LE77.Reset Latch-I	State of the module input: Reset Signal for the Latching
LE78.Gate Out	Signal: Output of the logic gate
LE78.Timer Out	Signal: Timer Output
LE78.Out	Signal: Latched Output (Q)
LE78.Out inverted	Signal: Negated Latched Output (Q NOT)
LE78.Gate In1-I	State of the module input: Assignment of the Input Signal
LE78.Gate In2-I	State of the module input: Assignment of the Input Signal
LE78.Gate In3-I	State of the module input: Assignment of the Input Signal
LE78.Gate In4-I	State of the module input: Assignment of the Input Signal
LE78.Reset Latch-I	State of the module input: Reset Signal for the Latching
LE79.Gate Out	Signal: Output of the logic gate
LE79.Timer Out	Signal: Timer Output
LE79.Out	Signal: Latched Output (Q)
LE79.Out inverted	Signal: Negated Latched Output (Q NOT)
LE79.Gate In1-I	State of the module input: Assignment of the Input Signal
LE79.Gate In2-I	State of the module input: Assignment of the Input Signal
LE79.Gate In3-I	State of the module input: Assignment of the Input Signal
LE79.Gate In4-I	State of the module input: Assignment of the Input Signal
LE79.Reset Latch-I	State of the module input: Reset Signal for the Latching
LE80.Gate Out	Signal: Output of the logic gate
LE80.Timer Out	Signal: Timer Output
LE80.Out	Signal: Latched Output (Q)
LE80.Out inverted	Signal: Negated Latched Output (Q NOT)
LE80.Gate In1-I	State of the module input: Assignment of the Input Signal
LE80.Gate In2-I	State of the module input: Assignment of the Input Signal
LE80.Gate In3-I	State of the module input: Assignment of the Input Signal
LE80.Gate In4-I	State of the module input: Assignment of the Input Signal
LE80.Reset Latch-I	State of the module input: Reset Signal for the Latching
Manual Start	Fault Simulation has been started manually.
Manual Stop	Fault Simulation has been stopped manually.
Running	Signal: Measuring value simulation is running
Started	Fault Simulation has been started
Stopped	Fault Simulation has been stopped
Ex Start Simulation-I	State of the module input:External Start of Fault Simulation (Using the test parameters)
ExBlo1-I	Module input state: External blocking1

1..n, Assignment List	Description
ExBlo2-I	Module input state: External blocking2
Ex ForcePost-I	State of the module input:Force Post state. Abort simulation.
PS 1	Signal: The currently active Parameter Set is PS 1
PS 2	Signal: The currently active Parameter Set is PS 2
PS 3	Signal: The currently active Parameter Set is PS 3
PS 4	Signal: The currently active Parameter Set is PS 4
PSS manual	Signal: Manual Switch over of a Parameter Set
PSS via Scada	Signal: Parameter Set Switch via Scada. Write into this output byte the integer of the parameter set that should become active (e.g. 4 => Switch onto parameter set 4).
PSS via Inp fct	Signal: Parameter Set Switch via input function
min 1 param changed	Signal: At least one parameter has been changed
Setting Lock Bypass	Signal: Short-period unlock of the Setting Lock
Maint Mode Active	Signal: Arc Flash Reduction Maintenance Active
Maint Mode Inactive	Signal: Arc Flash Reduction Maintenance Inactive
MaintMode Manually	Signal: Arc Flash Reduction Maintenance Manual Mode
Maint Mode SCADA	Signal: Arc Flash Reduction Maintenance SCADA Mode
Maint Mode DI	Signal: Arc Flash Reduction Maintenance Digital Input Mode
Ack LED	Signal: LEDs acknowledgement
Ack BO	Signal: Acknowledgement of the Binary Outputs
Ack Scada	Signal: Acknowledge latched SCADA signals
Ack TripCmd	Signal: Reset Trip Command
Ack LED-HMI	Signal: LEDs acknowledgement, triggered at the HMI
Ack BO-HMI	Signal: Acknowledgement of the Binary Outputs, triggered at the HMI
Ack Scada-HMI	Signal: Acknowledge latched SCADA signals, triggered at the HMI
Ack TripCmd-HMI	Signal: Reset Trip Command, triggered at the HMI
Ack LED-Sca	Signal: LEDs acknowledgement, triggered via SCADA
Ack BO-Sca	Signal: Acknowledgement of the Binary Outputs, triggered via SCADA
Ack Counter-Sca	Signal: Reset of all Counters, triggered via SCADA
Ack Scada-Sca	Signal: Acknowledge latched SCADA signals, triggered via SCADA
Ack TripCmd-Sca	Signal: Reset Trip Command, triggered via SCADA
Res OperationsCr	Signal:: Res OperationsCr
Res AlarmCr	Signal:: Res AlarmCr
Res TripCmdCr	Signal:: Res TripCmdCr
Res TotalCr	Signal:: Res TotalCr
Ack LED-I	Module input state: LEDs acknowledgement by digital input
Ack BO-I	Module input state: Acknowledgement of the binary Output Relays
Ack Scada-I	Module input state: Acknowledge latched SCADA signals.
PS1-I	State of the module input respectively of the signal, that should activate this Parameter Setting Group.

1..n, Assignment List	Description
PS2-I	State of the module input respectively of the signal, that should activate this Parameter Setting Group.
PS3-I	State of the module input respectively of the signal, that should activate this Parameter Setting Group.
PS4-I	State of the module input respectively of the signal, that should activate this Parameter Setting Group.
Setting Lock-I	State of the module input: No parameters can be changed as long as this input is true. The parameter settings are locked.
Maint Mode-I	Module Input State: Arc Flash Reduction Maintenance Switch
Internal test state	Auxiliary state for testing purposes.

17.167 VTS Block

Selection list referenced by the following parameters:

- V[1] . Meas Circuit Superv
- *[...]*

VTS Block	Description
Inactive	Inactive
Active	Active

17.168 CB Manager

Referenced by:

- Sync . CB Pos Detect

CB Manager	Description
-	No assignment
Pos	Signal: Circuit Breaker Position (0 = Indeterminate, 1 = OFF, 2 = ON, 3 = Disturbed)

17.169 1..n, Dig Inputs

Selection list referenced by the following parameters:

- ReCon[1] . PCC Fuse Fail VT
- TCS . Input 1
- TCS . Input 2

1..n, Dig Inputs	Description
-	No assignment
DI 1	Signal: Digital Input
DI 2	Signal: Digital Input
DI 3	Signal: Digital Input
DI 4	Signal: Digital Input
DI 5	Signal: Digital Input
DI 6	Signal: Digital Input
DI 7	Signal: Digital Input
DI 8	Signal: Digital Input

17.170 1..n, DI-LogicList

Selection list referenced by the following parameters:

- Sys . Maint Mode Activated by
- SG[1] . Aux ON
- SG[1] . Aux OFF
- SG[1] . Ready
- SG[1] . Removed
- SG[1] . SCmd ON
- *[. . .]*

1..n, DI-LogicList	Description
-	No assignment
DI 1	Signal: Digital Input
DI 2	Signal: Digital Input
DI 3	Signal: Digital Input
DI 4	Signal: Digital Input
DI 5	Signal: Digital Input
DI 6	Signal: Digital Input
DI 7	Signal: Digital Input

1..n, DI-LogicList	Description
DI 8	Signal: Digital Input
BinaryOutput0	Virtual Digital Output (DNP). This corresponds to a virtual binary input of the protective device.
BinaryOutput1	Virtual Digital Output (DNP). This corresponds to a virtual binary input of the protective device.
BinaryOutput2	Virtual Digital Output (DNP). This corresponds to a virtual binary input of the protective device.
BinaryOutput3	Virtual Digital Output (DNP). This corresponds to a virtual binary input of the protective device.
BinaryOutput4	Virtual Digital Output (DNP). This corresponds to a virtual binary input of the protective device.
BinaryOutput5	Virtual Digital Output (DNP). This corresponds to a virtual binary input of the protective device.
BinaryOutput6	Virtual Digital Output (DNP). This corresponds to a virtual binary input of the protective device.
BinaryOutput7	Virtual Digital Output (DNP). This corresponds to a virtual binary input of the protective device.
BinaryOutput8	Virtual Digital Output (DNP). This corresponds to a virtual binary input of the protective device.
BinaryOutput9	Virtual Digital Output (DNP). This corresponds to a virtual binary input of the protective device.
BinaryOutput10	Virtual Digital Output (DNP). This corresponds to a virtual binary input of the protective device.
BinaryOutput11	Virtual Digital Output (DNP). This corresponds to a virtual binary input of the protective device.
BinaryOutput12	Virtual Digital Output (DNP). This corresponds to a virtual binary input of the protective device.
BinaryOutput13	Virtual Digital Output (DNP). This corresponds to a virtual binary input of the protective device.
BinaryOutput14	Virtual Digital Output (DNP). This corresponds to a virtual binary input of the protective device.
BinaryOutput15	Virtual Digital Output (DNP). This corresponds to a virtual binary input of the protective device.
BinaryOutput16	Virtual Digital Output (DNP). This corresponds to a virtual binary input of the protective device.
BinaryOutput17	Virtual Digital Output (DNP). This corresponds to a virtual binary input of the protective device.
BinaryOutput18	Virtual Digital Output (DNP). This corresponds to a virtual binary input of the protective device.
BinaryOutput19	Virtual Digital Output (DNP). This corresponds to a virtual binary input of the protective device.
BinaryOutput20	Virtual Digital Output (DNP). This corresponds to a virtual binary input of the protective device.
BinaryOutput21	Virtual Digital Output (DNP). This corresponds to a virtual binary input of the protective device.
BinaryOutput22	Virtual Digital Output (DNP). This corresponds to a virtual binary input of the protective device.
BinaryOutput23	Virtual Digital Output (DNP). This corresponds to a virtual binary input of the protective device.

1..n, DI-LogicList	Description
BinaryOutput24	Virtual Digital Output (DNP). This corresponds to a virtual binary input of the protective device.
BinaryOutput25	Virtual Digital Output (DNP). This corresponds to a virtual binary input of the protective device.
BinaryOutput26	Virtual Digital Output (DNP). This corresponds to a virtual binary input of the protective device.
BinaryOutput27	Virtual Digital Output (DNP). This corresponds to a virtual binary input of the protective device.
BinaryOutput28	Virtual Digital Output (DNP). This corresponds to a virtual binary input of the protective device.
BinaryOutput29	Virtual Digital Output (DNP). This corresponds to a virtual binary input of the protective device.
BinaryOutput30	Virtual Digital Output (DNP). This corresponds to a virtual binary input of the protective device.
BinaryOutput31	Virtual Digital Output (DNP). This corresponds to a virtual binary input of the protective device.
Scada Cmd 1	Scada Command
Scada Cmd 2	Scada Command
Scada Cmd 3	Scada Command
Scada Cmd 4	Scada Command
Scada Cmd 5	Scada Command
Scada Cmd 6	Scada Command
Scada Cmd 7	Scada Command
Scada Cmd 8	Scada Command
Scada Cmd 9	Scada Command
Scada Cmd 10	Scada Command
Scada Cmd 11	Scada Command
Scada Cmd 12	Scada Command
Scada Cmd 13	Scada Command
Scada Cmd 14	Scada Command
Scada Cmd 15	Scada Command
Scada Cmd 16	Scada Command
LE1.Gate Out	Signal: Output of the logic gate
LE1.Timer Out	Signal: Timer Output
LE1.Out	Signal: Latched Output (Q)
LE1.Out inverted	Signal: Negated Latched Output (Q NOT)
LE2.Gate Out	Signal: Output of the logic gate
LE2.Timer Out	Signal: Timer Output
LE2.Out	Signal: Latched Output (Q)
LE2.Out inverted	Signal: Negated Latched Output (Q NOT)
LE3.Gate Out	Signal: Output of the logic gate
LE3.Timer Out	Signal: Timer Output

1..n, DI-LogicList	Description
LE3.Out	Signal: Latched Output (Q)
LE3.Out inverted	Signal: Negated Latched Output (Q NOT)
LE4.Gate Out	Signal: Output of the logic gate
LE4.Timer Out	Signal: Timer Output
LE4.Out	Signal: Latched Output (Q)
LE4.Out inverted	Signal: Negated Latched Output (Q NOT)
LE5.Gate Out	Signal: Output of the logic gate
LE5.Timer Out	Signal: Timer Output
LE5.Out	Signal: Latched Output (Q)
LE5.Out inverted	Signal: Negated Latched Output (Q NOT)
LE6.Gate Out	Signal: Output of the logic gate
LE6.Timer Out	Signal: Timer Output
LE6.Out	Signal: Latched Output (Q)
LE6.Out inverted	Signal: Negated Latched Output (Q NOT)
LE7.Gate Out	Signal: Output of the logic gate
LE7.Timer Out	Signal: Timer Output
LE7.Out	Signal: Latched Output (Q)
LE7.Out inverted	Signal: Negated Latched Output (Q NOT)
LE8.Gate Out	Signal: Output of the logic gate
LE8.Timer Out	Signal: Timer Output
LE8.Out	Signal: Latched Output (Q)
LE8.Out inverted	Signal: Negated Latched Output (Q NOT)
LE9.Gate Out	Signal: Output of the logic gate
LE9.Timer Out	Signal: Timer Output
LE9.Out	Signal: Latched Output (Q)
LE9.Out inverted	Signal: Negated Latched Output (Q NOT)
LE10.Gate Out	Signal: Output of the logic gate
LE10.Timer Out	Signal: Timer Output
LE10.Out	Signal: Latched Output (Q)
LE10.Out inverted	Signal: Negated Latched Output (Q NOT)
LE11.Gate Out	Signal: Output of the logic gate
LE11.Timer Out	Signal: Timer Output
LE11.Out	Signal: Latched Output (Q)
LE11.Out inverted	Signal: Negated Latched Output (Q NOT)
LE12.Gate Out	Signal: Output of the logic gate
LE12.Timer Out	Signal: Timer Output
LE12.Out	Signal: Latched Output (Q)
LE12.Out inverted	Signal: Negated Latched Output (Q NOT)

1..n, DI-LogicList	Description
LE13.Gate Out	Signal: Output of the logic gate
LE13.Timer Out	Signal: Timer Output
LE13.Out	Signal: Latched Output (Q)
LE13.Out inverted	Signal: Negated Latched Output (Q NOT)
LE14.Gate Out	Signal: Output of the logic gate
LE14.Timer Out	Signal: Timer Output
LE14.Out	Signal: Latched Output (Q)
LE14.Out inverted	Signal: Negated Latched Output (Q NOT)
LE15.Gate Out	Signal: Output of the logic gate
LE15.Timer Out	Signal: Timer Output
LE15.Out	Signal: Latched Output (Q)
LE15.Out inverted	Signal: Negated Latched Output (Q NOT)
LE16.Gate Out	Signal: Output of the logic gate
LE16.Timer Out	Signal: Timer Output
LE16.Out	Signal: Latched Output (Q)
LE16.Out inverted	Signal: Negated Latched Output (Q NOT)
LE17.Gate Out	Signal: Output of the logic gate
LE17.Timer Out	Signal: Timer Output
LE17.Out	Signal: Latched Output (Q)
LE17.Out inverted	Signal: Negated Latched Output (Q NOT)
LE18.Gate Out	Signal: Output of the logic gate
LE18.Timer Out	Signal: Timer Output
LE18.Out	Signal: Latched Output (Q)
LE18.Out inverted	Signal: Negated Latched Output (Q NOT)
LE19.Gate Out	Signal: Output of the logic gate
LE19.Timer Out	Signal: Timer Output
LE19.Out	Signal: Latched Output (Q)
LE19.Out inverted	Signal: Negated Latched Output (Q NOT)
LE20.Gate Out	Signal: Output of the logic gate
LE20.Timer Out	Signal: Timer Output
LE20.Out	Signal: Latched Output (Q)
LE20.Out inverted	Signal: Negated Latched Output (Q NOT)
LE21.Gate Out	Signal: Output of the logic gate
LE21.Timer Out	Signal: Timer Output
LE21.Out	Signal: Latched Output (Q)
LE21.Out inverted	Signal: Negated Latched Output (Q NOT)
LE22.Gate Out	Signal: Output of the logic gate
LE22.Timer Out	Signal: Timer Output

1..n, DI-LogicList	Description
LE22.Out	Signal: Latched Output (Q)
LE22.Out inverted	Signal: Negated Latched Output (Q NOT)
LE23.Gate Out	Signal: Output of the logic gate
LE23.Timer Out	Signal: Timer Output
LE23.Out	Signal: Latched Output (Q)
LE23.Out inverted	Signal: Negated Latched Output (Q NOT)
LE24.Gate Out	Signal: Output of the logic gate
LE24.Timer Out	Signal: Timer Output
LE24.Out	Signal: Latched Output (Q)
LE24.Out inverted	Signal: Negated Latched Output (Q NOT)
LE25.Gate Out	Signal: Output of the logic gate
LE25.Timer Out	Signal: Timer Output
LE25.Out	Signal: Latched Output (Q)
LE25.Out inverted	Signal: Negated Latched Output (Q NOT)
LE26.Gate Out	Signal: Output of the logic gate
LE26.Timer Out	Signal: Timer Output
LE26.Out	Signal: Latched Output (Q)
LE26.Out inverted	Signal: Negated Latched Output (Q NOT)
LE27.Gate Out	Signal: Output of the logic gate
LE27.Timer Out	Signal: Timer Output
LE27.Out	Signal: Latched Output (Q)
LE27.Out inverted	Signal: Negated Latched Output (Q NOT)
LE28.Gate Out	Signal: Output of the logic gate
LE28.Timer Out	Signal: Timer Output
LE28.Out	Signal: Latched Output (Q)
LE28.Out inverted	Signal: Negated Latched Output (Q NOT)
LE29.Gate Out	Signal: Output of the logic gate
LE29.Timer Out	Signal: Timer Output
LE29.Out	Signal: Latched Output (Q)
LE29.Out inverted	Signal: Negated Latched Output (Q NOT)
LE30.Gate Out	Signal: Output of the logic gate
LE30.Timer Out	Signal: Timer Output
LE30.Out	Signal: Latched Output (Q)
LE30.Out inverted	Signal: Negated Latched Output (Q NOT)
LE31.Gate Out	Signal: Output of the logic gate
LE31.Timer Out	Signal: Timer Output
LE31.Out	Signal: Latched Output (Q)
LE31.Out inverted	Signal: Negated Latched Output (Q NOT)

1..n, DI-LogicList	Description
LE32.Gate Out	Signal: Output of the logic gate
LE32.Timer Out	Signal: Timer Output
LE32.Out	Signal: Latched Output (Q)
LE32.Out inverted	Signal: Negated Latched Output (Q NOT)
LE33.Gate Out	Signal: Output of the logic gate
LE33.Timer Out	Signal: Timer Output
LE33.Out	Signal: Latched Output (Q)
LE33.Out inverted	Signal: Negated Latched Output (Q NOT)
LE34.Gate Out	Signal: Output of the logic gate
LE34.Timer Out	Signal: Timer Output
LE34.Out	Signal: Latched Output (Q)
LE34.Out inverted	Signal: Negated Latched Output (Q NOT)
LE35.Gate Out	Signal: Output of the logic gate
LE35.Timer Out	Signal: Timer Output
LE35.Out	Signal: Latched Output (Q)
LE35.Out inverted	Signal: Negated Latched Output (Q NOT)
LE36.Gate Out	Signal: Output of the logic gate
LE36.Timer Out	Signal: Timer Output
LE36.Out	Signal: Latched Output (Q)
LE36.Out inverted	Signal: Negated Latched Output (Q NOT)
LE37.Gate Out	Signal: Output of the logic gate
LE37.Timer Out	Signal: Timer Output
LE37.Out	Signal: Latched Output (Q)
LE37.Out inverted	Signal: Negated Latched Output (Q NOT)
LE38.Gate Out	Signal: Output of the logic gate
LE38.Timer Out	Signal: Timer Output
LE38.Out	Signal: Latched Output (Q)
LE38.Out inverted	Signal: Negated Latched Output (Q NOT)
LE39.Gate Out	Signal: Output of the logic gate
LE39.Timer Out	Signal: Timer Output
LE39.Out	Signal: Latched Output (Q)
LE39.Out inverted	Signal: Negated Latched Output (Q NOT)
LE40.Gate Out	Signal: Output of the logic gate
LE40.Timer Out	Signal: Timer Output
LE40.Out	Signal: Latched Output (Q)
LE40.Out inverted	Signal: Negated Latched Output (Q NOT)
LE41.Gate Out	Signal: Output of the logic gate
LE41.Timer Out	Signal: Timer Output

1..n, DI-LogicList	Description
LE41.Out	Signal: Latched Output (Q)
LE41.Out inverted	Signal: Negated Latched Output (Q NOT)
LE42.Gate Out	Signal: Output of the logic gate
LE42.Timer Out	Signal: Timer Output
LE42.Out	Signal: Latched Output (Q)
LE42.Out inverted	Signal: Negated Latched Output (Q NOT)
LE43.Gate Out	Signal: Output of the logic gate
LE43.Timer Out	Signal: Timer Output
LE43.Out	Signal: Latched Output (Q)
LE43.Out inverted	Signal: Negated Latched Output (Q NOT)
LE44.Gate Out	Signal: Output of the logic gate
LE44.Timer Out	Signal: Timer Output
LE44.Out	Signal: Latched Output (Q)
LE44.Out inverted	Signal: Negated Latched Output (Q NOT)
LE45.Gate Out	Signal: Output of the logic gate
LE45.Timer Out	Signal: Timer Output
LE45.Out	Signal: Latched Output (Q)
LE45.Out inverted	Signal: Negated Latched Output (Q NOT)
LE46.Gate Out	Signal: Output of the logic gate
LE46.Timer Out	Signal: Timer Output
LE46.Out	Signal: Latched Output (Q)
LE46.Out inverted	Signal: Negated Latched Output (Q NOT)
LE47.Gate Out	Signal: Output of the logic gate
LE47.Timer Out	Signal: Timer Output
LE47.Out	Signal: Latched Output (Q)
LE47.Out inverted	Signal: Negated Latched Output (Q NOT)
LE48.Gate Out	Signal: Output of the logic gate
LE48.Timer Out	Signal: Timer Output
LE48.Out	Signal: Latched Output (Q)
LE48.Out inverted	Signal: Negated Latched Output (Q NOT)
LE49.Gate Out	Signal: Output of the logic gate
LE49.Timer Out	Signal: Timer Output
LE49.Out	Signal: Latched Output (Q)
LE49.Out inverted	Signal: Negated Latched Output (Q NOT)
LE50.Gate Out	Signal: Output of the logic gate
LE50.Timer Out	Signal: Timer Output
LE50.Out	Signal: Latched Output (Q)
LE50.Out inverted	Signal: Negated Latched Output (Q NOT)

1..n, DI-LogicList	Description
LE51.Gate Out	Signal: Output of the logic gate
LE51.Timer Out	Signal: Timer Output
LE51.Out	Signal: Latched Output (Q)
LE51.Out inverted	Signal: Negated Latched Output (Q NOT)
LE52.Gate Out	Signal: Output of the logic gate
LE52.Timer Out	Signal: Timer Output
LE52.Out	Signal: Latched Output (Q)
LE52.Out inverted	Signal: Negated Latched Output (Q NOT)
LE53.Gate Out	Signal: Output of the logic gate
LE53.Timer Out	Signal: Timer Output
LE53.Out	Signal: Latched Output (Q)
LE53.Out inverted	Signal: Negated Latched Output (Q NOT)
LE54.Gate Out	Signal: Output of the logic gate
LE54.Timer Out	Signal: Timer Output
LE54.Out	Signal: Latched Output (Q)
LE54.Out inverted	Signal: Negated Latched Output (Q NOT)
LE55.Gate Out	Signal: Output of the logic gate
LE55.Timer Out	Signal: Timer Output
LE55.Out	Signal: Latched Output (Q)
LE55.Out inverted	Signal: Negated Latched Output (Q NOT)
LE56.Gate Out	Signal: Output of the logic gate
LE56.Timer Out	Signal: Timer Output
LE56.Out	Signal: Latched Output (Q)
LE56.Out inverted	Signal: Negated Latched Output (Q NOT)
LE57.Gate Out	Signal: Output of the logic gate
LE57.Timer Out	Signal: Timer Output
LE57.Out	Signal: Latched Output (Q)
LE57.Out inverted	Signal: Negated Latched Output (Q NOT)
LE58.Gate Out	Signal: Output of the logic gate
LE58.Timer Out	Signal: Timer Output
LE58.Out	Signal: Latched Output (Q)
LE58.Out inverted	Signal: Negated Latched Output (Q NOT)
LE59.Gate Out	Signal: Output of the logic gate
LE59.Timer Out	Signal: Timer Output
LE59.Out	Signal: Latched Output (Q)
LE59.Out inverted	Signal: Negated Latched Output (Q NOT)
LE60.Gate Out	Signal: Output of the logic gate
LE60.Timer Out	Signal: Timer Output

1..n, DI-LogicList	Description
LE60.Out	Signal: Latched Output (Q)
LE60.Out inverted	Signal: Negated Latched Output (Q NOT)
LE61.Gate Out	Signal: Output of the logic gate
LE61.Timer Out	Signal: Timer Output
LE61.Out	Signal: Latched Output (Q)
LE61.Out inverted	Signal: Negated Latched Output (Q NOT)
LE62.Gate Out	Signal: Output of the logic gate
LE62.Timer Out	Signal: Timer Output
LE62.Out	Signal: Latched Output (Q)
LE62.Out inverted	Signal: Negated Latched Output (Q NOT)
LE63.Gate Out	Signal: Output of the logic gate
LE63.Timer Out	Signal: Timer Output
LE63.Out	Signal: Latched Output (Q)
LE63.Out inverted	Signal: Negated Latched Output (Q NOT)
LE64.Gate Out	Signal: Output of the logic gate
LE64.Timer Out	Signal: Timer Output
LE64.Out	Signal: Latched Output (Q)
LE64.Out inverted	Signal: Negated Latched Output (Q NOT)
LE65.Gate Out	Signal: Output of the logic gate
LE65.Timer Out	Signal: Timer Output
LE65.Out	Signal: Latched Output (Q)
LE65.Out inverted	Signal: Negated Latched Output (Q NOT)
LE66.Gate Out	Signal: Output of the logic gate
LE66.Timer Out	Signal: Timer Output
LE66.Out	Signal: Latched Output (Q)
LE66.Out inverted	Signal: Negated Latched Output (Q NOT)
LE67.Gate Out	Signal: Output of the logic gate
LE67.Timer Out	Signal: Timer Output
LE67.Out	Signal: Latched Output (Q)
LE67.Out inverted	Signal: Negated Latched Output (Q NOT)
LE68.Gate Out	Signal: Output of the logic gate
LE68.Timer Out	Signal: Timer Output
LE68.Out	Signal: Latched Output (Q)
LE68.Out inverted	Signal: Negated Latched Output (Q NOT)
LE69.Gate Out	Signal: Output of the logic gate
LE69.Timer Out	Signal: Timer Output
LE69.Out	Signal: Latched Output (Q)
LE69.Out inverted	Signal: Negated Latched Output (Q NOT)

1..n, DI-LogicList	Description
LE70.Gate Out	Signal: Output of the logic gate
LE70.Timer Out	Signal: Timer Output
LE70.Out	Signal: Latched Output (Q)
LE70.Out inverted	Signal: Negated Latched Output (Q NOT)
LE71.Gate Out	Signal: Output of the logic gate
LE71.Timer Out	Signal: Timer Output
LE71.Out	Signal: Latched Output (Q)
LE71.Out inverted	Signal: Negated Latched Output (Q NOT)
LE72.Gate Out	Signal: Output of the logic gate
LE72.Timer Out	Signal: Timer Output
LE72.Out	Signal: Latched Output (Q)
LE72.Out inverted	Signal: Negated Latched Output (Q NOT)
LE73.Gate Out	Signal: Output of the logic gate
LE73.Timer Out	Signal: Timer Output
LE73.Out	Signal: Latched Output (Q)
LE73.Out inverted	Signal: Negated Latched Output (Q NOT)
LE74.Gate Out	Signal: Output of the logic gate
LE74.Timer Out	Signal: Timer Output
LE74.Out	Signal: Latched Output (Q)
LE74.Out inverted	Signal: Negated Latched Output (Q NOT)
LE75.Gate Out	Signal: Output of the logic gate
LE75.Timer Out	Signal: Timer Output
LE75.Out	Signal: Latched Output (Q)
LE75.Out inverted	Signal: Negated Latched Output (Q NOT)
LE76.Gate Out	Signal: Output of the logic gate
LE76.Timer Out	Signal: Timer Output
LE76.Out	Signal: Latched Output (Q)
LE76.Out inverted	Signal: Negated Latched Output (Q NOT)
LE77.Gate Out	Signal: Output of the logic gate
LE77.Timer Out	Signal: Timer Output
LE77.Out	Signal: Latched Output (Q)
LE77.Out inverted	Signal: Negated Latched Output (Q NOT)
LE78.Gate Out	Signal: Output of the logic gate
LE78.Timer Out	Signal: Timer Output
LE78.Out	Signal: Latched Output (Q)
LE78.Out inverted	Signal: Negated Latched Output (Q NOT)
LE79.Gate Out	Signal: Output of the logic gate
LE79.Timer Out	Signal: Timer Output

1..n, DI-LogicList	Description
LE79.Out	Signal: Latched Output (Q)
LE79.Out inverted	Signal: Negated Latched Output (Q NOT)
LE80.Gate Out	Signal: Output of the logic gate
LE80.Timer Out	Signal: Timer Output
LE80.Out	Signal: Latched Output (Q)
LE80.Out inverted	Signal: Negated Latched Output (Q NOT)

17.171 1..n, TrendRecList

Selection list referenced by the following parameters:

- Trend rec . Trend1
- Trend rec . Trend2
- Trend rec . Trend3
- Trend rec . Trend4
- Trend rec . Trend5
- Trend rec . Trend6
- *[. . .]*

1..n, TrendRecList	Description
-	No assignment
VL1	Measured value: Phase-to-neutral voltage (fundamental)
VL2	Measured value: Phase-to-neutral voltage (fundamental)
VL3	Measured value: Phase-to-neutral voltage (fundamental)
VX meas	Measured value (measured): VX measured (fundamental)
VG calc	Measured value (calculated): VG (fundamental)
VL12	Measured value: Phase-to-phase voltage (fundamental)
VL23	Measured value: Phase-to-phase voltage (fundamental)
VL31	Measured value: Phase-to-phase voltage (fundamental)
VL1 RMS	Measured value: Phase-to-neutral voltage (RMS)
VL2 RMS	Measured value: Phase-to-neutral voltage (RMS)
VL3 RMS	Measured value: Phase-to-neutral voltage (RMS)
VX meas RMS	Measured value (measured): VX measured (RMS)
VG calc RMS	Measured value (calculated): VG (RMS)
VL12 RMS	Measured value: Phase-to-phase voltage (RMS)
VL23 RMS	Measured value: Phase-to-phase voltage (RMS)
VL31 RMS	Measured value: Phase-to-phase voltage (RMS)
V0	Measured value (calculated): Symmetrical components Zero voltage(fundamental)

1..n, TrendRecList	Description
V1	Measured value (calculated): Symmetrical components positive phase sequence voltage(fundamental)
V2	Measured value (calculated): Symmetrical components negative phase sequence voltage(fundamental)
%(V2/V1)	Measured value (calculated): V2/V1, phase sequence will be taken into account automatically.
VL1 avg RMS	VL1 average value (RMS)
VL2 avg RMS	VL2 average value (RMS)
VL3 avg RMS	VL3 average value (RMS)
VL12 avg RMS	VL12 average value (RMS)
VL23 avg RMS	VL23 average value (RMS)
VL31 avg RMS	VL31 average value (RMS)
f	Measured value: Frequency
VL1 THD	Measured value (calculated): VL1 Total Harmonic Distortion
VL2 THD	Measured value (calculated): VL2 Total Harmonic Distortion
VL3 THD	Measured value (calculated): VL3 Total Harmonic Distortion
VL12 THD	Measured value (calculated): V12 Total Harmonic Distortion
VL23 THD	Measured value (calculated): V23 Total Harmonic Distortion
VL31 THD	Measured value (calculated): V31 Total Harmonic Distortion

17.172 Selection

Referenced by:

- HMI . Menu language

Selection	Description
English	English
German	German
Russian	Russian
Polish	Polish
French	French
Portuguese	Portuguese
Spanish	Spanish
Romanian	Romanian

17.173 Options

Referenced by:

- Sys . DM version

	Description
3.11.a	Version

17.174 1..n, PSS

Referenced by:

- Sys . PS1: activated by

1..n, PSS	Description
-	No assignment
Alarm	Signal: Alarm Voltage Transformer Measuring Circuit Supervision
DI 1	Signal: Digital Input
DI 2	Signal: Digital Input
DI 3	Signal: Digital Input
DI 4	Signal: Digital Input
DI 5	Signal: Digital Input
DI 6	Signal: Digital Input
DI 7	Signal: Digital Input
DI 8	Signal: Digital Input
LE1.Gate Out	Signal: Output of the logic gate
LE1.Timer Out	Signal: Timer Output
LE1.Out	Signal: Latched Output (Q)
LE1.Out inverted	Signal: Negated Latched Output (Q NOT)
LE2.Gate Out	Signal: Output of the logic gate
LE2.Timer Out	Signal: Timer Output
LE2.Out	Signal: Latched Output (Q)
LE2.Out inverted	Signal: Negated Latched Output (Q NOT)
LE3.Gate Out	Signal: Output of the logic gate
LE3.Timer Out	Signal: Timer Output
LE3.Out	Signal: Latched Output (Q)
LE3.Out inverted	Signal: Negated Latched Output (Q NOT)
LE4.Gate Out	Signal: Output of the logic gate
LE4.Timer Out	Signal: Timer Output
LE4.Out	Signal: Latched Output (Q)
LE4.Out inverted	Signal: Negated Latched Output (Q NOT)

1..n, PSS	Description
LE5.Gate Out	Signal: Output of the logic gate
LE5.Timer Out	Signal: Timer Output
LE5.Out	Signal: Latched Output (Q)
LE5.Out inverted	Signal: Negated Latched Output (Q NOT)
LE6.Gate Out	Signal: Output of the logic gate
LE6.Timer Out	Signal: Timer Output
LE6.Out	Signal: Latched Output (Q)
LE6.Out inverted	Signal: Negated Latched Output (Q NOT)
LE7.Gate Out	Signal: Output of the logic gate
LE7.Timer Out	Signal: Timer Output
LE7.Out	Signal: Latched Output (Q)
LE7.Out inverted	Signal: Negated Latched Output (Q NOT)
LE8.Gate Out	Signal: Output of the logic gate
LE8.Timer Out	Signal: Timer Output
LE8.Out	Signal: Latched Output (Q)
LE8.Out inverted	Signal: Negated Latched Output (Q NOT)
LE9.Gate Out	Signal: Output of the logic gate
LE9.Timer Out	Signal: Timer Output
LE9.Out	Signal: Latched Output (Q)
LE9.Out inverted	Signal: Negated Latched Output (Q NOT)
LE10.Gate Out	Signal: Output of the logic gate
LE10.Timer Out	Signal: Timer Output
LE10.Out	Signal: Latched Output (Q)
LE10.Out inverted	Signal: Negated Latched Output (Q NOT)
LE11.Gate Out	Signal: Output of the logic gate
LE11.Timer Out	Signal: Timer Output
LE11.Out	Signal: Latched Output (Q)
LE11.Out inverted	Signal: Negated Latched Output (Q NOT)
LE12.Gate Out	Signal: Output of the logic gate
LE12.Timer Out	Signal: Timer Output
LE12.Out	Signal: Latched Output (Q)
LE12.Out inverted	Signal: Negated Latched Output (Q NOT)
LE13.Gate Out	Signal: Output of the logic gate
LE13.Timer Out	Signal: Timer Output
LE13.Out	Signal: Latched Output (Q)
LE13.Out inverted	Signal: Negated Latched Output (Q NOT)
LE14.Gate Out	Signal: Output of the logic gate
LE14.Timer Out	Signal: Timer Output

1..n, PSS	Description
LE14.Out	Signal: Latched Output (Q)
LE14.Out inverted	Signal: Negated Latched Output (Q NOT)
LE15.Gate Out	Signal: Output of the logic gate
LE15.Timer Out	Signal: Timer Output
LE15.Out	Signal: Latched Output (Q)
LE15.Out inverted	Signal: Negated Latched Output (Q NOT)
LE16.Gate Out	Signal: Output of the logic gate
LE16.Timer Out	Signal: Timer Output
LE16.Out	Signal: Latched Output (Q)
LE16.Out inverted	Signal: Negated Latched Output (Q NOT)
LE17.Gate Out	Signal: Output of the logic gate
LE17.Timer Out	Signal: Timer Output
LE17.Out	Signal: Latched Output (Q)
LE17.Out inverted	Signal: Negated Latched Output (Q NOT)
LE18.Gate Out	Signal: Output of the logic gate
LE18.Timer Out	Signal: Timer Output
LE18.Out	Signal: Latched Output (Q)
LE18.Out inverted	Signal: Negated Latched Output (Q NOT)
LE19.Gate Out	Signal: Output of the logic gate
LE19.Timer Out	Signal: Timer Output
LE19.Out	Signal: Latched Output (Q)
LE19.Out inverted	Signal: Negated Latched Output (Q NOT)
LE20.Gate Out	Signal: Output of the logic gate
LE20.Timer Out	Signal: Timer Output
LE20.Out	Signal: Latched Output (Q)
LE20.Out inverted	Signal: Negated Latched Output (Q NOT)
LE21.Gate Out	Signal: Output of the logic gate
LE21.Timer Out	Signal: Timer Output
LE21.Out	Signal: Latched Output (Q)
LE21.Out inverted	Signal: Negated Latched Output (Q NOT)
LE22.Gate Out	Signal: Output of the logic gate
LE22.Timer Out	Signal: Timer Output
LE22.Out	Signal: Latched Output (Q)
LE22.Out inverted	Signal: Negated Latched Output (Q NOT)
LE23.Gate Out	Signal: Output of the logic gate
LE23.Timer Out	Signal: Timer Output
LE23.Out	Signal: Latched Output (Q)
LE23.Out inverted	Signal: Negated Latched Output (Q NOT)

1..n, PSS	Description
LE24.Gate Out	Signal: Output of the logic gate
LE24.Timer Out	Signal: Timer Output
LE24.Out	Signal: Latched Output (Q)
LE24.Out inverted	Signal: Negated Latched Output (Q NOT)
LE25.Gate Out	Signal: Output of the logic gate
LE25.Timer Out	Signal: Timer Output
LE25.Out	Signal: Latched Output (Q)
LE25.Out inverted	Signal: Negated Latched Output (Q NOT)
LE26.Gate Out	Signal: Output of the logic gate
LE26.Timer Out	Signal: Timer Output
LE26.Out	Signal: Latched Output (Q)
LE26.Out inverted	Signal: Negated Latched Output (Q NOT)
LE27.Gate Out	Signal: Output of the logic gate
LE27.Timer Out	Signal: Timer Output
LE27.Out	Signal: Latched Output (Q)
LE27.Out inverted	Signal: Negated Latched Output (Q NOT)
LE28.Gate Out	Signal: Output of the logic gate
LE28.Timer Out	Signal: Timer Output
LE28.Out	Signal: Latched Output (Q)
LE28.Out inverted	Signal: Negated Latched Output (Q NOT)
LE29.Gate Out	Signal: Output of the logic gate
LE29.Timer Out	Signal: Timer Output
LE29.Out	Signal: Latched Output (Q)
LE29.Out inverted	Signal: Negated Latched Output (Q NOT)
LE30.Gate Out	Signal: Output of the logic gate
LE30.Timer Out	Signal: Timer Output
LE30.Out	Signal: Latched Output (Q)
LE30.Out inverted	Signal: Negated Latched Output (Q NOT)
LE31.Gate Out	Signal: Output of the logic gate
LE31.Timer Out	Signal: Timer Output
LE31.Out	Signal: Latched Output (Q)
LE31.Out inverted	Signal: Negated Latched Output (Q NOT)
LE32.Gate Out	Signal: Output of the logic gate
LE32.Timer Out	Signal: Timer Output
LE32.Out	Signal: Latched Output (Q)
LE32.Out inverted	Signal: Negated Latched Output (Q NOT)
LE33.Gate Out	Signal: Output of the logic gate
LE33.Timer Out	Signal: Timer Output

1..n, PSS	Description
LE33.Out	Signal: Latched Output (Q)
LE33.Out inverted	Signal: Negated Latched Output (Q NOT)
LE34.Gate Out	Signal: Output of the logic gate
LE34.Timer Out	Signal: Timer Output
LE34.Out	Signal: Latched Output (Q)
LE34.Out inverted	Signal: Negated Latched Output (Q NOT)
LE35.Gate Out	Signal: Output of the logic gate
LE35.Timer Out	Signal: Timer Output
LE35.Out	Signal: Latched Output (Q)
LE35.Out inverted	Signal: Negated Latched Output (Q NOT)
LE36.Gate Out	Signal: Output of the logic gate
LE36.Timer Out	Signal: Timer Output
LE36.Out	Signal: Latched Output (Q)
LE36.Out inverted	Signal: Negated Latched Output (Q NOT)
LE37.Gate Out	Signal: Output of the logic gate
LE37.Timer Out	Signal: Timer Output
LE37.Out	Signal: Latched Output (Q)
LE37.Out inverted	Signal: Negated Latched Output (Q NOT)
LE38.Gate Out	Signal: Output of the logic gate
LE38.Timer Out	Signal: Timer Output
LE38.Out	Signal: Latched Output (Q)
LE38.Out inverted	Signal: Negated Latched Output (Q NOT)
LE39.Gate Out	Signal: Output of the logic gate
LE39.Timer Out	Signal: Timer Output
LE39.Out	Signal: Latched Output (Q)
LE39.Out inverted	Signal: Negated Latched Output (Q NOT)
LE40.Gate Out	Signal: Output of the logic gate
LE40.Timer Out	Signal: Timer Output
LE40.Out	Signal: Latched Output (Q)
LE40.Out inverted	Signal: Negated Latched Output (Q NOT)
LE41.Gate Out	Signal: Output of the logic gate
LE41.Timer Out	Signal: Timer Output
LE41.Out	Signal: Latched Output (Q)
LE41.Out inverted	Signal: Negated Latched Output (Q NOT)
LE42.Gate Out	Signal: Output of the logic gate
LE42.Timer Out	Signal: Timer Output
LE42.Out	Signal: Latched Output (Q)
LE42.Out inverted	Signal: Negated Latched Output (Q NOT)

1..n, PSS	Description
LE43.Gate Out	Signal: Output of the logic gate
LE43.Timer Out	Signal: Timer Output
LE43.Out	Signal: Latched Output (Q)
LE43.Out inverted	Signal: Negated Latched Output (Q NOT)
LE44.Gate Out	Signal: Output of the logic gate
LE44.Timer Out	Signal: Timer Output
LE44.Out	Signal: Latched Output (Q)
LE44.Out inverted	Signal: Negated Latched Output (Q NOT)
LE45.Gate Out	Signal: Output of the logic gate
LE45.Timer Out	Signal: Timer Output
LE45.Out	Signal: Latched Output (Q)
LE45.Out inverted	Signal: Negated Latched Output (Q NOT)
LE46.Gate Out	Signal: Output of the logic gate
LE46.Timer Out	Signal: Timer Output
LE46.Out	Signal: Latched Output (Q)
LE46.Out inverted	Signal: Negated Latched Output (Q NOT)
LE47.Gate Out	Signal: Output of the logic gate
LE47.Timer Out	Signal: Timer Output
LE47.Out	Signal: Latched Output (Q)
LE47.Out inverted	Signal: Negated Latched Output (Q NOT)
LE48.Gate Out	Signal: Output of the logic gate
LE48.Timer Out	Signal: Timer Output
LE48.Out	Signal: Latched Output (Q)
LE48.Out inverted	Signal: Negated Latched Output (Q NOT)
LE49.Gate Out	Signal: Output of the logic gate
LE49.Timer Out	Signal: Timer Output
LE49.Out	Signal: Latched Output (Q)
LE49.Out inverted	Signal: Negated Latched Output (Q NOT)
LE50.Gate Out	Signal: Output of the logic gate
LE50.Timer Out	Signal: Timer Output
LE50.Out	Signal: Latched Output (Q)
LE50.Out inverted	Signal: Negated Latched Output (Q NOT)
LE51.Gate Out	Signal: Output of the logic gate
LE51.Timer Out	Signal: Timer Output
LE51.Out	Signal: Latched Output (Q)
LE51.Out inverted	Signal: Negated Latched Output (Q NOT)
LE52.Gate Out	Signal: Output of the logic gate
LE52.Timer Out	Signal: Timer Output

1..n, PSS	Description
LE52.Out	Signal: Latched Output (Q)
LE52.Out inverted	Signal: Negated Latched Output (Q NOT)
LE53.Gate Out	Signal: Output of the logic gate
LE53.Timer Out	Signal: Timer Output
LE53.Out	Signal: Latched Output (Q)
LE53.Out inverted	Signal: Negated Latched Output (Q NOT)
LE54.Gate Out	Signal: Output of the logic gate
LE54.Timer Out	Signal: Timer Output
LE54.Out	Signal: Latched Output (Q)
LE54.Out inverted	Signal: Negated Latched Output (Q NOT)
LE55.Gate Out	Signal: Output of the logic gate
LE55.Timer Out	Signal: Timer Output
LE55.Out	Signal: Latched Output (Q)
LE55.Out inverted	Signal: Negated Latched Output (Q NOT)
LE56.Gate Out	Signal: Output of the logic gate
LE56.Timer Out	Signal: Timer Output
LE56.Out	Signal: Latched Output (Q)
LE56.Out inverted	Signal: Negated Latched Output (Q NOT)
LE57.Gate Out	Signal: Output of the logic gate
LE57.Timer Out	Signal: Timer Output
LE57.Out	Signal: Latched Output (Q)
LE57.Out inverted	Signal: Negated Latched Output (Q NOT)
LE58.Gate Out	Signal: Output of the logic gate
LE58.Timer Out	Signal: Timer Output
LE58.Out	Signal: Latched Output (Q)
LE58.Out inverted	Signal: Negated Latched Output (Q NOT)
LE59.Gate Out	Signal: Output of the logic gate
LE59.Timer Out	Signal: Timer Output
LE59.Out	Signal: Latched Output (Q)
LE59.Out inverted	Signal: Negated Latched Output (Q NOT)
LE60.Gate Out	Signal: Output of the logic gate
LE60.Timer Out	Signal: Timer Output
LE60.Out	Signal: Latched Output (Q)
LE60.Out inverted	Signal: Negated Latched Output (Q NOT)
LE61.Gate Out	Signal: Output of the logic gate
LE61.Timer Out	Signal: Timer Output
LE61.Out	Signal: Latched Output (Q)
LE61.Out inverted	Signal: Negated Latched Output (Q NOT)

1..n, PSS	Description
LE62.Gate Out	Signal: Output of the logic gate
LE62.Timer Out	Signal: Timer Output
LE62.Out	Signal: Latched Output (Q)
LE62.Out inverted	Signal: Negated Latched Output (Q NOT)
LE63.Gate Out	Signal: Output of the logic gate
LE63.Timer Out	Signal: Timer Output
LE63.Out	Signal: Latched Output (Q)
LE63.Out inverted	Signal: Negated Latched Output (Q NOT)
LE64.Gate Out	Signal: Output of the logic gate
LE64.Timer Out	Signal: Timer Output
LE64.Out	Signal: Latched Output (Q)
LE64.Out inverted	Signal: Negated Latched Output (Q NOT)
LE65.Gate Out	Signal: Output of the logic gate
LE65.Timer Out	Signal: Timer Output
LE65.Out	Signal: Latched Output (Q)
LE65.Out inverted	Signal: Negated Latched Output (Q NOT)
LE66.Gate Out	Signal: Output of the logic gate
LE66.Timer Out	Signal: Timer Output
LE66.Out	Signal: Latched Output (Q)
LE66.Out inverted	Signal: Negated Latched Output (Q NOT)
LE67.Gate Out	Signal: Output of the logic gate
LE67.Timer Out	Signal: Timer Output
LE67.Out	Signal: Latched Output (Q)
LE67.Out inverted	Signal: Negated Latched Output (Q NOT)
LE68.Gate Out	Signal: Output of the logic gate
LE68.Timer Out	Signal: Timer Output
LE68.Out	Signal: Latched Output (Q)
LE68.Out inverted	Signal: Negated Latched Output (Q NOT)
LE69.Gate Out	Signal: Output of the logic gate
LE69.Timer Out	Signal: Timer Output
LE69.Out	Signal: Latched Output (Q)
LE69.Out inverted	Signal: Negated Latched Output (Q NOT)
LE70.Gate Out	Signal: Output of the logic gate
LE70.Timer Out	Signal: Timer Output
LE70.Out	Signal: Latched Output (Q)
LE70.Out inverted	Signal: Negated Latched Output (Q NOT)
LE71.Gate Out	Signal: Output of the logic gate
LE71.Timer Out	Signal: Timer Output

1..n, PSS	Description
LE71.Out	Signal: Latched Output (Q)
LE71.Out inverted	Signal: Negated Latched Output (Q NOT)
LE72.Gate Out	Signal: Output of the logic gate
LE72.Timer Out	Signal: Timer Output
LE72.Out	Signal: Latched Output (Q)
LE72.Out inverted	Signal: Negated Latched Output (Q NOT)
LE73.Gate Out	Signal: Output of the logic gate
LE73.Timer Out	Signal: Timer Output
LE73.Out	Signal: Latched Output (Q)
LE73.Out inverted	Signal: Negated Latched Output (Q NOT)
LE74.Gate Out	Signal: Output of the logic gate
LE74.Timer Out	Signal: Timer Output
LE74.Out	Signal: Latched Output (Q)
LE74.Out inverted	Signal: Negated Latched Output (Q NOT)
LE75.Gate Out	Signal: Output of the logic gate
LE75.Timer Out	Signal: Timer Output
LE75.Out	Signal: Latched Output (Q)
LE75.Out inverted	Signal: Negated Latched Output (Q NOT)
LE76.Gate Out	Signal: Output of the logic gate
LE76.Timer Out	Signal: Timer Output
LE76.Out	Signal: Latched Output (Q)
LE76.Out inverted	Signal: Negated Latched Output (Q NOT)
LE77.Gate Out	Signal: Output of the logic gate
LE77.Timer Out	Signal: Timer Output
LE77.Out	Signal: Latched Output (Q)
LE77.Out inverted	Signal: Negated Latched Output (Q NOT)
LE78.Gate Out	Signal: Output of the logic gate
LE78.Timer Out	Signal: Timer Output
LE78.Out	Signal: Latched Output (Q)
LE78.Out inverted	Signal: Negated Latched Output (Q NOT)
LE79.Gate Out	Signal: Output of the logic gate
LE79.Timer Out	Signal: Timer Output
LE79.Out	Signal: Latched Output (Q)
LE79.Out inverted	Signal: Negated Latched Output (Q NOT)
LE80.Gate Out	Signal: Output of the logic gate
LE80.Timer Out	Signal: Timer Output
LE80.Out	Signal: Latched Output (Q)
LE80.Out inverted	Signal: Negated Latched Output (Q NOT)

1..n, PSS	Description
Maint Mode Active	Signal: Arc Flash Reduction Maintenance Active
Maint Mode Inactive	Signal: Arc Flash Reduction Maintenance Inactive

17.175 Trigger

Referenced by:

- CBF . Trigger1

Trigger	Description
-	No assignment
TripCmd	Signal: Trip Command
TripCmd	Signal: Trip Command
TripCmd	Signal: Trip Command
TripCmd	Signal: Trip Command
TripCmd	Signal: Trip Command
TripCmd	Signal: Trip Command
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TripCmd	Signal: Trip Command
TripCmd	Signal: Trip Command
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TripCmd	Signal: Trip Command
TripCmd	Signal: Trip Command

Trigger	Description
TripCmd	Signal: Trip Command
DI 1	Signal: Digital Input
DI 2	Signal: Digital Input
DI 3	Signal: Digital Input
DI 4	Signal: Digital Input
DI 5	Signal: Digital Input
DI 6	Signal: Digital Input
DI 7	Signal: Digital Input
DI 8	Signal: Digital Input
LE1.Gate Out	Signal: Output of the logic gate
LE1.Timer Out	Signal: Timer Output
LE1.Out	Signal: Latched Output (Q)
LE1.Out inverted	Signal: Negated Latched Output (Q NOT)
LE2.Gate Out	Signal: Output of the logic gate
LE2.Timer Out	Signal: Timer Output
LE2.Out	Signal: Latched Output (Q)
LE2.Out inverted	Signal: Negated Latched Output (Q NOT)
LE3.Gate Out	Signal: Output of the logic gate
LE3.Timer Out	Signal: Timer Output
LE3.Out	Signal: Latched Output (Q)
LE3.Out inverted	Signal: Negated Latched Output (Q NOT)
LE4.Gate Out	Signal: Output of the logic gate
LE4.Timer Out	Signal: Timer Output
LE4.Out	Signal: Latched Output (Q)
LE4.Out inverted	Signal: Negated Latched Output (Q NOT)
LE5.Gate Out	Signal: Output of the logic gate
LE5.Timer Out	Signal: Timer Output
LE5.Out	Signal: Latched Output (Q)
LE5.Out inverted	Signal: Negated Latched Output (Q NOT)
LE6.Gate Out	Signal: Output of the logic gate
LE6.Timer Out	Signal: Timer Output
LE6.Out	Signal: Latched Output (Q)
LE6.Out inverted	Signal: Negated Latched Output (Q NOT)
LE7.Gate Out	Signal: Output of the logic gate
LE7.Timer Out	Signal: Timer Output
LE7.Out	Signal: Latched Output (Q)
LE7.Out inverted	Signal: Negated Latched Output (Q NOT)
LE8.Gate Out	Signal: Output of the logic gate

Trigger	Description
LE8.Timer Out	Signal: Timer Output
LE8.Out	Signal: Latched Output (Q)
LE8.Out inverted	Signal: Negated Latched Output (Q NOT)
LE9.Gate Out	Signal: Output of the logic gate
LE9.Timer Out	Signal: Timer Output
LE9.Out	Signal: Latched Output (Q)
LE9.Out inverted	Signal: Negated Latched Output (Q NOT)
LE10.Gate Out	Signal: Output of the logic gate
LE10.Timer Out	Signal: Timer Output
LE10.Out	Signal: Latched Output (Q)
LE10.Out inverted	Signal: Negated Latched Output (Q NOT)
LE11.Gate Out	Signal: Output of the logic gate
LE11.Timer Out	Signal: Timer Output
LE11.Out	Signal: Latched Output (Q)
LE11.Out inverted	Signal: Negated Latched Output (Q NOT)
LE12.Gate Out	Signal: Output of the logic gate
LE12.Timer Out	Signal: Timer Output
LE12.Out	Signal: Latched Output (Q)
LE12.Out inverted	Signal: Negated Latched Output (Q NOT)
LE13.Gate Out	Signal: Output of the logic gate
LE13.Timer Out	Signal: Timer Output
LE13.Out	Signal: Latched Output (Q)
LE13.Out inverted	Signal: Negated Latched Output (Q NOT)
LE14.Gate Out	Signal: Output of the logic gate
LE14.Timer Out	Signal: Timer Output
LE14.Out	Signal: Latched Output (Q)
LE14.Out inverted	Signal: Negated Latched Output (Q NOT)
LE15.Gate Out	Signal: Output of the logic gate
LE15.Timer Out	Signal: Timer Output
LE15.Out	Signal: Latched Output (Q)
LE15.Out inverted	Signal: Negated Latched Output (Q NOT)
LE16.Gate Out	Signal: Output of the logic gate
LE16.Timer Out	Signal: Timer Output
LE16.Out	Signal: Latched Output (Q)
LE16.Out inverted	Signal: Negated Latched Output (Q NOT)
LE17.Gate Out	Signal: Output of the logic gate
LE17.Timer Out	Signal: Timer Output
LE17.Out	Signal: Latched Output (Q)

Trigger	Description
LE17.Out inverted	Signal: Negated Latched Output (Q NOT)
LE18.Gate Out	Signal: Output of the logic gate
LE18.Timer Out	Signal: Timer Output
LE18.Out	Signal: Latched Output (Q)
LE18.Out inverted	Signal: Negated Latched Output (Q NOT)
LE19.Gate Out	Signal: Output of the logic gate
LE19.Timer Out	Signal: Timer Output
LE19.Out	Signal: Latched Output (Q)
LE19.Out inverted	Signal: Negated Latched Output (Q NOT)
LE20.Gate Out	Signal: Output of the logic gate
LE20.Timer Out	Signal: Timer Output
LE20.Out	Signal: Latched Output (Q)
LE20.Out inverted	Signal: Negated Latched Output (Q NOT)
LE21.Gate Out	Signal: Output of the logic gate
LE21.Timer Out	Signal: Timer Output
LE21.Out	Signal: Latched Output (Q)
LE21.Out inverted	Signal: Negated Latched Output (Q NOT)
LE22.Gate Out	Signal: Output of the logic gate
LE22.Timer Out	Signal: Timer Output
LE22.Out	Signal: Latched Output (Q)
LE22.Out inverted	Signal: Negated Latched Output (Q NOT)
LE23.Gate Out	Signal: Output of the logic gate
LE23.Timer Out	Signal: Timer Output
LE23.Out	Signal: Latched Output (Q)
LE23.Out inverted	Signal: Negated Latched Output (Q NOT)
LE24.Gate Out	Signal: Output of the logic gate
LE24.Timer Out	Signal: Timer Output
LE24.Out	Signal: Latched Output (Q)
LE24.Out inverted	Signal: Negated Latched Output (Q NOT)
LE25.Gate Out	Signal: Output of the logic gate
LE25.Timer Out	Signal: Timer Output
LE25.Out	Signal: Latched Output (Q)
LE25.Out inverted	Signal: Negated Latched Output (Q NOT)
LE26.Gate Out	Signal: Output of the logic gate
LE26.Timer Out	Signal: Timer Output
LE26.Out	Signal: Latched Output (Q)
LE26.Out inverted	Signal: Negated Latched Output (Q NOT)
LE27.Gate Out	Signal: Output of the logic gate

Trigger	Description
LE27.Timer Out	Signal: Timer Output
LE27.Out	Signal: Latched Output (Q)
LE27.Out inverted	Signal: Negated Latched Output (Q NOT)
LE28.Gate Out	Signal: Output of the logic gate
LE28.Timer Out	Signal: Timer Output
LE28.Out	Signal: Latched Output (Q)
LE28.Out inverted	Signal: Negated Latched Output (Q NOT)
LE29.Gate Out	Signal: Output of the logic gate
LE29.Timer Out	Signal: Timer Output
LE29.Out	Signal: Latched Output (Q)
LE29.Out inverted	Signal: Negated Latched Output (Q NOT)
LE30.Gate Out	Signal: Output of the logic gate
LE30.Timer Out	Signal: Timer Output
LE30.Out	Signal: Latched Output (Q)
LE30.Out inverted	Signal: Negated Latched Output (Q NOT)
LE31.Gate Out	Signal: Output of the logic gate
LE31.Timer Out	Signal: Timer Output
LE31.Out	Signal: Latched Output (Q)
LE31.Out inverted	Signal: Negated Latched Output (Q NOT)
LE32.Gate Out	Signal: Output of the logic gate
LE32.Timer Out	Signal: Timer Output
LE32.Out	Signal: Latched Output (Q)
LE32.Out inverted	Signal: Negated Latched Output (Q NOT)
LE33.Gate Out	Signal: Output of the logic gate
LE33.Timer Out	Signal: Timer Output
LE33.Out	Signal: Latched Output (Q)
LE33.Out inverted	Signal: Negated Latched Output (Q NOT)
LE34.Gate Out	Signal: Output of the logic gate
LE34.Timer Out	Signal: Timer Output
LE34.Out	Signal: Latched Output (Q)
LE34.Out inverted	Signal: Negated Latched Output (Q NOT)
LE35.Gate Out	Signal: Output of the logic gate
LE35.Timer Out	Signal: Timer Output
LE35.Out	Signal: Latched Output (Q)
LE35.Out inverted	Signal: Negated Latched Output (Q NOT)
LE36.Gate Out	Signal: Output of the logic gate
LE36.Timer Out	Signal: Timer Output
LE36.Out	Signal: Latched Output (Q)

Trigger	Description
LE36.Out inverted	Signal: Negated Latched Output (Q NOT)
LE37.Gate Out	Signal: Output of the logic gate
LE37.Timer Out	Signal: Timer Output
LE37.Out	Signal: Latched Output (Q)
LE37.Out inverted	Signal: Negated Latched Output (Q NOT)
LE38.Gate Out	Signal: Output of the logic gate
LE38.Timer Out	Signal: Timer Output
LE38.Out	Signal: Latched Output (Q)
LE38.Out inverted	Signal: Negated Latched Output (Q NOT)
LE39.Gate Out	Signal: Output of the logic gate
LE39.Timer Out	Signal: Timer Output
LE39.Out	Signal: Latched Output (Q)
LE39.Out inverted	Signal: Negated Latched Output (Q NOT)
LE40.Gate Out	Signal: Output of the logic gate
LE40.Timer Out	Signal: Timer Output
LE40.Out	Signal: Latched Output (Q)
LE40.Out inverted	Signal: Negated Latched Output (Q NOT)
LE41.Gate Out	Signal: Output of the logic gate
LE41.Timer Out	Signal: Timer Output
LE41.Out	Signal: Latched Output (Q)
LE41.Out inverted	Signal: Negated Latched Output (Q NOT)
LE42.Gate Out	Signal: Output of the logic gate
LE42.Timer Out	Signal: Timer Output
LE42.Out	Signal: Latched Output (Q)
LE42.Out inverted	Signal: Negated Latched Output (Q NOT)
LE43.Gate Out	Signal: Output of the logic gate
LE43.Timer Out	Signal: Timer Output
LE43.Out	Signal: Latched Output (Q)
LE43.Out inverted	Signal: Negated Latched Output (Q NOT)
LE44.Gate Out	Signal: Output of the logic gate
LE44.Timer Out	Signal: Timer Output
LE44.Out	Signal: Latched Output (Q)
LE44.Out inverted	Signal: Negated Latched Output (Q NOT)
LE45.Gate Out	Signal: Output of the logic gate
LE45.Timer Out	Signal: Timer Output
LE45.Out	Signal: Latched Output (Q)
LE45.Out inverted	Signal: Negated Latched Output (Q NOT)
LE46.Gate Out	Signal: Output of the logic gate

Trigger	Description
LE46.Timer Out	Signal: Timer Output
LE46.Out	Signal: Latched Output (Q)
LE46.Out inverted	Signal: Negated Latched Output (Q NOT)
LE47.Gate Out	Signal: Output of the logic gate
LE47.Timer Out	Signal: Timer Output
LE47.Out	Signal: Latched Output (Q)
LE47.Out inverted	Signal: Negated Latched Output (Q NOT)
LE48.Gate Out	Signal: Output of the logic gate
LE48.Timer Out	Signal: Timer Output
LE48.Out	Signal: Latched Output (Q)
LE48.Out inverted	Signal: Negated Latched Output (Q NOT)
LE49.Gate Out	Signal: Output of the logic gate
LE49.Timer Out	Signal: Timer Output
LE49.Out	Signal: Latched Output (Q)
LE49.Out inverted	Signal: Negated Latched Output (Q NOT)
LE50.Gate Out	Signal: Output of the logic gate
LE50.Timer Out	Signal: Timer Output
LE50.Out	Signal: Latched Output (Q)
LE50.Out inverted	Signal: Negated Latched Output (Q NOT)
LE51.Gate Out	Signal: Output of the logic gate
LE51.Timer Out	Signal: Timer Output
LE51.Out	Signal: Latched Output (Q)
LE51.Out inverted	Signal: Negated Latched Output (Q NOT)
LE52.Gate Out	Signal: Output of the logic gate
LE52.Timer Out	Signal: Timer Output
LE52.Out	Signal: Latched Output (Q)
LE52.Out inverted	Signal: Negated Latched Output (Q NOT)
LE53.Gate Out	Signal: Output of the logic gate
LE53.Timer Out	Signal: Timer Output
LE53.Out	Signal: Latched Output (Q)
LE53.Out inverted	Signal: Negated Latched Output (Q NOT)
LE54.Gate Out	Signal: Output of the logic gate
LE54.Timer Out	Signal: Timer Output
LE54.Out	Signal: Latched Output (Q)
LE54.Out inverted	Signal: Negated Latched Output (Q NOT)
LE55.Gate Out	Signal: Output of the logic gate
LE55.Timer Out	Signal: Timer Output
LE55.Out	Signal: Latched Output (Q)

Trigger	Description
LE55.Out inverted	Signal: Negated Latched Output (Q NOT)
LE56.Gate Out	Signal: Output of the logic gate
LE56.Timer Out	Signal: Timer Output
LE56.Out	Signal: Latched Output (Q)
LE56.Out inverted	Signal: Negated Latched Output (Q NOT)
LE57.Gate Out	Signal: Output of the logic gate
LE57.Timer Out	Signal: Timer Output
LE57.Out	Signal: Latched Output (Q)
LE57.Out inverted	Signal: Negated Latched Output (Q NOT)
LE58.Gate Out	Signal: Output of the logic gate
LE58.Timer Out	Signal: Timer Output
LE58.Out	Signal: Latched Output (Q)
LE58.Out inverted	Signal: Negated Latched Output (Q NOT)
LE59.Gate Out	Signal: Output of the logic gate
LE59.Timer Out	Signal: Timer Output
LE59.Out	Signal: Latched Output (Q)
LE59.Out inverted	Signal: Negated Latched Output (Q NOT)
LE60.Gate Out	Signal: Output of the logic gate
LE60.Timer Out	Signal: Timer Output
LE60.Out	Signal: Latched Output (Q)
LE60.Out inverted	Signal: Negated Latched Output (Q NOT)
LE61.Gate Out	Signal: Output of the logic gate
LE61.Timer Out	Signal: Timer Output
LE61.Out	Signal: Latched Output (Q)
LE61.Out inverted	Signal: Negated Latched Output (Q NOT)
LE62.Gate Out	Signal: Output of the logic gate
LE62.Timer Out	Signal: Timer Output
LE62.Out	Signal: Latched Output (Q)
LE62.Out inverted	Signal: Negated Latched Output (Q NOT)
LE63.Gate Out	Signal: Output of the logic gate
LE63.Timer Out	Signal: Timer Output
LE63.Out	Signal: Latched Output (Q)
LE63.Out inverted	Signal: Negated Latched Output (Q NOT)
LE64.Gate Out	Signal: Output of the logic gate
LE64.Timer Out	Signal: Timer Output
LE64.Out	Signal: Latched Output (Q)
LE64.Out inverted	Signal: Negated Latched Output (Q NOT)
LE65.Gate Out	Signal: Output of the logic gate

Trigger	Description
LE65.Timer Out	Signal: Timer Output
LE65.Out	Signal: Latched Output (Q)
LE65.Out inverted	Signal: Negated Latched Output (Q NOT)
LE66.Gate Out	Signal: Output of the logic gate
LE66.Timer Out	Signal: Timer Output
LE66.Out	Signal: Latched Output (Q)
LE66.Out inverted	Signal: Negated Latched Output (Q NOT)
LE67.Gate Out	Signal: Output of the logic gate
LE67.Timer Out	Signal: Timer Output
LE67.Out	Signal: Latched Output (Q)
LE67.Out inverted	Signal: Negated Latched Output (Q NOT)
LE68.Gate Out	Signal: Output of the logic gate
LE68.Timer Out	Signal: Timer Output
LE68.Out	Signal: Latched Output (Q)
LE68.Out inverted	Signal: Negated Latched Output (Q NOT)
LE69.Gate Out	Signal: Output of the logic gate
LE69.Timer Out	Signal: Timer Output
LE69.Out	Signal: Latched Output (Q)
LE69.Out inverted	Signal: Negated Latched Output (Q NOT)
LE70.Gate Out	Signal: Output of the logic gate
LE70.Timer Out	Signal: Timer Output
LE70.Out	Signal: Latched Output (Q)
LE70.Out inverted	Signal: Negated Latched Output (Q NOT)
LE71.Gate Out	Signal: Output of the logic gate
LE71.Timer Out	Signal: Timer Output
LE71.Out	Signal: Latched Output (Q)
LE71.Out inverted	Signal: Negated Latched Output (Q NOT)
LE72.Gate Out	Signal: Output of the logic gate
LE72.Timer Out	Signal: Timer Output
LE72.Out	Signal: Latched Output (Q)
LE72.Out inverted	Signal: Negated Latched Output (Q NOT)
LE73.Gate Out	Signal: Output of the logic gate
LE73.Timer Out	Signal: Timer Output
LE73.Out	Signal: Latched Output (Q)
LE73.Out inverted	Signal: Negated Latched Output (Q NOT)
LE74.Gate Out	Signal: Output of the logic gate
LE74.Timer Out	Signal: Timer Output
LE74.Out	Signal: Latched Output (Q)

Trigger	Description
LE74.Out inverted	Signal: Negated Latched Output (Q NOT)
LE75.Gate Out	Signal: Output of the logic gate
LE75.Timer Out	Signal: Timer Output
LE75.Out	Signal: Latched Output (Q)
LE75.Out inverted	Signal: Negated Latched Output (Q NOT)
LE76.Gate Out	Signal: Output of the logic gate
LE76.Timer Out	Signal: Timer Output
LE76.Out	Signal: Latched Output (Q)
LE76.Out inverted	Signal: Negated Latched Output (Q NOT)
LE77.Gate Out	Signal: Output of the logic gate
LE77.Timer Out	Signal: Timer Output
LE77.Out	Signal: Latched Output (Q)
LE77.Out inverted	Signal: Negated Latched Output (Q NOT)
LE78.Gate Out	Signal: Output of the logic gate
LE78.Timer Out	Signal: Timer Output
LE78.Out	Signal: Latched Output (Q)
LE78.Out inverted	Signal: Negated Latched Output (Q NOT)
LE79.Gate Out	Signal: Output of the logic gate
LE79.Timer Out	Signal: Timer Output
LE79.Out	Signal: Latched Output (Q)
LE79.Out inverted	Signal: Negated Latched Output (Q NOT)
LE80.Gate Out	Signal: Output of the logic gate
LE80.Timer Out	Signal: Timer Output
LE80.Out	Signal: Latched Output (Q)
LE80.Out inverted	Signal: Negated Latched Output (Q NOT)

17.176 Decoupling Functions

Referenced by:

- ReCon[1] . Decoupling1
- *[...]*

Decoupling Functions	Description
-	No assignment
TripCmd	Signal: Trip Command
TripCmd	Signal: Trip Command
TripCmd	Signal: Trip Command
TripCmd	Signal: Trip Command

Decoupling Functions	Description
TripCmd	Signal: Trip Command
TripCmd	Signal: Trip Command
TripCmd	Signal: Trip Command
TripCmd	Signal: Trip Command
TripCmd	Signal: Trip Command
TripCmd	Signal: Trip Command
TripCmd	Signal: Trip Command
TripCmd	Signal: Trip Command
TripCmd	Signal: Trip Command
TripCmd	Signal: Trip Command
TripCmd	Signal: Trip Command
TripCmd	Signal: Trip Command
TripCmd	Signal: Trip Command
TripCmd	Signal: Trip Command
TripCmd	Signal: Trip Command
TripCmd	Signal: Trip Command
TripCmd	Signal: Trip Command
TripCmd	Signal: Trip Command
TripCmd	Signal: Trip Command
TripCmd	Signal: Trip Command
TripCmd	Signal: Trip Command
TripCmd	Signal: Trip Command
TripCmd	Signal: Trip Command
TripCmd	Signal: Trip Command
TripCmd	Signal: Trip Command
DI 1	Signal: Digital Input
DI 2	Signal: Digital Input
DI 3	Signal: Digital Input
DI 4	Signal: Digital Input
DI 5	Signal: Digital Input
DI 6	Signal: Digital Input
DI 7	Signal: Digital Input
DI 8	Signal: Digital Input
BinaryOutput0	Virtual Digital Output (DNP). This corresponds to a virtual binary input of the protective device.
BinaryOutput1	Virtual Digital Output (DNP). This corresponds to a virtual binary input of the protective device.
BinaryOutput2	Virtual Digital Output (DNP). This corresponds to a virtual binary input of the protective device.

Decoupling Functions	Description
BinaryOutput3	Virtual Digital Output (DNP). This corresponds to a virtual binary input of the protective device.
BinaryOutput4	Virtual Digital Output (DNP). This corresponds to a virtual binary input of the protective device.
BinaryOutput5	Virtual Digital Output (DNP). This corresponds to a virtual binary input of the protective device.
BinaryOutput6	Virtual Digital Output (DNP). This corresponds to a virtual binary input of the protective device.
BinaryOutput7	Virtual Digital Output (DNP). This corresponds to a virtual binary input of the protective device.
BinaryOutput8	Virtual Digital Output (DNP). This corresponds to a virtual binary input of the protective device.
BinaryOutput9	Virtual Digital Output (DNP). This corresponds to a virtual binary input of the protective device.
BinaryOutput10	Virtual Digital Output (DNP). This corresponds to a virtual binary input of the protective device.
BinaryOutput11	Virtual Digital Output (DNP). This corresponds to a virtual binary input of the protective device.
BinaryOutput12	Virtual Digital Output (DNP). This corresponds to a virtual binary input of the protective device.
BinaryOutput13	Virtual Digital Output (DNP). This corresponds to a virtual binary input of the protective device.
BinaryOutput14	Virtual Digital Output (DNP). This corresponds to a virtual binary input of the protective device.
BinaryOutput15	Virtual Digital Output (DNP). This corresponds to a virtual binary input of the protective device.
BinaryOutput16	Virtual Digital Output (DNP). This corresponds to a virtual binary input of the protective device.
BinaryOutput17	Virtual Digital Output (DNP). This corresponds to a virtual binary input of the protective device.
BinaryOutput18	Virtual Digital Output (DNP). This corresponds to a virtual binary input of the protective device.
BinaryOutput19	Virtual Digital Output (DNP). This corresponds to a virtual binary input of the protective device.
BinaryOutput20	Virtual Digital Output (DNP). This corresponds to a virtual binary input of the protective device.
BinaryOutput21	Virtual Digital Output (DNP). This corresponds to a virtual binary input of the protective device.
BinaryOutput22	Virtual Digital Output (DNP). This corresponds to a virtual binary input of the protective device.
BinaryOutput23	Virtual Digital Output (DNP). This corresponds to a virtual binary input of the protective device.
BinaryOutput24	Virtual Digital Output (DNP). This corresponds to a virtual binary input of the protective device.
BinaryOutput25	Virtual Digital Output (DNP). This corresponds to a virtual binary input of the protective device.
BinaryOutput26	Virtual Digital Output (DNP). This corresponds to a virtual binary input of the protective device.
BinaryOutput27	Virtual Digital Output (DNP). This corresponds to a virtual binary input of the protective device.

Decoupling Functions	Description
BinaryOutput28	Virtual Digital Output (DNP). This corresponds to a virtual binary input of the protective device.
BinaryOutput29	Virtual Digital Output (DNP). This corresponds to a virtual binary input of the protective device.
BinaryOutput30	Virtual Digital Output (DNP). This corresponds to a virtual binary input of the protective device.
BinaryOutput31	Virtual Digital Output (DNP). This corresponds to a virtual binary input of the protective device.
Scada Cmd 1	Scada Command
Scada Cmd 2	Scada Command
Scada Cmd 3	Scada Command
Scada Cmd 4	Scada Command
Scada Cmd 5	Scada Command
Scada Cmd 6	Scada Command
Scada Cmd 7	Scada Command
Scada Cmd 8	Scada Command
Scada Cmd 9	Scada Command
Scada Cmd 10	Scada Command
Scada Cmd 11	Scada Command
Scada Cmd 12	Scada Command
Scada Cmd 13	Scada Command
Scada Cmd 14	Scada Command
Scada Cmd 15	Scada Command
Scada Cmd 16	Scada Command
GOSINGGIO1.Ind1.stVal	Signal: Virtual Input (IEC61850 GGIO Ind): State
GOSINGGIO1.Ind2.stVal	Signal: Virtual Input (IEC61850 GGIO Ind): State
GOSINGGIO1.Ind3.stVal	Signal: Virtual Input (IEC61850 GGIO Ind): State
GOSINGGIO1.Ind4.stVal	Signal: Virtual Input (IEC61850 GGIO Ind): State
GOSINGGIO1.Ind5.stVal	Signal: Virtual Input (IEC61850 GGIO Ind): State
GOSINGGIO1.Ind6.stVal	Signal: Virtual Input (IEC61850 GGIO Ind): State
GOSINGGIO1.Ind7.stVal	Signal: Virtual Input (IEC61850 GGIO Ind): State
GOSINGGIO1.Ind8.stVal	Signal: Virtual Input (IEC61850 GGIO Ind): State
GOSINGGIO1.Ind9.stVal	Signal: Virtual Input (IEC61850 GGIO Ind): State
GOSINGGIO1.Ind10.stVal	Signal: Virtual Input (IEC61850 GGIO Ind): State
GOSINGGIO1.Ind11.stVal	Signal: Virtual Input (IEC61850 GGIO Ind): State
GOSINGGIO1.Ind12.stVal	Signal: Virtual Input (IEC61850 GGIO Ind): State
GOSINGGIO1.Ind13.stVal	Signal: Virtual Input (IEC61850 GGIO Ind): State
GOSINGGIO1.Ind14.stVal	Signal: Virtual Input (IEC61850 GGIO Ind): State
GOSINGGIO1.Ind15.stVal	Signal: Virtual Input (IEC61850 GGIO Ind): State
GOSINGGIO1.Ind16.stVal	Signal: Virtual Input (IEC61850 GGIO Ind): State

Decoupling Functions	Description
GOSINGGIO1.Ind17.stVal	Signal: Virtual Input (IEC61850 GGIO Ind): State
GOSINGGIO1.Ind18.stVal	Signal: Virtual Input (IEC61850 GGIO Ind): State
GOSINGGIO1.Ind19.stVal	Signal: Virtual Input (IEC61850 GGIO Ind): State
GOSINGGIO1.Ind20.stVal	Signal: Virtual Input (IEC61850 GGIO Ind): State
GOSINGGIO1.Ind21.stVal	Signal: Virtual Input (IEC61850 GGIO Ind): State
GOSINGGIO1.Ind22.stVal	Signal: Virtual Input (IEC61850 GGIO Ind): State
GOSINGGIO1.Ind23.stVal	Signal: Virtual Input (IEC61850 GGIO Ind): State
GOSINGGIO1.Ind24.stVal	Signal: Virtual Input (IEC61850 GGIO Ind): State
GOSINGGIO1.Ind25.stVal	Signal: Virtual Input (IEC61850 GGIO Ind): State
GOSINGGIO1.Ind26.stVal	Signal: Virtual Input (IEC61850 GGIO Ind): State
GOSINGGIO1.Ind27.stVal	Signal: Virtual Input (IEC61850 GGIO Ind): State
GOSINGGIO1.Ind28.stVal	Signal: Virtual Input (IEC61850 GGIO Ind): State
GOSINGGIO1.Ind29.stVal	Signal: Virtual Input (IEC61850 GGIO Ind): State
GOSINGGIO1.Ind30.stVal	Signal: Virtual Input (IEC61850 GGIO Ind): State
GOSINGGIO1.Ind31.stVal	Signal: Virtual Input (IEC61850 GGIO Ind): State
GOSINGGIO1.Ind32.stVal	Signal: Virtual Input (IEC61850 GGIO Ind): State
CTLGGIO1.SPCSO1.stVal	Status bit that can be set by clients like e.g. SCADA (Single Point Controllable Status Output).
CTLGGIO1.SPCSO2.stVal	Status bit that can be set by clients like e.g. SCADA (Single Point Controllable Status Output).
CTLGGIO1.SPCSO3.stVal	Status bit that can be set by clients like e.g. SCADA (Single Point Controllable Status Output).
CTLGGIO1.SPCSO4.stVal	Status bit that can be set by clients like e.g. SCADA (Single Point Controllable Status Output).
CTLGGIO1.SPCSO5.stVal	Status bit that can be set by clients like e.g. SCADA (Single Point Controllable Status Output).
CTLGGIO1.SPCSO6.stVal	Status bit that can be set by clients like e.g. SCADA (Single Point Controllable Status Output).
CTLGGIO1.SPCSO7.stVal	Status bit that can be set by clients like e.g. SCADA (Single Point Controllable Status Output).
CTLGGIO1.SPCSO8.stVal	Status bit that can be set by clients like e.g. SCADA (Single Point Controllable Status Output).
CTLGGIO1.SPCSO9.stVal	Status bit that can be set by clients like e.g. SCADA (Single Point Controllable Status Output).
CTLGGIO1.SPCSO10.stVal	Status bit that can be set by clients like e.g. SCADA (Single Point Controllable Status Output).
CTLGGIO1.SPCSO11.stVal	Status bit that can be set by clients like e.g. SCADA (Single Point Controllable Status Output).
CTLGGIO1.SPCSO12.stVal	Status bit that can be set by clients like e.g. SCADA (Single Point Controllable Status Output).
CTLGGIO1.SPCSO13.stVal	Status bit that can be set by clients like e.g. SCADA (Single Point Controllable Status Output).
CTLGGIO1.SPCSO14.stVal	Status bit that can be set by clients like e.g. SCADA (Single Point Controllable Status Output).

Decoupling Functions	Description
CTLGGIO1.SPCSO15.stVal	Status bit that can be set by clients like e.g. SCADA (Single Point Controllable Status Output).
CTLGGIO1.SPCSO16.stVal	Status bit that can be set by clients like e.g. SCADA (Single Point Controllable Status Output).
Scada Cmd 1	Scada Command
Scada Cmd 2	Scada Command
Scada Cmd 3	Scada Command
Scada Cmd 4	Scada Command
Scada Cmd 5	Scada Command
Scada Cmd 6	Scada Command
Scada Cmd 7	Scada Command
Scada Cmd 8	Scada Command
Scada Cmd 9	Scada Command
Scada Cmd 10	Scada Command
Scada Cmd 1	Scada Command
Scada Cmd 2	Scada Command
Scada Cmd 3	Scada Command
Scada Cmd 4	Scada Command
Scada Cmd 5	Scada Command
Scada Cmd 6	Scada Command
Scada Cmd 7	Scada Command
Scada Cmd 8	Scada Command
Scada Cmd 9	Scada Command
Scada Cmd 10	Scada Command
Scada Cmd 11	Scada Command
Scada Cmd 12	Scada Command
Scada Cmd 13	Scada Command
Scada Cmd 14	Scada Command
Scada Cmd 15	Scada Command
Scada Cmd 16	Scada Command
Scada Cmd 1	Scada Command
Scada Cmd 2	Scada Command
Scada Cmd 3	Scada Command
Scada Cmd 4	Scada Command
Scada Cmd 5	Scada Command
Scada Cmd 6	Scada Command
Scada Cmd 7	Scada Command
Scada Cmd 8	Scada Command
Scada Cmd 9	Scada Command

Decoupling Functions	Description
Scada Cmd 10	Scada Command
Scada Cmd 11	Scada Command
Scada Cmd 12	Scada Command
Scada Cmd 13	Scada Command
Scada Cmd 14	Scada Command
Scada Cmd 15	Scada Command
Scada Cmd 16	Scada Command
LE1.Gate Out	Signal: Output of the logic gate
LE1.Timer Out	Signal: Timer Output
LE1.Out	Signal: Latched Output (Q)
LE1.Out inverted	Signal: Negated Latched Output (Q NOT)
LE2.Gate Out	Signal: Output of the logic gate
LE2.Timer Out	Signal: Timer Output
LE2.Out	Signal: Latched Output (Q)
LE2.Out inverted	Signal: Negated Latched Output (Q NOT)
LE3.Gate Out	Signal: Output of the logic gate
LE3.Timer Out	Signal: Timer Output
LE3.Out	Signal: Latched Output (Q)
LE3.Out inverted	Signal: Negated Latched Output (Q NOT)
LE4.Gate Out	Signal: Output of the logic gate
LE4.Timer Out	Signal: Timer Output
LE4.Out	Signal: Latched Output (Q)
LE4.Out inverted	Signal: Negated Latched Output (Q NOT)
LE5.Gate Out	Signal: Output of the logic gate
LE5.Timer Out	Signal: Timer Output
LE5.Out	Signal: Latched Output (Q)
LE5.Out inverted	Signal: Negated Latched Output (Q NOT)
LE6.Gate Out	Signal: Output of the logic gate
LE6.Timer Out	Signal: Timer Output
LE6.Out	Signal: Latched Output (Q)
LE6.Out inverted	Signal: Negated Latched Output (Q NOT)
LE7.Gate Out	Signal: Output of the logic gate
LE7.Timer Out	Signal: Timer Output
LE7.Out	Signal: Latched Output (Q)
LE7.Out inverted	Signal: Negated Latched Output (Q NOT)
LE8.Gate Out	Signal: Output of the logic gate
LE8.Timer Out	Signal: Timer Output
LE8.Out	Signal: Latched Output (Q)

Decoupling Functions	Description
LE8.Out inverted	Signal: Negated Latched Output (Q NOT)
LE9.Gate Out	Signal: Output of the logic gate
LE9.Timer Out	Signal: Timer Output
LE9.Out	Signal: Latched Output (Q)
LE9.Out inverted	Signal: Negated Latched Output (Q NOT)
LE10.Gate Out	Signal: Output of the logic gate
LE10.Timer Out	Signal: Timer Output
LE10.Out	Signal: Latched Output (Q)
LE10.Out inverted	Signal: Negated Latched Output (Q NOT)
LE11.Gate Out	Signal: Output of the logic gate
LE11.Timer Out	Signal: Timer Output
LE11.Out	Signal: Latched Output (Q)
LE11.Out inverted	Signal: Negated Latched Output (Q NOT)
LE12.Gate Out	Signal: Output of the logic gate
LE12.Timer Out	Signal: Timer Output
LE12.Out	Signal: Latched Output (Q)
LE12.Out inverted	Signal: Negated Latched Output (Q NOT)
LE13.Gate Out	Signal: Output of the logic gate
LE13.Timer Out	Signal: Timer Output
LE13.Out	Signal: Latched Output (Q)
LE13.Out inverted	Signal: Negated Latched Output (Q NOT)
LE14.Gate Out	Signal: Output of the logic gate
LE14.Timer Out	Signal: Timer Output
LE14.Out	Signal: Latched Output (Q)
LE14.Out inverted	Signal: Negated Latched Output (Q NOT)
LE15.Gate Out	Signal: Output of the logic gate
LE15.Timer Out	Signal: Timer Output
LE15.Out	Signal: Latched Output (Q)
LE15.Out inverted	Signal: Negated Latched Output (Q NOT)
LE16.Gate Out	Signal: Output of the logic gate
LE16.Timer Out	Signal: Timer Output
LE16.Out	Signal: Latched Output (Q)
LE16.Out inverted	Signal: Negated Latched Output (Q NOT)
LE17.Gate Out	Signal: Output of the logic gate
LE17.Timer Out	Signal: Timer Output
LE17.Out	Signal: Latched Output (Q)
LE17.Out inverted	Signal: Negated Latched Output (Q NOT)
LE18.Gate Out	Signal: Output of the logic gate

Decoupling Functions	Description
LE18.Timer Out	Signal: Timer Output
LE18.Out	Signal: Latched Output (Q)
LE18.Out inverted	Signal: Negated Latched Output (Q NOT)
LE19.Gate Out	Signal: Output of the logic gate
LE19.Timer Out	Signal: Timer Output
LE19.Out	Signal: Latched Output (Q)
LE19.Out inverted	Signal: Negated Latched Output (Q NOT)
LE20.Gate Out	Signal: Output of the logic gate
LE20.Timer Out	Signal: Timer Output
LE20.Out	Signal: Latched Output (Q)
LE20.Out inverted	Signal: Negated Latched Output (Q NOT)
LE21.Gate Out	Signal: Output of the logic gate
LE21.Timer Out	Signal: Timer Output
LE21.Out	Signal: Latched Output (Q)
LE21.Out inverted	Signal: Negated Latched Output (Q NOT)
LE22.Gate Out	Signal: Output of the logic gate
LE22.Timer Out	Signal: Timer Output
LE22.Out	Signal: Latched Output (Q)
LE22.Out inverted	Signal: Negated Latched Output (Q NOT)
LE23.Gate Out	Signal: Output of the logic gate
LE23.Timer Out	Signal: Timer Output
LE23.Out	Signal: Latched Output (Q)
LE23.Out inverted	Signal: Negated Latched Output (Q NOT)
LE24.Gate Out	Signal: Output of the logic gate
LE24.Timer Out	Signal: Timer Output
LE24.Out	Signal: Latched Output (Q)
LE24.Out inverted	Signal: Negated Latched Output (Q NOT)
LE25.Gate Out	Signal: Output of the logic gate
LE25.Timer Out	Signal: Timer Output
LE25.Out	Signal: Latched Output (Q)
LE25.Out inverted	Signal: Negated Latched Output (Q NOT)
LE26.Gate Out	Signal: Output of the logic gate
LE26.Timer Out	Signal: Timer Output
LE26.Out	Signal: Latched Output (Q)
LE26.Out inverted	Signal: Negated Latched Output (Q NOT)
LE27.Gate Out	Signal: Output of the logic gate
LE27.Timer Out	Signal: Timer Output
LE27.Out	Signal: Latched Output (Q)

Decoupling Functions	Description
LE27.Out inverted	Signal: Negated Latched Output (Q NOT)
LE28.Gate Out	Signal: Output of the logic gate
LE28.Timer Out	Signal: Timer Output
LE28.Out	Signal: Latched Output (Q)
LE28.Out inverted	Signal: Negated Latched Output (Q NOT)
LE29.Gate Out	Signal: Output of the logic gate
LE29.Timer Out	Signal: Timer Output
LE29.Out	Signal: Latched Output (Q)
LE29.Out inverted	Signal: Negated Latched Output (Q NOT)
LE30.Gate Out	Signal: Output of the logic gate
LE30.Timer Out	Signal: Timer Output
LE30.Out	Signal: Latched Output (Q)
LE30.Out inverted	Signal: Negated Latched Output (Q NOT)
LE31.Gate Out	Signal: Output of the logic gate
LE31.Timer Out	Signal: Timer Output
LE31.Out	Signal: Latched Output (Q)
LE31.Out inverted	Signal: Negated Latched Output (Q NOT)
LE32.Gate Out	Signal: Output of the logic gate
LE32.Timer Out	Signal: Timer Output
LE32.Out	Signal: Latched Output (Q)
LE32.Out inverted	Signal: Negated Latched Output (Q NOT)
LE33.Gate Out	Signal: Output of the logic gate
LE33.Timer Out	Signal: Timer Output
LE33.Out	Signal: Latched Output (Q)
LE33.Out inverted	Signal: Negated Latched Output (Q NOT)
LE34.Gate Out	Signal: Output of the logic gate
LE34.Timer Out	Signal: Timer Output
LE34.Out	Signal: Latched Output (Q)
LE34.Out inverted	Signal: Negated Latched Output (Q NOT)
LE35.Gate Out	Signal: Output of the logic gate
LE35.Timer Out	Signal: Timer Output
LE35.Out	Signal: Latched Output (Q)
LE35.Out inverted	Signal: Negated Latched Output (Q NOT)
LE36.Gate Out	Signal: Output of the logic gate
LE36.Timer Out	Signal: Timer Output
LE36.Out	Signal: Latched Output (Q)
LE36.Out inverted	Signal: Negated Latched Output (Q NOT)
LE37.Gate Out	Signal: Output of the logic gate

Decoupling Functions	Description
LE37.Timer Out	Signal: Timer Output
LE37.Out	Signal: Latched Output (Q)
LE37.Out inverted	Signal: Negated Latched Output (Q NOT)
LE38.Gate Out	Signal: Output of the logic gate
LE38.Timer Out	Signal: Timer Output
LE38.Out	Signal: Latched Output (Q)
LE38.Out inverted	Signal: Negated Latched Output (Q NOT)
LE39.Gate Out	Signal: Output of the logic gate
LE39.Timer Out	Signal: Timer Output
LE39.Out	Signal: Latched Output (Q)
LE39.Out inverted	Signal: Negated Latched Output (Q NOT)
LE40.Gate Out	Signal: Output of the logic gate
LE40.Timer Out	Signal: Timer Output
LE40.Out	Signal: Latched Output (Q)
LE40.Out inverted	Signal: Negated Latched Output (Q NOT)
LE41.Gate Out	Signal: Output of the logic gate
LE41.Timer Out	Signal: Timer Output
LE41.Out	Signal: Latched Output (Q)
LE41.Out inverted	Signal: Negated Latched Output (Q NOT)
LE42.Gate Out	Signal: Output of the logic gate
LE42.Timer Out	Signal: Timer Output
LE42.Out	Signal: Latched Output (Q)
LE42.Out inverted	Signal: Negated Latched Output (Q NOT)
LE43.Gate Out	Signal: Output of the logic gate
LE43.Timer Out	Signal: Timer Output
LE43.Out	Signal: Latched Output (Q)
LE43.Out inverted	Signal: Negated Latched Output (Q NOT)
LE44.Gate Out	Signal: Output of the logic gate
LE44.Timer Out	Signal: Timer Output
LE44.Out	Signal: Latched Output (Q)
LE44.Out inverted	Signal: Negated Latched Output (Q NOT)
LE45.Gate Out	Signal: Output of the logic gate
LE45.Timer Out	Signal: Timer Output
LE45.Out	Signal: Latched Output (Q)
LE45.Out inverted	Signal: Negated Latched Output (Q NOT)
LE46.Gate Out	Signal: Output of the logic gate
LE46.Timer Out	Signal: Timer Output
LE46.Out	Signal: Latched Output (Q)

Decoupling Functions	Description
LE46.Out inverted	Signal: Negated Latched Output (Q NOT)
LE47.Gate Out	Signal: Output of the logic gate
LE47.Timer Out	Signal: Timer Output
LE47.Out	Signal: Latched Output (Q)
LE47.Out inverted	Signal: Negated Latched Output (Q NOT)
LE48.Gate Out	Signal: Output of the logic gate
LE48.Timer Out	Signal: Timer Output
LE48.Out	Signal: Latched Output (Q)
LE48.Out inverted	Signal: Negated Latched Output (Q NOT)
LE49.Gate Out	Signal: Output of the logic gate
LE49.Timer Out	Signal: Timer Output
LE49.Out	Signal: Latched Output (Q)
LE49.Out inverted	Signal: Negated Latched Output (Q NOT)
LE50.Gate Out	Signal: Output of the logic gate
LE50.Timer Out	Signal: Timer Output
LE50.Out	Signal: Latched Output (Q)
LE50.Out inverted	Signal: Negated Latched Output (Q NOT)
LE51.Gate Out	Signal: Output of the logic gate
LE51.Timer Out	Signal: Timer Output
LE51.Out	Signal: Latched Output (Q)
LE51.Out inverted	Signal: Negated Latched Output (Q NOT)
LE52.Gate Out	Signal: Output of the logic gate
LE52.Timer Out	Signal: Timer Output
LE52.Out	Signal: Latched Output (Q)
LE52.Out inverted	Signal: Negated Latched Output (Q NOT)
LE53.Gate Out	Signal: Output of the logic gate
LE53.Timer Out	Signal: Timer Output
LE53.Out	Signal: Latched Output (Q)
LE53.Out inverted	Signal: Negated Latched Output (Q NOT)
LE54.Gate Out	Signal: Output of the logic gate
LE54.Timer Out	Signal: Timer Output
LE54.Out	Signal: Latched Output (Q)
LE54.Out inverted	Signal: Negated Latched Output (Q NOT)
LE55.Gate Out	Signal: Output of the logic gate
LE55.Timer Out	Signal: Timer Output
LE55.Out	Signal: Latched Output (Q)
LE55.Out inverted	Signal: Negated Latched Output (Q NOT)
LE56.Gate Out	Signal: Output of the logic gate

Decoupling Functions	Description
LE56.Timer Out	Signal: Timer Output
LE56.Out	Signal: Latched Output (Q)
LE56.Out inverted	Signal: Negated Latched Output (Q NOT)
LE57.Gate Out	Signal: Output of the logic gate
LE57.Timer Out	Signal: Timer Output
LE57.Out	Signal: Latched Output (Q)
LE57.Out inverted	Signal: Negated Latched Output (Q NOT)
LE58.Gate Out	Signal: Output of the logic gate
LE58.Timer Out	Signal: Timer Output
LE58.Out	Signal: Latched Output (Q)
LE58.Out inverted	Signal: Negated Latched Output (Q NOT)
LE59.Gate Out	Signal: Output of the logic gate
LE59.Timer Out	Signal: Timer Output
LE59.Out	Signal: Latched Output (Q)
LE59.Out inverted	Signal: Negated Latched Output (Q NOT)
LE60.Gate Out	Signal: Output of the logic gate
LE60.Timer Out	Signal: Timer Output
LE60.Out	Signal: Latched Output (Q)
LE60.Out inverted	Signal: Negated Latched Output (Q NOT)
LE61.Gate Out	Signal: Output of the logic gate
LE61.Timer Out	Signal: Timer Output
LE61.Out	Signal: Latched Output (Q)
LE61.Out inverted	Signal: Negated Latched Output (Q NOT)
LE62.Gate Out	Signal: Output of the logic gate
LE62.Timer Out	Signal: Timer Output
LE62.Out	Signal: Latched Output (Q)
LE62.Out inverted	Signal: Negated Latched Output (Q NOT)
LE63.Gate Out	Signal: Output of the logic gate
LE63.Timer Out	Signal: Timer Output
LE63.Out	Signal: Latched Output (Q)
LE63.Out inverted	Signal: Negated Latched Output (Q NOT)
LE64.Gate Out	Signal: Output of the logic gate
LE64.Timer Out	Signal: Timer Output
LE64.Out	Signal: Latched Output (Q)
LE64.Out inverted	Signal: Negated Latched Output (Q NOT)
LE65.Gate Out	Signal: Output of the logic gate
LE65.Timer Out	Signal: Timer Output
LE65.Out	Signal: Latched Output (Q)

Decoupling Functions	Description
LE65.Out inverted	Signal: Negated Latched Output (Q NOT)
LE66.Gate Out	Signal: Output of the logic gate
LE66.Timer Out	Signal: Timer Output
LE66.Out	Signal: Latched Output (Q)
LE66.Out inverted	Signal: Negated Latched Output (Q NOT)
LE67.Gate Out	Signal: Output of the logic gate
LE67.Timer Out	Signal: Timer Output
LE67.Out	Signal: Latched Output (Q)
LE67.Out inverted	Signal: Negated Latched Output (Q NOT)
LE68.Gate Out	Signal: Output of the logic gate
LE68.Timer Out	Signal: Timer Output
LE68.Out	Signal: Latched Output (Q)
LE68.Out inverted	Signal: Negated Latched Output (Q NOT)
LE69.Gate Out	Signal: Output of the logic gate
LE69.Timer Out	Signal: Timer Output
LE69.Out	Signal: Latched Output (Q)
LE69.Out inverted	Signal: Negated Latched Output (Q NOT)
LE70.Gate Out	Signal: Output of the logic gate
LE70.Timer Out	Signal: Timer Output
LE70.Out	Signal: Latched Output (Q)
LE70.Out inverted	Signal: Negated Latched Output (Q NOT)
LE71.Gate Out	Signal: Output of the logic gate
LE71.Timer Out	Signal: Timer Output
LE71.Out	Signal: Latched Output (Q)
LE71.Out inverted	Signal: Negated Latched Output (Q NOT)
LE72.Gate Out	Signal: Output of the logic gate
LE72.Timer Out	Signal: Timer Output
LE72.Out	Signal: Latched Output (Q)
LE72.Out inverted	Signal: Negated Latched Output (Q NOT)
LE73.Gate Out	Signal: Output of the logic gate
LE73.Timer Out	Signal: Timer Output
LE73.Out	Signal: Latched Output (Q)
LE73.Out inverted	Signal: Negated Latched Output (Q NOT)
LE74.Gate Out	Signal: Output of the logic gate
LE74.Timer Out	Signal: Timer Output
LE74.Out	Signal: Latched Output (Q)
LE74.Out inverted	Signal: Negated Latched Output (Q NOT)
LE75.Gate Out	Signal: Output of the logic gate

Decoupling Functions	Description
LE75.Timer Out	Signal: Timer Output
LE75.Out	Signal: Latched Output (Q)
LE75.Out inverted	Signal: Negated Latched Output (Q NOT)
LE76.Gate Out	Signal: Output of the logic gate
LE76.Timer Out	Signal: Timer Output
LE76.Out	Signal: Latched Output (Q)
LE76.Out inverted	Signal: Negated Latched Output (Q NOT)
LE77.Gate Out	Signal: Output of the logic gate
LE77.Timer Out	Signal: Timer Output
LE77.Out	Signal: Latched Output (Q)
LE77.Out inverted	Signal: Negated Latched Output (Q NOT)
LE78.Gate Out	Signal: Output of the logic gate
LE78.Timer Out	Signal: Timer Output
LE78.Out	Signal: Latched Output (Q)
LE78.Out inverted	Signal: Negated Latched Output (Q NOT)
LE79.Gate Out	Signal: Output of the logic gate
LE79.Timer Out	Signal: Timer Output
LE79.Out	Signal: Latched Output (Q)
LE79.Out inverted	Signal: Negated Latched Output (Q NOT)
LE80.Gate Out	Signal: Output of the logic gate
LE80.Timer Out	Signal: Timer Output
LE80.Out	Signal: Latched Output (Q)
LE80.Out inverted	Signal: Negated Latched Output (Q NOT)

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Referenced by:

- Sync . CBCloseInitiate

1..n, SyncRequestList	Description
-	No assignment
Sync ON request	Signal: Synchronous ON request
DI 1	Signal: Digital Input
DI 2	Signal: Digital Input
DI 3	Signal: Digital Input
DI 4	Signal: Digital Input
DI 5	Signal: Digital Input
DI 6	Signal: Digital Input

1..n, SyncRequestList	Description
DI 7	Signal: Digital Input
DI 8	Signal: Digital Input
LE1.Gate Out	Signal: Output of the logic gate
LE1.Timer Out	Signal: Timer Output
LE1.Out	Signal: Latched Output (Q)
LE1.Out inverted	Signal: Negated Latched Output (Q NOT)
LE2.Gate Out	Signal: Output of the logic gate
LE2.Timer Out	Signal: Timer Output
LE2.Out	Signal: Latched Output (Q)
LE2.Out inverted	Signal: Negated Latched Output (Q NOT)
LE3.Gate Out	Signal: Output of the logic gate
LE3.Timer Out	Signal: Timer Output
LE3.Out	Signal: Latched Output (Q)
LE3.Out inverted	Signal: Negated Latched Output (Q NOT)
LE4.Gate Out	Signal: Output of the logic gate
LE4.Timer Out	Signal: Timer Output
LE4.Out	Signal: Latched Output (Q)
LE4.Out inverted	Signal: Negated Latched Output (Q NOT)
LE5.Gate Out	Signal: Output of the logic gate
LE5.Timer Out	Signal: Timer Output
LE5.Out	Signal: Latched Output (Q)
LE5.Out inverted	Signal: Negated Latched Output (Q NOT)
LE6.Gate Out	Signal: Output of the logic gate
LE6.Timer Out	Signal: Timer Output
LE6.Out	Signal: Latched Output (Q)
LE6.Out inverted	Signal: Negated Latched Output (Q NOT)
LE7.Gate Out	Signal: Output of the logic gate
LE7.Timer Out	Signal: Timer Output
LE7.Out	Signal: Latched Output (Q)
LE7.Out inverted	Signal: Negated Latched Output (Q NOT)
LE8.Gate Out	Signal: Output of the logic gate
LE8.Timer Out	Signal: Timer Output
LE8.Out	Signal: Latched Output (Q)
LE8.Out inverted	Signal: Negated Latched Output (Q NOT)
LE9.Gate Out	Signal: Output of the logic gate
LE9.Timer Out	Signal: Timer Output
LE9.Out	Signal: Latched Output (Q)
LE9.Out inverted	Signal: Negated Latched Output (Q NOT)

1..n, SyncRequestList	Description
LE10.Gate Out	Signal: Output of the logic gate
LE10.Timer Out	Signal: Timer Output
LE10.Out	Signal: Latched Output (Q)
LE10.Out inverted	Signal: Negated Latched Output (Q NOT)
LE11.Gate Out	Signal: Output of the logic gate
LE11.Timer Out	Signal: Timer Output
LE11.Out	Signal: Latched Output (Q)
LE11.Out inverted	Signal: Negated Latched Output (Q NOT)
LE12.Gate Out	Signal: Output of the logic gate
LE12.Timer Out	Signal: Timer Output
LE12.Out	Signal: Latched Output (Q)
LE12.Out inverted	Signal: Negated Latched Output (Q NOT)
LE13.Gate Out	Signal: Output of the logic gate
LE13.Timer Out	Signal: Timer Output
LE13.Out	Signal: Latched Output (Q)
LE13.Out inverted	Signal: Negated Latched Output (Q NOT)
LE14.Gate Out	Signal: Output of the logic gate
LE14.Timer Out	Signal: Timer Output
LE14.Out	Signal: Latched Output (Q)
LE14.Out inverted	Signal: Negated Latched Output (Q NOT)
LE15.Gate Out	Signal: Output of the logic gate
LE15.Timer Out	Signal: Timer Output
LE15.Out	Signal: Latched Output (Q)
LE15.Out inverted	Signal: Negated Latched Output (Q NOT)
LE16.Gate Out	Signal: Output of the logic gate
LE16.Timer Out	Signal: Timer Output
LE16.Out	Signal: Latched Output (Q)
LE16.Out inverted	Signal: Negated Latched Output (Q NOT)
LE17.Gate Out	Signal: Output of the logic gate
LE17.Timer Out	Signal: Timer Output
LE17.Out	Signal: Latched Output (Q)
LE17.Out inverted	Signal: Negated Latched Output (Q NOT)
LE18.Gate Out	Signal: Output of the logic gate
LE18.Timer Out	Signal: Timer Output
LE18.Out	Signal: Latched Output (Q)
LE18.Out inverted	Signal: Negated Latched Output (Q NOT)
LE19.Gate Out	Signal: Output of the logic gate
LE19.Timer Out	Signal: Timer Output

1..n, SyncRequestList	Description
LE19.Out	Signal: Latched Output (Q)
LE19.Out inverted	Signal: Negated Latched Output (Q NOT)
LE20.Gate Out	Signal: Output of the logic gate
LE20.Timer Out	Signal: Timer Output
LE20.Out	Signal: Latched Output (Q)
LE20.Out inverted	Signal: Negated Latched Output (Q NOT)
LE21.Gate Out	Signal: Output of the logic gate
LE21.Timer Out	Signal: Timer Output
LE21.Out	Signal: Latched Output (Q)
LE21.Out inverted	Signal: Negated Latched Output (Q NOT)
LE22.Gate Out	Signal: Output of the logic gate
LE22.Timer Out	Signal: Timer Output
LE22.Out	Signal: Latched Output (Q)
LE22.Out inverted	Signal: Negated Latched Output (Q NOT)
LE23.Gate Out	Signal: Output of the logic gate
LE23.Timer Out	Signal: Timer Output
LE23.Out	Signal: Latched Output (Q)
LE23.Out inverted	Signal: Negated Latched Output (Q NOT)
LE24.Gate Out	Signal: Output of the logic gate
LE24.Timer Out	Signal: Timer Output
LE24.Out	Signal: Latched Output (Q)
LE24.Out inverted	Signal: Negated Latched Output (Q NOT)
LE25.Gate Out	Signal: Output of the logic gate
LE25.Timer Out	Signal: Timer Output
LE25.Out	Signal: Latched Output (Q)
LE25.Out inverted	Signal: Negated Latched Output (Q NOT)
LE26.Gate Out	Signal: Output of the logic gate
LE26.Timer Out	Signal: Timer Output
LE26.Out	Signal: Latched Output (Q)
LE26.Out inverted	Signal: Negated Latched Output (Q NOT)
LE27.Gate Out	Signal: Output of the logic gate
LE27.Timer Out	Signal: Timer Output
LE27.Out	Signal: Latched Output (Q)
LE27.Out inverted	Signal: Negated Latched Output (Q NOT)
LE28.Gate Out	Signal: Output of the logic gate
LE28.Timer Out	Signal: Timer Output
LE28.Out	Signal: Latched Output (Q)
LE28.Out inverted	Signal: Negated Latched Output (Q NOT)

1..n, SyncRequestList	Description
LE29.Gate Out	Signal: Output of the logic gate
LE29.Timer Out	Signal: Timer Output
LE29.Out	Signal: Latched Output (Q)
LE29.Out inverted	Signal: Negated Latched Output (Q NOT)
LE30.Gate Out	Signal: Output of the logic gate
LE30.Timer Out	Signal: Timer Output
LE30.Out	Signal: Latched Output (Q)
LE30.Out inverted	Signal: Negated Latched Output (Q NOT)
LE31.Gate Out	Signal: Output of the logic gate
LE31.Timer Out	Signal: Timer Output
LE31.Out	Signal: Latched Output (Q)
LE31.Out inverted	Signal: Negated Latched Output (Q NOT)
LE32.Gate Out	Signal: Output of the logic gate
LE32.Timer Out	Signal: Timer Output
LE32.Out	Signal: Latched Output (Q)
LE32.Out inverted	Signal: Negated Latched Output (Q NOT)
LE33.Gate Out	Signal: Output of the logic gate
LE33.Timer Out	Signal: Timer Output
LE33.Out	Signal: Latched Output (Q)
LE33.Out inverted	Signal: Negated Latched Output (Q NOT)
LE34.Gate Out	Signal: Output of the logic gate
LE34.Timer Out	Signal: Timer Output
LE34.Out	Signal: Latched Output (Q)
LE34.Out inverted	Signal: Negated Latched Output (Q NOT)
LE35.Gate Out	Signal: Output of the logic gate
LE35.Timer Out	Signal: Timer Output
LE35.Out	Signal: Latched Output (Q)
LE35.Out inverted	Signal: Negated Latched Output (Q NOT)
LE36.Gate Out	Signal: Output of the logic gate
LE36.Timer Out	Signal: Timer Output
LE36.Out	Signal: Latched Output (Q)
LE36.Out inverted	Signal: Negated Latched Output (Q NOT)
LE37.Gate Out	Signal: Output of the logic gate
LE37.Timer Out	Signal: Timer Output
LE37.Out	Signal: Latched Output (Q)
LE37.Out inverted	Signal: Negated Latched Output (Q NOT)
LE38.Gate Out	Signal: Output of the logic gate
LE38.Timer Out	Signal: Timer Output

1..n, SyncRequestList	Description
LE38.Out	Signal: Latched Output (Q)
LE38.Out inverted	Signal: Negated Latched Output (Q NOT)
LE39.Gate Out	Signal: Output of the logic gate
LE39.Timer Out	Signal: Timer Output
LE39.Out	Signal: Latched Output (Q)
LE39.Out inverted	Signal: Negated Latched Output (Q NOT)
LE40.Gate Out	Signal: Output of the logic gate
LE40.Timer Out	Signal: Timer Output
LE40.Out	Signal: Latched Output (Q)
LE40.Out inverted	Signal: Negated Latched Output (Q NOT)
LE41.Gate Out	Signal: Output of the logic gate
LE41.Timer Out	Signal: Timer Output
LE41.Out	Signal: Latched Output (Q)
LE41.Out inverted	Signal: Negated Latched Output (Q NOT)
LE42.Gate Out	Signal: Output of the logic gate
LE42.Timer Out	Signal: Timer Output
LE42.Out	Signal: Latched Output (Q)
LE42.Out inverted	Signal: Negated Latched Output (Q NOT)
LE43.Gate Out	Signal: Output of the logic gate
LE43.Timer Out	Signal: Timer Output
LE43.Out	Signal: Latched Output (Q)
LE43.Out inverted	Signal: Negated Latched Output (Q NOT)
LE44.Gate Out	Signal: Output of the logic gate
LE44.Timer Out	Signal: Timer Output
LE44.Out	Signal: Latched Output (Q)
LE44.Out inverted	Signal: Negated Latched Output (Q NOT)
LE45.Gate Out	Signal: Output of the logic gate
LE45.Timer Out	Signal: Timer Output
LE45.Out	Signal: Latched Output (Q)
LE45.Out inverted	Signal: Negated Latched Output (Q NOT)
LE46.Gate Out	Signal: Output of the logic gate
LE46.Timer Out	Signal: Timer Output
LE46.Out	Signal: Latched Output (Q)
LE46.Out inverted	Signal: Negated Latched Output (Q NOT)
LE47.Gate Out	Signal: Output of the logic gate
LE47.Timer Out	Signal: Timer Output
LE47.Out	Signal: Latched Output (Q)
LE47.Out inverted	Signal: Negated Latched Output (Q NOT)

1..n, SyncRequestList	Description
LE48.Gate Out	Signal: Output of the logic gate
LE48.Timer Out	Signal: Timer Output
LE48.Out	Signal: Latched Output (Q)
LE48.Out inverted	Signal: Negated Latched Output (Q NOT)
LE49.Gate Out	Signal: Output of the logic gate
LE49.Timer Out	Signal: Timer Output
LE49.Out	Signal: Latched Output (Q)
LE49.Out inverted	Signal: Negated Latched Output (Q NOT)
LE50.Gate Out	Signal: Output of the logic gate
LE50.Timer Out	Signal: Timer Output
LE50.Out	Signal: Latched Output (Q)
LE50.Out inverted	Signal: Negated Latched Output (Q NOT)
LE51.Gate Out	Signal: Output of the logic gate
LE51.Timer Out	Signal: Timer Output
LE51.Out	Signal: Latched Output (Q)
LE51.Out inverted	Signal: Negated Latched Output (Q NOT)
LE52.Gate Out	Signal: Output of the logic gate
LE52.Timer Out	Signal: Timer Output
LE52.Out	Signal: Latched Output (Q)
LE52.Out inverted	Signal: Negated Latched Output (Q NOT)
LE53.Gate Out	Signal: Output of the logic gate
LE53.Timer Out	Signal: Timer Output
LE53.Out	Signal: Latched Output (Q)
LE53.Out inverted	Signal: Negated Latched Output (Q NOT)
LE54.Gate Out	Signal: Output of the logic gate
LE54.Timer Out	Signal: Timer Output
LE54.Out	Signal: Latched Output (Q)
LE54.Out inverted	Signal: Negated Latched Output (Q NOT)
LE55.Gate Out	Signal: Output of the logic gate
LE55.Timer Out	Signal: Timer Output
LE55.Out	Signal: Latched Output (Q)
LE55.Out inverted	Signal: Negated Latched Output (Q NOT)
LE56.Gate Out	Signal: Output of the logic gate
LE56.Timer Out	Signal: Timer Output
LE56.Out	Signal: Latched Output (Q)
LE56.Out inverted	Signal: Negated Latched Output (Q NOT)
LE57.Gate Out	Signal: Output of the logic gate
LE57.Timer Out	Signal: Timer Output

1..n, SyncRequestList	Description
LE57.Out	Signal: Latched Output (Q)
LE57.Out inverted	Signal: Negated Latched Output (Q NOT)
LE58.Gate Out	Signal: Output of the logic gate
LE58.Timer Out	Signal: Timer Output
LE58.Out	Signal: Latched Output (Q)
LE58.Out inverted	Signal: Negated Latched Output (Q NOT)
LE59.Gate Out	Signal: Output of the logic gate
LE59.Timer Out	Signal: Timer Output
LE59.Out	Signal: Latched Output (Q)
LE59.Out inverted	Signal: Negated Latched Output (Q NOT)
LE60.Gate Out	Signal: Output of the logic gate
LE60.Timer Out	Signal: Timer Output
LE60.Out	Signal: Latched Output (Q)
LE60.Out inverted	Signal: Negated Latched Output (Q NOT)
LE61.Gate Out	Signal: Output of the logic gate
LE61.Timer Out	Signal: Timer Output
LE61.Out	Signal: Latched Output (Q)
LE61.Out inverted	Signal: Negated Latched Output (Q NOT)
LE62.Gate Out	Signal: Output of the logic gate
LE62.Timer Out	Signal: Timer Output
LE62.Out	Signal: Latched Output (Q)
LE62.Out inverted	Signal: Negated Latched Output (Q NOT)
LE63.Gate Out	Signal: Output of the logic gate
LE63.Timer Out	Signal: Timer Output
LE63.Out	Signal: Latched Output (Q)
LE63.Out inverted	Signal: Negated Latched Output (Q NOT)
LE64.Gate Out	Signal: Output of the logic gate
LE64.Timer Out	Signal: Timer Output
LE64.Out	Signal: Latched Output (Q)
LE64.Out inverted	Signal: Negated Latched Output (Q NOT)
LE65.Gate Out	Signal: Output of the logic gate
LE65.Timer Out	Signal: Timer Output
LE65.Out	Signal: Latched Output (Q)
LE65.Out inverted	Signal: Negated Latched Output (Q NOT)
LE66.Gate Out	Signal: Output of the logic gate
LE66.Timer Out	Signal: Timer Output
LE66.Out	Signal: Latched Output (Q)
LE66.Out inverted	Signal: Negated Latched Output (Q NOT)

1..n, SyncRequestList	Description
LE67.Gate Out	Signal: Output of the logic gate
LE67.Timer Out	Signal: Timer Output
LE67.Out	Signal: Latched Output (Q)
LE67.Out inverted	Signal: Negated Latched Output (Q NOT)
LE68.Gate Out	Signal: Output of the logic gate
LE68.Timer Out	Signal: Timer Output
LE68.Out	Signal: Latched Output (Q)
LE68.Out inverted	Signal: Negated Latched Output (Q NOT)
LE69.Gate Out	Signal: Output of the logic gate
LE69.Timer Out	Signal: Timer Output
LE69.Out	Signal: Latched Output (Q)
LE69.Out inverted	Signal: Negated Latched Output (Q NOT)
LE70.Gate Out	Signal: Output of the logic gate
LE70.Timer Out	Signal: Timer Output
LE70.Out	Signal: Latched Output (Q)
LE70.Out inverted	Signal: Negated Latched Output (Q NOT)
LE71.Gate Out	Signal: Output of the logic gate
LE71.Timer Out	Signal: Timer Output
LE71.Out	Signal: Latched Output (Q)
LE71.Out inverted	Signal: Negated Latched Output (Q NOT)
LE72.Gate Out	Signal: Output of the logic gate
LE72.Timer Out	Signal: Timer Output
LE72.Out	Signal: Latched Output (Q)
LE72.Out inverted	Signal: Negated Latched Output (Q NOT)
LE73.Gate Out	Signal: Output of the logic gate
LE73.Timer Out	Signal: Timer Output
LE73.Out	Signal: Latched Output (Q)
LE73.Out inverted	Signal: Negated Latched Output (Q NOT)
LE74.Gate Out	Signal: Output of the logic gate
LE74.Timer Out	Signal: Timer Output
LE74.Out	Signal: Latched Output (Q)
LE74.Out inverted	Signal: Negated Latched Output (Q NOT)
LE75.Gate Out	Signal: Output of the logic gate
LE75.Timer Out	Signal: Timer Output
LE75.Out	Signal: Latched Output (Q)
LE75.Out inverted	Signal: Negated Latched Output (Q NOT)
LE76.Gate Out	Signal: Output of the logic gate
LE76.Timer Out	Signal: Timer Output

1..n, SyncRequestList	Description
LE76.Out	Signal: Latched Output (Q)
LE76.Out inverted	Signal: Negated Latched Output (Q NOT)
LE77.Gate Out	Signal: Output of the logic gate
LE77.Timer Out	Signal: Timer Output
LE77.Out	Signal: Latched Output (Q)
LE77.Out inverted	Signal: Negated Latched Output (Q NOT)
LE78.Gate Out	Signal: Output of the logic gate
LE78.Timer Out	Signal: Timer Output
LE78.Out	Signal: Latched Output (Q)
LE78.Out inverted	Signal: Negated Latched Output (Q NOT)
LE79.Gate Out	Signal: Output of the logic gate
LE79.Timer Out	Signal: Timer Output
LE79.Out	Signal: Latched Output (Q)
LE79.Out inverted	Signal: Negated Latched Output (Q NOT)
LE80.Gate Out	Signal: Output of the logic gate
LE80.Timer Out	Signal: Timer Output
LE80.Out	Signal: Latched Output (Q)
LE80.Out inverted	Signal: Negated Latched Output (Q NOT)

17.178 1..n, In-SyncList

Referenced by:

- SG[1] . Synchronism

1..n, In-SyncList	Description
-	No assignment
Ready to Close	Signal: Ready to Close
DI 1	Signal: Digital Input
DI 2	Signal: Digital Input
DI 3	Signal: Digital Input
DI 4	Signal: Digital Input
DI 5	Signal: Digital Input
DI 6	Signal: Digital Input
DI 7	Signal: Digital Input
DI 8	Signal: Digital Input
LE1.Gate Out	Signal: Output of the logic gate
LE1.Timer Out	Signal: Timer Output
LE1.Out	Signal: Latched Output (Q)

1..n, In-SyncList	Description
LE1.Out inverted	Signal: Negated Latched Output (Q NOT)
LE2.Gate Out	Signal: Output of the logic gate
LE2.Timer Out	Signal: Timer Output
LE2.Out	Signal: Latched Output (Q)
LE2.Out inverted	Signal: Negated Latched Output (Q NOT)
LE3.Gate Out	Signal: Output of the logic gate
LE3.Timer Out	Signal: Timer Output
LE3.Out	Signal: Latched Output (Q)
LE3.Out inverted	Signal: Negated Latched Output (Q NOT)
LE4.Gate Out	Signal: Output of the logic gate
LE4.Timer Out	Signal: Timer Output
LE4.Out	Signal: Latched Output (Q)
LE4.Out inverted	Signal: Negated Latched Output (Q NOT)
LE5.Gate Out	Signal: Output of the logic gate
LE5.Timer Out	Signal: Timer Output
LE5.Out	Signal: Latched Output (Q)
LE5.Out inverted	Signal: Negated Latched Output (Q NOT)
LE6.Gate Out	Signal: Output of the logic gate
LE6.Timer Out	Signal: Timer Output
LE6.Out	Signal: Latched Output (Q)
LE6.Out inverted	Signal: Negated Latched Output (Q NOT)
LE7.Gate Out	Signal: Output of the logic gate
LE7.Timer Out	Signal: Timer Output
LE7.Out	Signal: Latched Output (Q)
LE7.Out inverted	Signal: Negated Latched Output (Q NOT)
LE8.Gate Out	Signal: Output of the logic gate
LE8.Timer Out	Signal: Timer Output
LE8.Out	Signal: Latched Output (Q)
LE8.Out inverted	Signal: Negated Latched Output (Q NOT)
LE9.Gate Out	Signal: Output of the logic gate
LE9.Timer Out	Signal: Timer Output
LE9.Out	Signal: Latched Output (Q)
LE9.Out inverted	Signal: Negated Latched Output (Q NOT)
LE10.Gate Out	Signal: Output of the logic gate
LE10.Timer Out	Signal: Timer Output
LE10.Out	Signal: Latched Output (Q)
LE10.Out inverted	Signal: Negated Latched Output (Q NOT)
LE11.Gate Out	Signal: Output of the logic gate

1..n, In-SyncList	Description
LE11.Timer Out	Signal: Timer Output
LE11.Out	Signal: Latched Output (Q)
LE11.Out inverted	Signal: Negated Latched Output (Q NOT)
LE12.Gate Out	Signal: Output of the logic gate
LE12.Timer Out	Signal: Timer Output
LE12.Out	Signal: Latched Output (Q)
LE12.Out inverted	Signal: Negated Latched Output (Q NOT)
LE13.Gate Out	Signal: Output of the logic gate
LE13.Timer Out	Signal: Timer Output
LE13.Out	Signal: Latched Output (Q)
LE13.Out inverted	Signal: Negated Latched Output (Q NOT)
LE14.Gate Out	Signal: Output of the logic gate
LE14.Timer Out	Signal: Timer Output
LE14.Out	Signal: Latched Output (Q)
LE14.Out inverted	Signal: Negated Latched Output (Q NOT)
LE15.Gate Out	Signal: Output of the logic gate
LE15.Timer Out	Signal: Timer Output
LE15.Out	Signal: Latched Output (Q)
LE15.Out inverted	Signal: Negated Latched Output (Q NOT)
LE16.Gate Out	Signal: Output of the logic gate
LE16.Timer Out	Signal: Timer Output
LE16.Out	Signal: Latched Output (Q)
LE16.Out inverted	Signal: Negated Latched Output (Q NOT)
LE17.Gate Out	Signal: Output of the logic gate
LE17.Timer Out	Signal: Timer Output
LE17.Out	Signal: Latched Output (Q)
LE17.Out inverted	Signal: Negated Latched Output (Q NOT)
LE18.Gate Out	Signal: Output of the logic gate
LE18.Timer Out	Signal: Timer Output
LE18.Out	Signal: Latched Output (Q)
LE18.Out inverted	Signal: Negated Latched Output (Q NOT)
LE19.Gate Out	Signal: Output of the logic gate
LE19.Timer Out	Signal: Timer Output
LE19.Out	Signal: Latched Output (Q)
LE19.Out inverted	Signal: Negated Latched Output (Q NOT)
LE20.Gate Out	Signal: Output of the logic gate
LE20.Timer Out	Signal: Timer Output
LE20.Out	Signal: Latched Output (Q)

1..n, In-SyncList	Description
LE20.Out inverted	Signal: Negated Latched Output (Q NOT)
LE21.Gate Out	Signal: Output of the logic gate
LE21.Timer Out	Signal: Timer Output
LE21.Out	Signal: Latched Output (Q)
LE21.Out inverted	Signal: Negated Latched Output (Q NOT)
LE22.Gate Out	Signal: Output of the logic gate
LE22.Timer Out	Signal: Timer Output
LE22.Out	Signal: Latched Output (Q)
LE22.Out inverted	Signal: Negated Latched Output (Q NOT)
LE23.Gate Out	Signal: Output of the logic gate
LE23.Timer Out	Signal: Timer Output
LE23.Out	Signal: Latched Output (Q)
LE23.Out inverted	Signal: Negated Latched Output (Q NOT)
LE24.Gate Out	Signal: Output of the logic gate
LE24.Timer Out	Signal: Timer Output
LE24.Out	Signal: Latched Output (Q)
LE24.Out inverted	Signal: Negated Latched Output (Q NOT)
LE25.Gate Out	Signal: Output of the logic gate
LE25.Timer Out	Signal: Timer Output
LE25.Out	Signal: Latched Output (Q)
LE25.Out inverted	Signal: Negated Latched Output (Q NOT)
LE26.Gate Out	Signal: Output of the logic gate
LE26.Timer Out	Signal: Timer Output
LE26.Out	Signal: Latched Output (Q)
LE26.Out inverted	Signal: Negated Latched Output (Q NOT)
LE27.Gate Out	Signal: Output of the logic gate
LE27.Timer Out	Signal: Timer Output
LE27.Out	Signal: Latched Output (Q)
LE27.Out inverted	Signal: Negated Latched Output (Q NOT)
LE28.Gate Out	Signal: Output of the logic gate
LE28.Timer Out	Signal: Timer Output
LE28.Out	Signal: Latched Output (Q)
LE28.Out inverted	Signal: Negated Latched Output (Q NOT)
LE29.Gate Out	Signal: Output of the logic gate
LE29.Timer Out	Signal: Timer Output
LE29.Out	Signal: Latched Output (Q)
LE29.Out inverted	Signal: Negated Latched Output (Q NOT)
LE30.Gate Out	Signal: Output of the logic gate

1..n, In-SyncList	Description
LE30.Timer Out	Signal: Timer Output
LE30.Out	Signal: Latched Output (Q)
LE30.Out inverted	Signal: Negated Latched Output (Q NOT)
LE31.Gate Out	Signal: Output of the logic gate
LE31.Timer Out	Signal: Timer Output
LE31.Out	Signal: Latched Output (Q)
LE31.Out inverted	Signal: Negated Latched Output (Q NOT)
LE32.Gate Out	Signal: Output of the logic gate
LE32.Timer Out	Signal: Timer Output
LE32.Out	Signal: Latched Output (Q)
LE32.Out inverted	Signal: Negated Latched Output (Q NOT)
LE33.Gate Out	Signal: Output of the logic gate
LE33.Timer Out	Signal: Timer Output
LE33.Out	Signal: Latched Output (Q)
LE33.Out inverted	Signal: Negated Latched Output (Q NOT)
LE34.Gate Out	Signal: Output of the logic gate
LE34.Timer Out	Signal: Timer Output
LE34.Out	Signal: Latched Output (Q)
LE34.Out inverted	Signal: Negated Latched Output (Q NOT)
LE35.Gate Out	Signal: Output of the logic gate
LE35.Timer Out	Signal: Timer Output
LE35.Out	Signal: Latched Output (Q)
LE35.Out inverted	Signal: Negated Latched Output (Q NOT)
LE36.Gate Out	Signal: Output of the logic gate
LE36.Timer Out	Signal: Timer Output
LE36.Out	Signal: Latched Output (Q)
LE36.Out inverted	Signal: Negated Latched Output (Q NOT)
LE37.Gate Out	Signal: Output of the logic gate
LE37.Timer Out	Signal: Timer Output
LE37.Out	Signal: Latched Output (Q)
LE37.Out inverted	Signal: Negated Latched Output (Q NOT)
LE38.Gate Out	Signal: Output of the logic gate
LE38.Timer Out	Signal: Timer Output
LE38.Out	Signal: Latched Output (Q)
LE38.Out inverted	Signal: Negated Latched Output (Q NOT)
LE39.Gate Out	Signal: Output of the logic gate
LE39.Timer Out	Signal: Timer Output
LE39.Out	Signal: Latched Output (Q)

1..n, In-SyncList	Description
LE39.Out inverted	Signal: Negated Latched Output (Q NOT)
LE40.Gate Out	Signal: Output of the logic gate
LE40.Timer Out	Signal: Timer Output
LE40.Out	Signal: Latched Output (Q)
LE40.Out inverted	Signal: Negated Latched Output (Q NOT)
LE41.Gate Out	Signal: Output of the logic gate
LE41.Timer Out	Signal: Timer Output
LE41.Out	Signal: Latched Output (Q)
LE41.Out inverted	Signal: Negated Latched Output (Q NOT)
LE42.Gate Out	Signal: Output of the logic gate
LE42.Timer Out	Signal: Timer Output
LE42.Out	Signal: Latched Output (Q)
LE42.Out inverted	Signal: Negated Latched Output (Q NOT)
LE43.Gate Out	Signal: Output of the logic gate
LE43.Timer Out	Signal: Timer Output
LE43.Out	Signal: Latched Output (Q)
LE43.Out inverted	Signal: Negated Latched Output (Q NOT)
LE44.Gate Out	Signal: Output of the logic gate
LE44.Timer Out	Signal: Timer Output
LE44.Out	Signal: Latched Output (Q)
LE44.Out inverted	Signal: Negated Latched Output (Q NOT)
LE45.Gate Out	Signal: Output of the logic gate
LE45.Timer Out	Signal: Timer Output
LE45.Out	Signal: Latched Output (Q)
LE45.Out inverted	Signal: Negated Latched Output (Q NOT)
LE46.Gate Out	Signal: Output of the logic gate
LE46.Timer Out	Signal: Timer Output
LE46.Out	Signal: Latched Output (Q)
LE46.Out inverted	Signal: Negated Latched Output (Q NOT)
LE47.Gate Out	Signal: Output of the logic gate
LE47.Timer Out	Signal: Timer Output
LE47.Out	Signal: Latched Output (Q)
LE47.Out inverted	Signal: Negated Latched Output (Q NOT)
LE48.Gate Out	Signal: Output of the logic gate
LE48.Timer Out	Signal: Timer Output
LE48.Out	Signal: Latched Output (Q)
LE48.Out inverted	Signal: Negated Latched Output (Q NOT)
LE49.Gate Out	Signal: Output of the logic gate

1..n, In-SyncList	Description
LE49.Timer Out	Signal: Timer Output
LE49.Out	Signal: Latched Output (Q)
LE49.Out inverted	Signal: Negated Latched Output (Q NOT)
LE50.Gate Out	Signal: Output of the logic gate
LE50.Timer Out	Signal: Timer Output
LE50.Out	Signal: Latched Output (Q)
LE50.Out inverted	Signal: Negated Latched Output (Q NOT)
LE51.Gate Out	Signal: Output of the logic gate
LE51.Timer Out	Signal: Timer Output
LE51.Out	Signal: Latched Output (Q)
LE51.Out inverted	Signal: Negated Latched Output (Q NOT)
LE52.Gate Out	Signal: Output of the logic gate
LE52.Timer Out	Signal: Timer Output
LE52.Out	Signal: Latched Output (Q)
LE52.Out inverted	Signal: Negated Latched Output (Q NOT)
LE53.Gate Out	Signal: Output of the logic gate
LE53.Timer Out	Signal: Timer Output
LE53.Out	Signal: Latched Output (Q)
LE53.Out inverted	Signal: Negated Latched Output (Q NOT)
LE54.Gate Out	Signal: Output of the logic gate
LE54.Timer Out	Signal: Timer Output
LE54.Out	Signal: Latched Output (Q)
LE54.Out inverted	Signal: Negated Latched Output (Q NOT)
LE55.Gate Out	Signal: Output of the logic gate
LE55.Timer Out	Signal: Timer Output
LE55.Out	Signal: Latched Output (Q)
LE55.Out inverted	Signal: Negated Latched Output (Q NOT)
LE56.Gate Out	Signal: Output of the logic gate
LE56.Timer Out	Signal: Timer Output
LE56.Out	Signal: Latched Output (Q)
LE56.Out inverted	Signal: Negated Latched Output (Q NOT)
LE57.Gate Out	Signal: Output of the logic gate
LE57.Timer Out	Signal: Timer Output
LE57.Out	Signal: Latched Output (Q)
LE57.Out inverted	Signal: Negated Latched Output (Q NOT)
LE58.Gate Out	Signal: Output of the logic gate
LE58.Timer Out	Signal: Timer Output
LE58.Out	Signal: Latched Output (Q)

1..n, In-SyncList	Description
LE58.Out inverted	Signal: Negated Latched Output (Q NOT)
LE59.Gate Out	Signal: Output of the logic gate
LE59.Timer Out	Signal: Timer Output
LE59.Out	Signal: Latched Output (Q)
LE59.Out inverted	Signal: Negated Latched Output (Q NOT)
LE60.Gate Out	Signal: Output of the logic gate
LE60.Timer Out	Signal: Timer Output
LE60.Out	Signal: Latched Output (Q)
LE60.Out inverted	Signal: Negated Latched Output (Q NOT)
LE61.Gate Out	Signal: Output of the logic gate
LE61.Timer Out	Signal: Timer Output
LE61.Out	Signal: Latched Output (Q)
LE61.Out inverted	Signal: Negated Latched Output (Q NOT)
LE62.Gate Out	Signal: Output of the logic gate
LE62.Timer Out	Signal: Timer Output
LE62.Out	Signal: Latched Output (Q)
LE62.Out inverted	Signal: Negated Latched Output (Q NOT)
LE63.Gate Out	Signal: Output of the logic gate
LE63.Timer Out	Signal: Timer Output
LE63.Out	Signal: Latched Output (Q)
LE63.Out inverted	Signal: Negated Latched Output (Q NOT)
LE64.Gate Out	Signal: Output of the logic gate
LE64.Timer Out	Signal: Timer Output
LE64.Out	Signal: Latched Output (Q)
LE64.Out inverted	Signal: Negated Latched Output (Q NOT)
LE65.Gate Out	Signal: Output of the logic gate
LE65.Timer Out	Signal: Timer Output
LE65.Out	Signal: Latched Output (Q)
LE65.Out inverted	Signal: Negated Latched Output (Q NOT)
LE66.Gate Out	Signal: Output of the logic gate
LE66.Timer Out	Signal: Timer Output
LE66.Out	Signal: Latched Output (Q)
LE66.Out inverted	Signal: Negated Latched Output (Q NOT)
LE67.Gate Out	Signal: Output of the logic gate
LE67.Timer Out	Signal: Timer Output
LE67.Out	Signal: Latched Output (Q)
LE67.Out inverted	Signal: Negated Latched Output (Q NOT)
LE68.Gate Out	Signal: Output of the logic gate

1..n, In-SyncList	Description
LE68.Timer Out	Signal: Timer Output
LE68.Out	Signal: Latched Output (Q)
LE68.Out inverted	Signal: Negated Latched Output (Q NOT)
LE69.Gate Out	Signal: Output of the logic gate
LE69.Timer Out	Signal: Timer Output
LE69.Out	Signal: Latched Output (Q)
LE69.Out inverted	Signal: Negated Latched Output (Q NOT)
LE70.Gate Out	Signal: Output of the logic gate
LE70.Timer Out	Signal: Timer Output
LE70.Out	Signal: Latched Output (Q)
LE70.Out inverted	Signal: Negated Latched Output (Q NOT)
LE71.Gate Out	Signal: Output of the logic gate
LE71.Timer Out	Signal: Timer Output
LE71.Out	Signal: Latched Output (Q)
LE71.Out inverted	Signal: Negated Latched Output (Q NOT)
LE72.Gate Out	Signal: Output of the logic gate
LE72.Timer Out	Signal: Timer Output
LE72.Out	Signal: Latched Output (Q)
LE72.Out inverted	Signal: Negated Latched Output (Q NOT)
LE73.Gate Out	Signal: Output of the logic gate
LE73.Timer Out	Signal: Timer Output
LE73.Out	Signal: Latched Output (Q)
LE73.Out inverted	Signal: Negated Latched Output (Q NOT)
LE74.Gate Out	Signal: Output of the logic gate
LE74.Timer Out	Signal: Timer Output
LE74.Out	Signal: Latched Output (Q)
LE74.Out inverted	Signal: Negated Latched Output (Q NOT)
LE75.Gate Out	Signal: Output of the logic gate
LE75.Timer Out	Signal: Timer Output
LE75.Out	Signal: Latched Output (Q)
LE75.Out inverted	Signal: Negated Latched Output (Q NOT)
LE76.Gate Out	Signal: Output of the logic gate
LE76.Timer Out	Signal: Timer Output
LE76.Out	Signal: Latched Output (Q)
LE76.Out inverted	Signal: Negated Latched Output (Q NOT)
LE77.Gate Out	Signal: Output of the logic gate
LE77.Timer Out	Signal: Timer Output
LE77.Out	Signal: Latched Output (Q)

1..n, In-SyncList	Description
LE77.Out inverted	Signal: Negated Latched Output (Q NOT)
LE78.Gate Out	Signal: Output of the logic gate
LE78.Timer Out	Signal: Timer Output
LE78.Out	Signal: Latched Output (Q)
LE78.Out inverted	Signal: Negated Latched Output (Q NOT)
LE79.Gate Out	Signal: Output of the logic gate
LE79.Timer Out	Signal: Timer Output
LE79.Out	Signal: Latched Output (Q)
LE79.Out inverted	Signal: Negated Latched Output (Q NOT)
LE80.Gate Out	Signal: Output of the logic gate
LE80.Timer Out	Signal: Timer Output
LE80.Out	Signal: Latched Output (Q)
LE80.Out inverted	Signal: Negated Latched Output (Q NOT)

17.179 1..n, Trip Cmds

Selection list referenced by the following parameters:

- SG[1] . Off Cmd1
- SG[1] . Off Cmd2
- SG[1] . Off Cmd3
- SG[1] . Off Cmd4
- SG[1] . Off Cmd5
- *[. . .]*

1..n, Trip Cmds	Description
-	No assignment
TripCmd	Signal: Trip Command
TripCmd	Signal: Trip Command
TripCmd	Signal: Trip Command
TripCmd	Signal: Trip Command
TripCmd	Signal: Trip Command
TripCmd	Signal: Trip Command
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TripCmd	Signal: Trip Command

1..n, Trip Cmds	Description
TripCmd	Signal: Trip Command
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TripCmd	Signal: Trip Command
TripCmd	Signal: Trip Command

17.180 Used Protocol

Referenced by:

- TimeSync . TimeSync

Used Protocol	Description
-	-
IRIG-B	IRIG-B-Module
SNTP	SNTP-Module
Modbus	Modbus Protocol
IEC 60870-5-103	IEC 60870-5-103 Protocol
IEC104	IEC 60870-5-104 communication
DNP3	Distributed Network Protocol
PTP	PTP-Module

17.181 1..n, Assignment List

Referenced by:

- DNP3 . BinaryCounter 0
- *[. . .]*

1..n, Assignment List	Description
-	No assignment
Fault No.	Fault number
No. of Grid Faults	Number of grid faults: This is a counter for all faults (i.e. General Alarms »Prot . Alarm«), but except faults during a running cycle of the Automatic Reclosure module (signal »AR . running«). (Remark: The »Fault No.« counts every new fault independent of AR cycles. This means that for protective devices without AR module these two counters are equivalent.)
TripCmd Cr	Counter: Total number of trips of the switchgear.
Num Vdips in t-LVRT	Number of Voltage dips during t-LVRT
Cr Tot Numb of Vdips	Counter Total number of voltage dips.
Cr Num Vdips to Trip	Counter Total number of voltage dips that caused a Trip
Num Vdips in t-LVRT	Number of Voltage dips during t-LVRT
Cr Tot Numb of Vdips	Counter Total number of voltage dips.
Cr Num Vdips to Trip	Counter Total number of voltage dips that caused a Trip
Operating hours Cr	Operating hours counter of the protective device

17.182 1..n, Assignment List

Referenced by:

- DNP3 . DoubleBitInput 0

1..n, Assignment List	Description
-	No assignment
Pos	Signal: Circuit Breaker Position (0 = Indeterminate, 1 = OFF, 2 = ON, 3 = Disturbed)

17.183 Used Protocol

Referenced by:

- Scada . Protocol

Used Protocol	Description
-	Do not use
Modbus RTU	Modbus Protocol RTU
Modbus TCP	Modbus Protocol TCP
Modbus TCP/RTU	Modbus Protocol TCP/RTU
DNP3 RTU	Distributed Network Protocol RTU
DNP3 TCP	Distributed Network Protocol TCP
DNP3 UDP	Distributed Network Protocol UDP
IEC 60870-5-103	IEC 60870-5-103 Protocol
IEC 60870-5-104	IEC 60870-5-104 Protocol
IEC 61850	IEC 61850 communication
Profibus	Profibus Module

PROTECTION MADE SIMPLE.

HighPROTEC

MRU4

REFERENCE MANUAL

docs.SEGelectronics.de/mru4-2

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