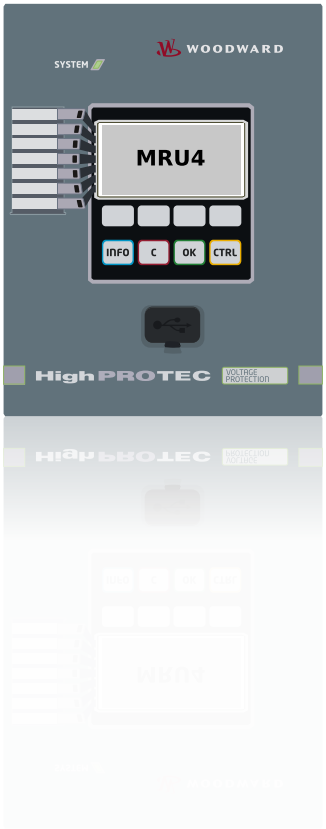
WOODWARD

HighPROTEC

Reference manual MRU4-3.6-EN-REF



MRU4

Voltage Protection

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1 About This Reference Manual

This document is a reference of all the Setting Values, Direct Commands and Signals of the MRU4. In other words, it lists all parameters that are available (or can be made available) with the (optionally) full featured versions of the MRU4 protection device.

CAUTION!

This document does not intend to give long and/or detailed description, nor does it intend to replace the full Technical Manual in any way. Only a quite short description is given for each parameter.

This document is a reference of all the Setting Values, Direct Commands and Signals of the MRU4.

Every HighPROTEC protection device operates using a lot of digital values of various types. Throughout our Technical Documentation, we are talking of “settings” (or “parameters”) or “signals” or “(measured) values”, depending on the type.

Please consult the Technical Manual, in particular Chapter “Modules, Settings, Signals and Values”, for details of the existing data types.

Modules

The firmware of every HighPROTEC protection device can be thought of being sub-divided in several independent function blocks, the so-called “modules”. Every protection function, for example, is a module of its own. But one of the fundamental concepts of a HighPROTEC protection device is to implement this with great consequence: The functionality of calculating statistical data is a module (named »Statistics«), every communication protocol is a module, the control of switchgear devices is a module (named »Ctrl«), but the properties of the switchgear itself is part of another module. There is even a general protection module (named »Prot«) that interacts all specific protection modules.

Every parameter, every value and every signal is therefore a member of some module.

But note that the settings dialogs (on the panel (HMI) or in the *Smart view* operating software) often omit the module name whenever it is clear from the menu branch. This means the parameters are often displayed only with their individual parameter names, i. e. simply *»Function«* instead of the full-blown *»I[1] . Function«*. This increases the overview and simplifies all configuration and operation work; however, it is good to know that the writing *»Function«* is just an abbreviation. In fact, **every** parameter **always** belongs to a module, and therefore – to make this concept absolutely clear – the reference tables have always the module name added in front of every parameter name

Especially for protection functions it is often required to have several instances active. For example, overcurrent protection usually has several “stages”, and all of these are running at the same time (using their individual setting values). Therefore it is an important feature of every HighPROTEC protection device that a lot of modules exist in several “instances”, which are numbered (in brackets): For the overcurrent protection, for example: »I[1]«, I[2]«, …

In the reference tables, usually every module has its own dedicated chapter, which lists the available number of instances at the beginning. Then, however, in the sub-chapters listing the various parameter types, only the first instance (e. g. »I[1]«) is mentioned, because all the other instances are identical anyway.

Structure of a Reference Table

Since (almost) every module can be activated or deactivated independently of the other modules and all parameters of an inactive module disappear from the menu branch it would not be helpful if this Reference Manual would list parameters sorted according to the menu structure. Instead, we list categories of modules (e. g. “Protection Functions”) and all the modules within a category.

For each parameter, there is a table with its properties, looking like this:

Module . Parameter	[Menu Path to This Parameter]	
Default Value For some parameters: • Availability restrictions	Value Range	Perm.
Type	*Short descriptive text explaining the functionality of this parameter.*	

“Type” is the data type of the parameter, which is denoted by a small icon. The following types are possible:

- Setting Parameter
- Direct Control
- Input State
- Signal (Output State)
- Statistical Value
- Counter
- (Measuring) Value
- Dialog — Such a dialog can feature several data objects using a special representation and/or functionality.

“Perm.” means “permission”, i. e. the access level and password that is required to modify the parameter. (Please refer to the “Security” chapter in the full Technical Manual for details.)

“ Adapt. Param.” means that this parameter supports Adaptive Parameter Sets. (See the “Adaptive Parameter Sets” section in the User Manual.)

For some parameter types (e. g. Input and Output States), the second row (default, value range, permission) is useless and therefore omitted.

Example of a parameter:

I[1] . **Mode**	[Device planning]	
non directional	Selection List Mode: -, non directional, forward, reverse	S.3
	general operation mode	

This means that one can find the parameter in the menu [Device planning], and its values are picked from a selection list named “Mode”. The “⮡” arrow indicates a cross-reference (hyperlink) into the “Selection Lists” chapter, and a click takes you to a table that lists all available choices. The access level “S.3” means the access level “Supervisor-Lv3”, which is required to modify the parameter.

Audience of This Manual

The manual serves as working basis for:

- Engineers in the protection field,
- commissioning engineers,
- people dealing with setting, testing and maintenance of protection and control devices,
- as well as trained personnel for electrical installations and power stations.

All functions concerning the MRU4 are listed. Should there be a description of any functions, parameters or inputs/outputs which do not apply to the device in use, please ignore that information.

This manual describes the (optionally) full featured versions of the devices.

All technical information and data included in this manual reflect their state at the time this document was issued. We reserve the right to carry out technical modifications in line with further development without changing this manual and without previous notice. Hence no claim can be brought based on the information and descriptions this manual includes.

We do not accept any liability for damage and operational failures caused by operating errors or disregarding the directions of this manual.

No part of this manual is allowed to be reproduced or passed on to others in any form, unless *Woodward* have approved in writing.

This Reference Manual is part of the delivery scope when purchasing the device. In case the device is passed on (sold) to a third party, the manual has to be handed over as well.

Information Concerning Liability and Warranty

Woodward does not accept any liability for damage resulting from conversions or changes carried out on the device or planning (projecting) work, parameter setting or adjustment changes done by the customer.

The warranty expires after a device has been opened by others than *Woodward* specialists.

Warranty and liability conditions stated in *Woodward* General Terms and Conditions are not supplemented by the above mentioned explanations.

2 Hardware

2.1 Device Configuration

Voltage Protection						
MRU4	**-2**	**#**	**#**	**#**	**#**	**#**
Hardware Variant 1						
8 digital inputs | 6 binary output relays Operating Range | Voltage measuring inputs: 0-800VAC		**A**				
Hardware Variant 2						
Standard			**0**			
Housing						
Flush mounting				**A**		
19 inch mounting (semi-flush)				**B**		
Customized Version 1				**H**		
Customized Version 2				**K**		
Communication						
Without					**A**	
RS 485: Modbus RTU | IEC 60870-5-103 | DNP3 RTU					**B**	
Ethernet: Modbus TCP | DNP3 UDP/TCP | IEC 60870-5-104					**C**	
Fiber Optics: Profibus-DP					**D**	
D-SUB: Profibus-DP					**E**	
Fiber Optics: Modbus RTU | IEC 60870-5-103 | DNP3 RTU					**F**	
RS 485/D-SUB: Modbus RTU | IEC 60870-5-103 | DNP3 RTU					**G**	
Ethernet: IEC 61850 communication | Modbus TCP | DNP3 UDP/TCP | IEC 60870-5-104					**H**	
RS 485, Ethernet: Modbus TCP/RTU | IEC 60870-5-103 | IEC 60870-5-104 | DNP3 UDP/TCP/RTU					**I**	
Ethernet/Fiber Optics: IEC 61850 communication | Modbus TCP | DNP3 UDP/TCP | IEC 60870-5-104					**K**	
Ethernet/Fiber Optics: Modbus TCP | DNP3 UDP/TCP | IEC 60870-5-104					**L**	
RS 485, Ethernet: IEC 61850 | Modbus TCP/RTU | IEC 60870-5-103 | IEC 60870-5-104 | DNP3 UDP/TCP/RTU					**T**	
Printed Circuit Board						
Standard						**A**

Voltage Protection						
MRU4	**-2**	**#**	**#**	**#**	**#**	**#**
printed circuit boards are conformal coated						**B**

2.2 Digital Inputs

2.2.1 DI Slot X1 (“DI8-X1”)

DI Slot X1 . **Nom voltage**	[Device Para / Digital Inputs / DI Slot X1 / Group 1] [Device Para / Digital Inputs / DI Slot X1 / Group 2] [Device Para / Digital Inputs / DI Slot X1 / Group 3]	
24 VDC	24 VDC, 48 VDC, 60 VDC, 110 VDC, 230 VDC, 110 VAC, 230 VAC ↳ Nom voltage.	S.3
Nominal voltage of the digital inputs		

DI Slot X1 . **Inverting 1** **...** DI Slot X1 . **Inverting 8**	[Device Para / Digital Inputs / DI Slot X1 / Group 1] [Device Para / Digital Inputs / DI Slot X1 / Group 2] [Device Para / Digital Inputs / DI Slot X1 / Group 3]	
inactive	inactive, active ↳ Mode.	S.3
Inverting the input signals.		

DI Slot X1 . **Debouncing time 1** **...** DI Slot X1 . **Debouncing time 8**	[Device Para / Digital Inputs / DI Slot X1 / Group 1] [Device Para / Digital Inputs / DI Slot X1 / Group 2] [Device Para / Digital Inputs / DI Slot X1 / Group 3]	
no debouncing time	no debouncing time, 20 ms, 50 ms, 100 ms ↳ Debouncing time.	S.3
A change of the state of a digital input will only be recognized after the debouncing time has expired (become effective). Thus, transient signals will not be misinterpreted.		

DI Slot X1 . **DI 1** **...** DI Slot X1 . **DI 8**	[Device Para / Digital Inputs / DI Slot X1 / Group 1] [Device Para / Digital Inputs / DI Slot X1 / Group 2] [Device Para / Digital Inputs / DI Slot X1 / Group 3]
Signal: Digital Input	

2.3 Binary Outputs

2.3.1 BO Slot X2 (6 Binary Outputs)

BO Slot X2 . **Operating Mode**	[Device Para / Binary Outputs / BO Slot X2 / BO 1]	
Normally open (NO)	Normally open (NO), Normally closed (NC) ↳ 1...n Operating Modes.	S.3
Operating Mode		

BO Slot X2 . **t-hold**	[Device Para / Binary Outputs / BO Slot X2 / BO 1]	
0.00s	0.00s . . . 300.00s	S.3
To clearly identify the state transition of a binary output relay, the "new state" is being hold, at least for the duration of the hold time.		

BO Slot X2 . **t-Off Delay**	[Device Para / Binary Outputs / BO Slot X2 / BO 1]	
0.00s	0.00s . . . 300.00s	S.3
Switch Off Delay		

BO Slot X2 . **Latched**	[Device Para / Binary Outputs / BO Slot X2 / BO 1]	
inactive	inactive, active ↳ Mode.	S.3
Defines whether the Relay Output will be latched when it picks up.		

BO Slot X2 . **Acknowledgement**	[Device Para / Binary Outputs / BO Slot X2 / BO 1]	
“-” *Only available if:* • BO Slot X2 . Latched = active	“-” . . . Sys . Internal test state ↳ 1..n, Assignment List.	S.3
Acknowledgement Signal - An acknowledgement signal (that acknowledges the corresponding binary output relay) can be assigned to each output relay. The acknowledgement-signal is only effective if the parameter "Latched" is set to active.		

BO Slot X2 . **Inverting**	[Device Para / Binary Outputs / BO Slot X2 / BO 1]	
inactive	inactive, active ↳ Mode.	S.3
Inverting of the collective signal (OR-gate/disjunction). In combination with inverted input signals an AND-gate can be programmed (Conjunction).		

BO Slot X2 . **Assignment 1**	[Device Para / Binary Outputs / BO Slot X2 / BO 1]	
SG[1] . TripCmd	“-” . . . Sys . Internal test state ↳ 1..n, Assignment List.	S.3
Assignment		

BO Slot X2 . **Inverting 1** . . . BO Slot X2 . **Inverting 7**	[Device Para / Binary Outputs / BO Slot X2 / BO 1]	
inactive	inactive, active ↳ Mode.	S.3
Inverting of the state of the assigned signal.		

BO Slot X2 . **Assignment 2** . . . BO Slot X2 . **Assignment 7**	[Device Para / Binary Outputs / BO Slot X2 / BO 1]	
“-”	“-” . . . Sys . Internal test state ↳ 1..n, Assignment List.	S.3
Assignment		

BO Slot X2 . **Operating Mode**	[Device Para / Binary Outputs / BO Slot X2 / BO 2]	
Normally open (NO)	Normally open (NO), Normally closed (NC) ↳ 1...n Operating Modes.	S.3
Operating Mode		

BO Slot X2 . **t-hold**	[Device Para / Binary Outputs / BO Slot X2 / BO 2]	
0.00s	0.00s . . . 300.00s	S.3
To clearly identify the state transition of a binary output relay, the "new state" is being hold, at least for the duration of the hold time.		

BO Slot X2 . **t-Off Delay**	[Device Para / Binary Outputs / BO Slot X2 / BO 2]	
0.00s	0.00s . . . 300.00s	S.3
Switch Off Delay		

BO Slot X2 . **Latched**	[Device Para / Binary Outputs / BO Slot X2 / BO 2]	
inactive	inactive, active ↳ Mode.	S.3
Defines whether the Relay Output will be latched when it picks up.		

BO Slot X2 . **Acknowledgement**	[Device Para / Binary Outputs / BO Slot X2 / BO 2]	
"-" *Only available if:* • BO Slot X2 . Latched = active	"-" . . . Sys . Internal test state ↳ 1..n, Assignment List.	S.3
Acknowledgement Signal - An acknowledgement signal (that acknowledges the corresponding binary output relay) can be assigned to each output relay. The acknowledgement-signal is only effective if the parameter "Latched" is set to active.		

BO Slot X2 . **Inverting**	[Device Para / Binary Outputs / BO Slot X2 / BO 2]	
inactive	inactive, active ↳ Mode.	S.3
Inverting of the collective signal (OR-gate/disjunction). In combination with inverted input signals an AND-gate can be programmed (Conjunction).		

BO Slot X2 . **Assignment 1**	[Device Para / Binary Outputs / BO Slot X2 / BO 2]	
Prot . Alarm	"-" . . . Sys . Internal test state ↳ 1..n, Assignment List.	S.3
Assignment		

BO Slot X2 . **Inverting 1** **. . .** BO Slot X2 . **Inverting 7**	[Device Para / Binary Outputs / BO Slot X2 / BO 2]	
inactive	inactive, active ↳ Mode.	S.3
Inverting of the state of the assigned signal.		

BO Slot X2 . **Assignment 2** **...** BO Slot X2 . **Assignment 7**	[Device Para / Binary Outputs / BO Slot X2 / BO 2]	
"-"	"-" ... Sys . Internal test state ↳ 1..n, Assignment List.	S.3
Assignment		

BO Slot X2 . **Operating Mode**	[Device Para / Binary Outputs / BO Slot X2 / BO 3]	
Normally open (NO)	Normally open (NO), Normally closed (NC) ↳ 1...n Operating Modes.	S.3
Operating Mode		

BO Slot X2 . **t-hold**	[Device Para / Binary Outputs / BO Slot X2 / BO 3]	
0.00s	0.00s ... 300.00s	S.3
To clearly identify the state transition of a binary output relay, the "new state" is being hold, at least for the duration of the hold time.		

BO Slot X2 . **t-Off Delay**	[Device Para / Binary Outputs / BO Slot X2 / BO 3]	
0.00s	0.00s ... 300.00s	S.3
Switch Off Delay		

BO Slot X2 . **Latched**	[Device Para / Binary Outputs / BO Slot X2 / BO 3]	
inactive	inactive, active ↳ Mode.	S.3
Defines whether the Relay Output will be latched when it picks up.		

BO Slot X2 . **Acknowledgement**	[Device Para / Binary Outputs / BO Slot X2 / BO 3]	
"-" *Only available if:* • BO Slot X2 . Latched = active	"-" ... Sys . Internal test state ↳ 1..n, Assignment List.	S.3
Acknowledgement Signal - An acknowledgement signal (that acknowledges the corresponding binary output relay) can be assigned to each output relay. The acknowledgement-signal is only effective if the parameter "Latched" is set to active.		

BO Slot X2 . **Inverting**	[Device Para / Binary Outputs / BO Slot X2 / BO 3]	
inactive	inactive, active ↳ Mode.	S.3
Inverting of the collective signal (OR-gate/disjunction). In combination with inverted input signals an AND-gate can be programmed (Conjunction).		

BO Slot X2 . **Assignment 1**	[Device Para / Binary Outputs / BO Slot X2 / BO 3]	
SG[1] . ON Cmd	"-" . . . Sys . Internal test state ↳ 1..n, Assignment List.	S.3
Assignment		

BO Slot X2 . **Inverting 1** **. . .** BO Slot X2 . **Inverting 7**	[Device Para / Binary Outputs / BO Slot X2 / BO 3]	
inactive	inactive, active ↳ Mode.	S.3
Inverting of the state of the assigned signal.		

BO Slot X2 . **Assignment 2** **. . .** BO Slot X2 . **Assignment 7**	[Device Para / Binary Outputs / BO Slot X2 / BO 3]	
"-"	"-" . . . Sys . Internal test state ↳ 1..n, Assignment List.	S.3
Assignment		

BO Slot X2 . **Operating Mode**	[Device Para / Binary Outputs / BO Slot X2 / BO 4]	
Normally open (NO)	Normally open (NO), Normally closed (NC) ↳ 1...n Operating Modes.	S.3
Operating Mode		

BO Slot X2 . **t-hold**	[Device Para / Binary Outputs / BO Slot X2 / BO 4]	
0.00s	0.00s ... 300.00s	S.3
To clearly identify the state transition of a binary output relay, the "new state" is being hold, at least for the duration of the hold time.		

BO Slot X2 . **t-Off Delay**	[Device Para / Binary Outputs / BO Slot X2 / BO 4]	
0.00s	0.00s ... 300.00s	S.3
Switch Off Delay		

BO Slot X2 . **Latched**	[Device Para / Binary Outputs / BO Slot X2 / BO 4]	
inactive	inactive, active ↳ Mode.	S.3
Defines whether the Relay Output will be latched when it picks up.		

BO Slot X2 . **Acknowledgement**	[Device Para / Binary Outputs / BO Slot X2 / BO 4]	
"-" *Only available if:* • BO Slot X2 . Latched = active	"-" ... Sys . Internal test state ↳ 1..n, Assignment List.	S.3
Acknowledgement Signal - An acknowledgement signal (that acknowledges the corresponding binary output relay) can be assigned to each output relay. The acknowledgement-signal is only effective if the parameter "Latched" is set to active.		

BO Slot X2 . **Inverting**	[Device Para / Binary Outputs / BO Slot X2 / BO 4]	
inactive	inactive, active ↳ Mode.	S.3
Inverting of the collective signal (OR-gate/disjunction). In combination with inverted input signals an AND-gate can be programmed (Conjunction).		

BO Slot X2 . **Assignment 1**	[Device Para / Binary Outputs / BO Slot X2 / BO 4]	
SG[1] . OFF Cmd	"-" ... Sys . Internal test state ↳ 1..n, Assignment List.	S.3
Assignment		

BO Slot X2 . **Inverting 1** **...** BO Slot X2 . **Inverting 7**	[Device Para / Binary Outputs / BO Slot X2 / BO 4]	
inactive	inactive, active ↳ Mode.	S.3
Inverting of the state of the assigned signal.		

BO Slot X2 . **Assignment 2** **...** BO Slot X2 . **Assignment 7**	[Device Para / Binary Outputs / BO Slot X2 / BO 4]	
“-”	“-” ... Sys . Internal test state ↳ 1..n, Assignment List.	S.3
Assignment		

BO Slot X2 . **Operating Mode**	[Device Para / Binary Outputs / BO Slot X2 / BO 5]	
Normally open (NO)	Normally open (NO), Normally closed (NC) ↳ 1...n Operating Modes.	S.3
Operating Mode		

BO Slot X2 . **t-hold**	[Device Para / Binary Outputs / BO Slot X2 / BO 5]	
0.00s	0.00s ... 300.00s	S.3
To clearly identify the state transition of a binary output relay, the "new state" is being hold, at least for the duration of the hold time.		

BO Slot X2 . **t-Off Delay**	[Device Para / Binary Outputs / BO Slot X2 / BO 5]	
0.00s	0.00s ... 300.00s	S.3
Switch Off Delay		

BO Slot X2 . **Latched**	[Device Para / Binary Outputs / BO Slot X2 / BO 5]	
inactive	inactive, active ↳ Mode.	S.3
Defines whether the Relay Output will be latched when it picks up.		

BO Slot X2 . **Acknowledgement**	[Device Para / Binary Outputs / BO Slot X2 / BO 5]	
"-" *Only available if:* • BO Slot X2 . Latched = active	"-" . . . Sys . Internal test state ↳ 1..n, Assignment List.	S.3
Acknowledgement Signal - An acknowledgement signal (that acknowledges the corresponding binary output relay) can be assigned to each output relay. The acknowledgement-signal is only effective if the parameter "Latched" is set to active.		

BO Slot X2 . **Inverting**	[Device Para / Binary Outputs / BO Slot X2 / BO 5]	
inactive	inactive, active ↳ Mode.	S.3
Inverting of the collective signal (OR-gate/disjunction). In combination with inverted input signals an AND-gate can be programmed (Conjunction).		

BO Slot X2 . **Assignment 1** **. . .** BO Slot X2 . **Assignment 7**	[Device Para / Binary Outputs / BO Slot X2 / BO 5]	
"-"	"-" . . . Sys . Internal test state ↳ 1..n, Assignment List.	S.3
Assignment		

BO Slot X2 . **Inverting 1** **. . .** BO Slot X2 . **Inverting 7**	[Device Para / Binary Outputs / BO Slot X2 / BO 5]	
inactive	inactive, active ↳ Mode.	S.3
Inverting of the state of the assigned signal.		

2.3.1.1 BO Slot X2: Service

BO Slot X2 . **DISARMED Ctrl**	[Service / Test (Prot inhibit) / DISARMED / BO Slot X2]	
inactive	inactive, active ↳ active/inactive.	S.3
Enables and disables the disarming of the relay outputs. This is the first step of a two step process, to inhibit the operation or the relay outputs. Please refer to "DISARMED" for the second step.		

BO Slot X2 . **Disarm Mode**	[Service / Test (Prot inhibit) / DISARMED / BO Slot X2]	
permanent	permanent, timeout ↳ Mode.	S.3
CAUTION! RELAYS DISARMED in order to safely perform maintenance while eliminating the risk of taking an entire process off-line. (Note: The Supervision Contact cannot be disarmed). YOU MUST ENSURE that the relays are ARMED AGAIN after maintenance.		

BO Slot X2 . **t-Timeout DISARM**	[Service / Test (Prot inhibit) / DISARMED / BO Slot X2]	
0.03s *Only available if:* • BO Slot X2 . Disarm Mode = timeout	0.00s ... 300.00s	S.3
The relays will be armed again after expiring of this time.		

BO Slot X2 . **DISARMED**	[Service / Test (Prot inhibit) / DISARMED / BO Slot X2]	
inactive	inactive, active ↳ active/inactive.	S.3
This is the second step, after the "DISARMED Ctrl" has been activated, that is required to DISARM the relay outputs. This will DISARM those output relays that are currently not latched and that are not on “hold” by a pending minimum hold time. CAUTION! RELAYS DISARMED in order to safely perform maintenance while eliminating the risk of taking an entire process off-line. (Note: Zone Interlocking and Supervision Contact cannot be disarmed). YOU MUST ENSURE that the relays are ARMED AGAIN after maintenance.		

BO Slot X2 . **Force Mode**	[Service / Test (Prot inhibit) / Force OR / BO Slot X2]	
permanent	permanent, timeout ↳ Mode.	S.3

By means of this function the normal Output Relay States can be overwritten (forced) in case that the Relay is not in a disarmed state. The relays can be set from normal operation (relay works according to the assigned signals) to "force energized" or "force de-energized" state.

BO Slot X2 . **t-Timeout Force**	[Service / Test (Prot inhibit) / Force OR / BO Slot X2]	
0.03s *Only available if:* • BO Slot X2 . Force Mode = timeout	0.00s . . . 300.00s	S.3

The Output State will be set by force for the duration of this time. That means for the duration of this time the Output Relay does not show the state of the signals that are assigned on it.

BO Slot X2 . **Force all Outs**	[Service / Test (Prot inhibit) / Force OR / BO Slot X2]	
Normal	Normal, De-Energized, Energized ↳ Relay operating modes.	S.3

By means of this function the normal Output Relay State can be overwritten (forced). The relay can be set from normal operation (relay works according to the assigned signals) to "force energized" or "force de-energized" state. Forcing all outputs relays of an entire assembly group is superior to forcing a single output relay.

BO Slot X2 . **Force OR1** **. . .** BO Slot X2 . **Force OR5**	[Service / Test (Prot inhibit) / Force OR / BO Slot X2]	
Normal	Normal, De-Energized, Energized ↳ Relay operating modes.	S.3

By means of this function the normal Output Relay State can be overwritten (forced). The relay can be set from normal operation (relay works according to the assigned signals) to "force energized" or "force de-energized" state.

2.4 LEDs

2.4.1 LED 1

LEDs group A . **Latched**	[Device Para / LEDs / LED 1]	
inactive	inactive, active, active, ack. by alarm ↳ Mode.	S.3
Defines whether the LED will be latched when it picks up.		

LEDs group A . **Ack signal**	[Device Para / LEDs / LED 1]	
“-”	“-” . . . Sys . Internal test state ↳ 1..n, Assignment List.	S.3
Acknowledgement signal for the LED. If latching is set to active the LED can only be acknowledged if those signals that initiated the setting are no longer present.		

LEDs group A . **LED active color**	[Device Para / LEDs / LED 1]	
green	green, red, red flash, green flash, “-” ↳ LED active color.	S.3
The LED lights up in this color if the state of the OR-assignment of the signals is true.		

LEDs group A . **LED inactive color**	[Device Para / LEDs / LED 1]	
“-”	green, red, red flash, green flash, “-” ↳ LED active color.	S.3
The LED lights up in this color if the state of the OR-assignment of the signals is untrue.		

LEDs group A . **Assignment 1**	[Device Para / LEDs / LED 1]	
Prot . active	“-” . . . Sys . Internal test state ↳ 1..n, Assignment List.	S.3
Assignment		

LEDs group A . **Inverting 1**	[Device Para / LEDs / LED 1]	
inactive	inactive, active ↳ Mode.	S.3
Inverting of the state of the assigned signal.		

LEDs group A . **Assignment 2**	[Device Para / LEDs / LED 1]	
“-”	“-” . . . Sys . Internal test state ↳ 1..n, Assignment List.	S.3
Assignment		

LEDs group A . **Inverting 2**	[Device Para / LEDs / LED 1]	
inactive	inactive, active ↳ Mode.	S.3
Inverting of the state of the assigned signal.		

LEDs group A . **Assignment 3**	[Device Para / LEDs / LED 1]	
“-”	“-” . . . Sys . Internal test state ↳ 1..n, Assignment List.	S.3
Assignment		

LEDs group A . **Inverting 3**	[Device Para / LEDs / LED 1]	
inactive	inactive, active ↳ Mode.	S.3
Inverting of the state of the assigned signal.		

LEDs group A . **Assignment 4**	[Device Para / LEDs / LED 1]	
“-”	“-” . . . Sys . Internal test state ↳ 1..n, Assignment List.	S.3
Assignment		

LEDs group A . **Inverting 4**	[Device Para / LEDs / LED 1]	
inactive	inactive, active ↳ Mode.	S.3
Inverting of the state of the assigned signal.		

LEDs group A . **Assignment 5**	[Device Para / LEDs / LED 1]	
“-”	“-” . . . Sys . Internal test state ↳ 1..n, Assignment List.	S.3
Assignment		

LEDs group A . **Inverting 5**	[Device Para / LEDs / LED 1]	
inactive	inactive, active ↳ Mode.	S.3
Inverting of the state of the assigned signal.		

2.4.2 LED 2

LEDs group A . **Latched**	[Device Para / LEDs / LED 2]	
active	inactive, active, active, ack. by alarm ↳ Mode.	S.3
Defines whether the LED will be latched when it picks up.		

LEDs group A . **Ack signal**	[Device Para / LEDs / LED 2]	
“-”	“-” . . . Sys . Internal test state ↳ 1..n, Assignment List.	S.3
Acknowledgement signal for the LED. If latching is set to active the LED can only be acknowledged if those signals that initiated the setting are no longer present.		

LEDs group A . **LED active color**	[Device Para / LEDs / LED 2]	
red	green, red, red flash, green flash, “-” ↳ LED active color.	S.3
The LED lights up in this color if the state of the OR-assignment of the signals is true.		

LEDs group A . **LED inactive color**	[Device Para / LEDs / LED 2]	
“-”	green, red, red flash, green flash, “-” ↳ LED active color.	S.3
The LED lights up in this color if the state of the OR-assignment of the signals is untrue.		

LEDs group A . **Assignment 1**	[Device Para / LEDs / LED 2]	
SG[1] . TripCmd	“-” . . . Sys . Internal test state ↳ 1..n, Assignment List.	S.3
Assignment		

LEDs group A . **Inverting 1**	[Device Para / LEDs / LED 2]	
inactive	inactive, active ↳ Mode.	S.3
Inverting of the state of the assigned signal.		

LEDs group A . **Assignment 2**	[Device Para / LEDs / LED 2]	
“-”	“-” . . . Sys . Internal test state ↳ 1..n, Assignment List.	S.3
Assignment		

LEDs group A . **Inverting 2**	[Device Para / LEDs / LED 2]	
inactive	inactive, active ↳ Mode.	S.3
Inverting of the state of the assigned signal.		

LEDs group A . **Assignment 3**	[Device Para / LEDs / LED 2]	
“-”	“-” . . . Sys . Internal test state ↳ 1..n, Assignment List.	S.3
Assignment		

LEDs group A . **Inverting 3**	[Device Para / LEDs / LED 2]	
inactive	inactive, active ↳ Mode.	S.3
Inverting of the state of the assigned signal.		

LEDs group A . **Assignment 4**	[Device Para / LEDs / LED 2]	
“-”	“-” . . . Sys . Internal test state ↳ 1..n, Assignment List.	S.3
Assignment		

LEDs group A . **Inverting 4**	[Device Para / LEDs / LED 2]	
inactive	inactive, active ↳ Mode.	S.3
Inverting of the state of the assigned signal.		

LEDs group A . **Assignment 5**	[Device Para / LEDs / LED 2]	
“-”	“-” . . . Sys . Internal test state ↳ 1..n, Assignment List.	S.3
Assignment		

LEDs group A . **Inverting 5**	[Device Para / LEDs / LED 2]	
inactive	inactive, active ↳ Mode.	S.3
Inverting of the state of the assigned signal.		

2.4.3 LED 3

LEDs group A . **Latched**	[Device Para / LEDs / LED 3]	
inactive	inactive, active, active, ack. by alarm ↳ Mode.	S.3
Defines whether the LED will be latched when it picks up.		

LEDs group A . **Ack signal**	[Device Para / LEDs / LED 3]	
"-"	"-" . . . Sys . Internal test state ↳ 1..n, Assignment List.	S.3
Acknowledgement signal for the LED. If latching is set to active the LED can only be acknowledged if those signals that initiated the setting are no longer present.		

LEDs group A . **LED active color**	[Device Para / LEDs / LED 3]	
red flash	green, red, red flash, green flash, "-" ↳ LED active color.	S.3
The LED lights up in this color if the state of the OR-assignment of the signals is true.		

LEDs group A . **LED inactive color**	[Device Para / LEDs / LED 3]	
"-"	green, red, red flash, green flash, "-" ↳ LED active color.	S.3
The LED lights up in this color if the state of the OR-assignment of the signals is untrue.		

LEDs group A . **Assignment 1**	[Device Para / LEDs / LED 3]	
Prot . Alarm	"-" . . . Sys . Internal test state ↳ 1..n, Assignment List.	S.3
Assignment		

LEDs group A . **Inverting 1**	[Device Para / LEDs / LED 3]	
inactive	inactive, active ↳ Mode.	S.3
Inverting of the state of the assigned signal.		

LEDs group A . **Assignment 2**	[Device Para / LEDs / LED 3]	
“-”	“-” . . . Sys . Internal test state ↳ 1..n, Assignment List.	S.3
Assignment		

LEDs group A . **Inverting 2**	[Device Para / LEDs / LED 3]	
inactive	inactive, active ↳ Mode.	S.3
Inverting of the state of the assigned signal.		

LEDs group A . **Assignment 3**	[Device Para / LEDs / LED 3]	
“-”	“-” . . . Sys . Internal test state ↳ 1..n, Assignment List.	S.3
Assignment		

LEDs group A . **Inverting 3**	[Device Para / LEDs / LED 3]	
inactive	inactive, active ↳ Mode.	S.3
Inverting of the state of the assigned signal.		

LEDs group A . **Assignment 4**	[Device Para / LEDs / LED 3]	
“-”	“-” . . . Sys . Internal test state ↳ 1..n, Assignment List.	S.3
Assignment		

LEDs group A . **Inverting 4**	[Device Para / LEDs / LED 3]	
inactive	inactive, active ↳ Mode.	S.3
Inverting of the state of the assigned signal.		

LEDs group A . **Assignment 5**	[Device Para / LEDs / LED 3]	
“-”	“-” . . . Sys . Internal test state ↳ 1..n, Assignment List.	S.3
Assignment		

LEDs group A . **Inverting 5**	[Device Para / LEDs / LED 3]	
inactive	inactive, active ↳ Mode.	S.3
Inverting of the state of the assigned signal.		

2.4.4 LED 4

LEDs group A . **Latched**	[Device Para / LEDs / LED 4]	
inactive	inactive, active, active, ack. by alarm ↳ Mode.	S.3
Defines whether the LED will be latched when it picks up.		

LEDs group A . **Ack signal**	[Device Para / LEDs / LED 4]	
“-”	“-” . . . Sys . Internal test state ↳ 1..n, Assignment List.	S.3
Acknowledgement signal for the LED. If latching is set to active the LED can only be acknowledged if those signals that initiated the setting are no longer present.		

LEDs group A . **LED active color**	[Device Para / LEDs / LED 4]	
red	green, red, red flash, green flash, “-” ↳ LED active color.	S.3
The LED lights up in this color if the state of the OR-assignment of the signals is true.		

LEDs group A . **LED inactive color**	[Device Para / LEDs / LED 4]	
“-”	green, red, red flash, green flash, “-” ↳ LED active color.	S.3
The LED lights up in this color if the state of the OR-assignment of the signals is untrue.		

LEDs group A . **Assignment 1**	[Device Para / LEDs / LED 4]	
“-”	“-” . . . Sys . Internal test state ↳ 1..n, Assignment List.	S.3
Assignment		

LEDs group A . **Inverting 1**	[Device Para / LEDs / LED 4]	
inactive	inactive, active ↳ Mode.	S.3
Inverting of the state of the assigned signal.		

LEDs group A . **Assignment 2**	[Device Para / LEDs / LED 4]	
“-”	“-” . . . Sys . Internal test state ↳ 1..n, Assignment List.	S.3
Assignment		

LEDs group A . **Inverting 2**	[Device Para / LEDs / LED 4]	
inactive	inactive, active ↳ Mode.	S.3
Inverting of the state of the assigned signal.		

LEDs group A . **Assignment 3**	[Device Para / LEDs / LED 4]	
“-”	“-” . . . Sys . Internal test state ↳ 1..n, Assignment List.	S.3
Assignment		

LEDs group A . **Inverting 3**	[Device Para / LEDs / LED 4]	
inactive	inactive, active ↳ Mode.	S.3
Inverting of the state of the assigned signal.		

LEDs group A . **Assignment 4**	[Device Para / LEDs / LED 4]	
“-”	“-” . . . Sys . Internal test state ↳ 1..n, Assignment List.	S.3
Assignment		

LEDs group A . **Inverting 4**	[Device Para / LEDs / LED 4]	
inactive	inactive, active ↳ Mode.	S.3
Inverting of the state of the assigned signal.		

LEDs group A . **Assignment 5**	[Device Para / LEDs / LED 4]	
“-”	“-” . . . Sys . Internal test state ↳ 1..n, Assignment List.	S.3
Assignment		

LEDs group A . **Inverting 5**	[Device Para / LEDs / LED 4]	
inactive	inactive, active ↳ Mode.	S.3
Inverting of the state of the assigned signal.		

2.4.5 LED 5

LEDs group A . **Latched**	[Device Para / LEDs / LED 5]	
inactive	inactive, active, active, ack. by alarm ↳ Mode.	S.3
Defines whether the LED will be latched when it picks up.		

LEDs group A . **Ack signal**	[Device Para / LEDs / LED 5]	
"-"	"-" . . . Sys . Internal test state ↳ 1..n, Assignment List.	S.3
Acknowledgement signal for the LED. If latching is set to active the LED can only be acknowledged if those signals that initiated the setting are no longer present.		

LEDs group A . **LED active color**	[Device Para / LEDs / LED 5]	
red	green, red, red flash, green flash, "-" ↳ LED active color.	S.3
The LED lights up in this color if the state of the OR-assignment of the signals is true.		

LEDs group A . **LED inactive color**	[Device Para / LEDs / LED 5]	
"-"	green, red, red flash, green flash, "-" ↳ LED active color.	S.3
The LED lights up in this color if the state of the OR-assignment of the signals is untrue.		

LEDs group A . **Assignment 1**	[Device Para / LEDs / LED 5]	
"-"	"-" . . . Sys . Internal test state ↳ 1..n, Assignment List.	S.3
Assignment		

LEDs group A . **Inverting 1**	[Device Para / LEDs / LED 5]	
inactive	inactive, active ↳ Mode.	S.3
Inverting of the state of the assigned signal.		

LEDs group A . **Assignment 2**	[Device Para / LEDs / LED 5]	
“-”	“-” . . . Sys . Internal test state ↳ 1..n, Assignment List.	S.3
Assignment		

LEDs group A . **Inverting 2**	[Device Para / LEDs / LED 5]	
inactive	inactive, active ↳ Mode.	S.3
Inverting of the state of the assigned signal.		

LEDs group A . **Assignment 3**	[Device Para / LEDs / LED 5]	
“-”	“-” . . . Sys . Internal test state ↳ 1..n, Assignment List.	S.3
Assignment		

LEDs group A . **Inverting 3**	[Device Para / LEDs / LED 5]	
inactive	inactive, active ↳ Mode.	S.3
Inverting of the state of the assigned signal.		

LEDs group A . **Assignment 4**	[Device Para / LEDs / LED 5]	
“-”	“-” . . . Sys . Internal test state ↳ 1..n, Assignment List.	S.3
Assignment		

LEDs group A . **Inverting 4**	[Device Para / LEDs / LED 5]	
inactive	inactive, active ↳ Mode.	S.3
Inverting of the state of the assigned signal.		

LEDs group A . **Assignment 5**	[Device Para / LEDs / LED 5]	
“-”	“-” . . . Sys . Internal test state ↳ 1..n, Assignment List.	S.3
Assignment		

LEDs group A . **Inverting 5**	[Device Para / LEDs / LED 5]	
inactive	inactive, active ↳ Mode.	S.3
Inverting of the state of the assigned signal.		

2.4.6 LED 6

LEDs group A . **Latched**	[Device Para / LEDs / LED 6]	
inactive	inactive, active, active, ack. by alarm ↳ Mode.	S.3
Defines whether the LED will be latched when it picks up.		

LEDs group A . **Ack signal**	[Device Para / LEDs / LED 6]	
“-”	“-” . . . Sys . Internal test state ↳ 1..n, Assignment List.	S.3
Acknowledgement signal for the LED. If latching is set to active the LED can only be acknowledged if those signals that initiated the setting are no longer present.		

LEDs group A . **LED active color**	[Device Para / LEDs / LED 6]	
red	green, red, red flash, green flash, “-” ↳ LED active color.	S.3
The LED lights up in this color if the state of the OR-assignment of the signals is true.		

LEDs group A . **LED inactive color**	[Device Para / LEDs / LED 6]	
“-”	green, red, red flash, green flash, “-” ↳ LED active color.	S.3
The LED lights up in this color if the state of the OR-assignment of the signals is untrue.		

LEDs group A . **Assignment 1**	[Device Para / LEDs / LED 6]	
“-”	“-” . . . Sys . Internal test state ↳ 1..n, Assignment List.	S.3
Assignment		

LEDs group A . **Inverting 1**	[Device Para / LEDs / LED 6]	
inactive	inactive, active ↳ Mode.	S.3
Inverting of the state of the assigned signal.		

LEDs group A . **Assignment 2**	[Device Para / LEDs / LED 6]	
“-”	“-” . . . Sys . Internal test state ↳ 1..n, Assignment List.	S.3
Assignment		

LEDs group A . **Inverting 2**	[Device Para / LEDs / LED 6]	
inactive	inactive, active ↳ Mode.	S.3
Inverting of the state of the assigned signal.		

LEDs group A . **Assignment 3**	[Device Para / LEDs / LED 6]	
“-”	“-” . . . Sys . Internal test state ↳ 1..n, Assignment List.	S.3
Assignment		

LEDs group A . **Inverting 3**	[Device Para / LEDs / LED 6]	
inactive	inactive, active ↳ Mode.	S.3
Inverting of the state of the assigned signal.		

LEDs group A . **Assignment 4**	[Device Para / LEDs / LED 6]	
“-”	“-” . . . Sys . Internal test state ↳ 1..n, Assignment List.	S.3
Assignment		

LEDs group A . **Inverting 4**	[Device Para / LEDs / LED 6]	
inactive	inactive, active ↳ Mode.	S.3
Inverting of the state of the assigned signal.		

LEDs group A . **Assignment 5**	[Device Para / LEDs / LED 6]	
“-”	“-” . . . Sys . Internal test state ↳ 1..n, Assignment List.	S.3
Assignment		

LEDs group A . **Inverting 5**	[Device Para / LEDs / LED 6]	
inactive	inactive, active ↳ Mode.	S.3
Inverting of the state of the assigned signal.		

2.4.7 LED 7

LEDs group A . **Latched**	[Device Para / LEDs / LED 7]	
inactive	inactive, active, active, ack. by alarm ↳ Mode.	S.3
Defines whether the LED will be latched when it picks up.		

LEDs group A . **Ack signal**	[Device Para / LEDs / LED 7]	
“-”	“-” . . . Sys . Internal test state ↳ 1..n, Assignment List.	S.3
Acknowledgement signal for the LED. If latching is set to active the LED can only be acknowledged if those signals that initiated the setting are no longer present.		

LEDs group A . **LED active color**	[Device Para / LEDs / LED 7]	
red	green, red, red flash, green flash, “-” ↳ LED active color.	S.3
The LED lights up in this color if the state of the OR-assignment of the signals is true.		

LEDs group A . **LED inactive color**	[Device Para / LEDs / LED 7]	
“-”	green, red, red flash, green flash, “-” ↳ LED active color.	S.3
The LED lights up in this color if the state of the OR-assignment of the signals is untrue.		

LEDs group A . **Assignment 1**	[Device Para / LEDs / LED 7]	
“-”	“-” . . . Sys . Internal test state ↳ 1..n, Assignment List.	S.3
Assignment		

LEDs group A . **Inverting 1**	[Device Para / LEDs / LED 7]	
inactive	inactive, active ↳ Mode.	S.3
Inverting of the state of the assigned signal.		

LEDs group A . **Assignment 2**	[Device Para / LEDs / LED 7]	
“-”	“-” . . . Sys . Internal test state ↳ 1..n, Assignment List.	S.3
Assignment		

LEDs group A . **Inverting 2**	[Device Para / LEDs / LED 7]	
inactive	inactive, active ↳ Mode.	S.3
Inverting of the state of the assigned signal.		

LEDs group A . **Assignment 3**	[Device Para / LEDs / LED 7]	
“-”	“-” . . . Sys . Internal test state ↳ 1..n, Assignment List.	S.3
Assignment		

LEDs group A . **Inverting 3**	[Device Para / LEDs / LED 7]	
inactive	inactive, active ↳ Mode.	S.3
Inverting of the state of the assigned signal.		

LEDs group A . **Assignment 4**	[Device Para / LEDs / LED 7]	
“-”	“-” . . . Sys . Internal test state ↳ 1..n, Assignment List.	S.3
Assignment		

LEDs group A . **Inverting 4**	[Device Para / LEDs / LED 7]	
inactive	inactive, active ↳ Mode.	S.3
Inverting of the state of the assigned signal.		

LEDs group A . **Assignment 5**	[Device Para / LEDs / LED 7]	
“-”	“-” . . . Sys . Internal test state ↳ 1..n, Assignment List.	S.3
Assignment		

LEDs group A . **Inverting 5**	[Device Para / LEDs / LED 7]	
inactive	inactive, active ↳ Mode.	S.3
Inverting of the state of the assigned signal.		

2.5 HMI

front-panel

Password	[Device Para / Security / Password]
This item represents a special dialog. (See the Technical Manual for details.) *Changing the password*	

Access Level	[Device Para / Security / Access Level]
This item represents a special dialog. (See the Technical Manual for details.) *Access Level*	

2.5.1 HMI: Global Parameters

HMI . **Display Off**	[Device Para / HMI]	
180s	20s ... 3600s	S.3
The display back light will be turned off when this timer has expired.		

HMI . **Menu language**	[Device Para / HMI]	
English	English ... Romanian ↳ Selection.	S.3
Selection of the language		

HMI . **Display ANSI Device No.**	[Device Para / HMI]	
active	inactive, active ↳ Mode.	S.3
Display ANSI Device Numbers		

HMI . **t-max Edit/Access**	[Device Para / Security / General Settings]	
180s	20s ... 3600s	S.3
If no other key(s) is pressed at the panel, after expiration of this time, all cached (changed) parameters are canceled. The device access will be locked by falling back into Read-only level Lv0.		

2.5.2 HMI: Direct Controls

HMI . **Contrast**	[Device Para / HMI]	
50%	0% ... 100%	S.3
◉	*Contrast*	

HMI . **Config. Device Reset**	[Device Para / Security / General Settings]	
"Fact.def.", "PW rst"	"Fact.def.", "PW rst", Only “Fact.defaults”, Reset deact. ↳ Config. Device Reset.	S.3
◉	*If the »C« key is pressed while the device is performing a cold restart a general Reset Dialog appears on the screen. Select which options shall be available with this dialog.*	

2.5.3 HMI: Values

HMI . **Config. Device Reset**	[Operation / Security / Security States]	
"Fact.def.", "PW rst"	"Fact.def.", "PW rst", Only “Fact.defaults”, Reset deact. ↳ Config. Device Reset.	
⟍	*If the »C« key is pressed while the device is performing a cold restart a general Reset Dialog appears on the screen. Select which options shall be available with this dialog.*	

3 Security

- Ctrl . Switching Authority: ⮡ Tab.
- HMI . Config. Device Reset: ⮡ Tab.
- HMI . t-max Edit/Access: ⮡ Tab.
- HMI . Config. Device Reset: ⮡ Tab.
- Password: ⮡ Tab.
- Access Level: ⮡ Tab.

Sys . **Smart view via USB**	[Operation / Security / Security States]	
active	inactive, active ⮡ Mode.	
✎	*Information whether or not the Smart view access via the USB interface is activated (allowed).*	

Sys . **Smart view via Eth**	[Operation / Security / Security States]	
active *Avail. depends on HW*	inactive, active ⮡ Mode.	
✎	*Information whether or not the Smart view access via the Ethernet interface is activated (allowed).*	

Sys . **Passw. for USB conn.**	[Operation / Security / Security States]	
disabled	disabled, default, def. by user ⮡ Type of passw. def..	
✎	*Type / Security-level of the connection password that is used for a USB connection.*	

Sys . **Passw.remote net.conn.**	[Operation / Security / Security States]	
disabled *Avail. depends on HW*	disabled, default, def. by user ⮡ Type of passw. def..	
✎	*Type / Security-level of the connection password that is used for a Smart view connection via some network interface.*	

Sys . **TLS Certificate**	[Operation / Security / Security States]	
Device-specific	Device-specific, Basic, Corrupt ↳ TLS Certificate.	
Type of certificate that the device uses for the encrypted communication. This value is directly related to the security-level of the communication.		

Security Logger	[Operation / Security / Security Logger]
This item represents a special dialog. (See the Technical Manual for details.) *Security-related messages*	

Sys . **Smart view via USB**	[Device Para / Security / Communication]	
active	inactive, active ↳ Mode.	S.3
Activate (allow) or inactivate (disallow) the Smart view access via the USB interface.		

Sys . **Smart view via Eth**	[Device Para / Security / Communication]	
active *Avail. depends on HW*	inactive, active ↳ Mode.	S.3
Activate (allow) or inactivate (disallow) the Smart view access via the Ethernet interface.		

4 Field settings

Field settings

4.1 Field Para: Global Parameters

Field Para . **Phase Sequence**	[Field Para / General Settings]	
ABC	ABC, ACB ↳ Phase Sequence.	S.3
Phase Sequence direction		

Field Para . **f**	[Field Para / General Settings]	
50Hz	50Hz, 60Hz ↳ fN.	S.3
Nominal frequency		

4.2 VT

Voltage Transformer

4.2.1 VT: Global Parameters

VT . **V Cutoff Level**	[Device Para / Measurem Display / Voltage]	
0.005Vn	0.0Vn ... 0.100Vn	S.3
The Phase Voltage shown in the Display or within the PC Software will be displayed as zero, if the Phase Voltage falls below this Cutoff Level. This parameter has no impact on recorders. This parameter is related to the voltage that is connected to the device (phase-to-phase or phase-to-earth).		

VT . **VG meas Cutoff Level**	[Device Para / Measurem Display / Voltage]	
0.005Vn	0.0Vn ... 0.100Vn	S.3
The measured Residual Voltage shown in the Display or within the PC Software will be displayed as zero, if the measured Residual Voltage falls below this Cutoff Level. This parameter has no impact on recorders.		

VT . **VG calc Cutoff Level**	[Device Para / Measurem Display / Voltage]	
0.005Vn	0.0Vn ... 0.100Vn	S.3
The calculated Residual Voltage shown in the Display or within the PC Software will be displayed as zero, if the calculated Residual Voltage falls below this Cutoff Level. This parameter has no impact on recorders.		

VT . **V012 Comp Cutoff Level**	[Device Para / Measurem Display / Voltage]	
0.005Vn	0.0Vn ... 0.100Vn	S.3
The Symmetrical Component shown in the Display or within the PC Software will be displayed as zero, if the Symmetrical Component falls below this Cutoff Level. This parameter has no impact on recorders.		

VT . **VT pri**	[Field Para / VT]	
10000V	60V ... 500000V	S.3
Nominal voltage of the Voltage Transformers at the primary side. Note that always the phase-to-phase voltage must be entered here.		

VT . **VT sec**	[Field Para / VT]	
100V	60.00V ... 520.00V	S.3
Nominal voltage of the Voltage Transformers at the secondary side. Note that always the phase-to-phase voltage must be entered here.		

VT . **VT con**	[Field Para / VT]	
Phase to Ground	Phase to Phase, Phase to Ground ↳ VT con.	S.3
This parameter has to be set in order to ensure the correct assignment of the voltage measurement channels in the device.		

VT . **EVT pri**	[Field Para / VT]	
10000V	60V . . . 500000V	S.3
Primary nominal voltage of the e-n winding of the voltage transformers, which is only taken into account in the direct measurement of the residual voltage (GVT con=measured/broken delta).		

VT . **EVT sec**	[Field Para / VT]	
100V	35.00V . . . 520.00V	S.3
Secondary nominal voltage of the e-n winding of the voltage transformers, which is only taken into account in the direct measurement of the residual voltage.		

VT . **V Sync**	[Field Para / VT]	
L12	L1, L2, L3, L12, L23, L31 ↳ Voltages to be synchronized.	S.3
The fourth measuring input of the voltage measuring card measures the voltage that is to be synchronized.		

VT . **V Block f**	[Field Para / Frequency]	
0.5Vn	0.15Vn . . . 0.90Vn	S.3
Threshold for the release of the frequency stages		

VT . **delta phi - Mode**	[Field Para / Frequency]	
two phases	one phase, two phases, three phases ↳ delta phi - Mode.	S.3
The delta phi element (vector surge) trips, if the permissable voltage angle shift (delta phi) of the three measured voltages (phase-ground or phase-phase) in: one phase, two phases or within all phases is exceeded.		

VT . **Stab. window f**	[Field Para / Frequency]	
0	0 ... 10	S.3
Stabilizing window, for stabilizing the frequency values against momentary fluctuations. The setting value is in cycles at the rated frequency.		

VT . **Window df/dt**	[Field Para / Frequency]	
4	2 ... 10	S.3
Window for the determination of df/dt (ROCOF). The setting value is in cycles at the rated frequency.		

VT . **Stab. window df/dt**	[Field Para / Frequency]	
5	2 ... 10	S.3
Stabilizing window, for stabilizing the df/dt (ROCOF) values against momentary fluctuations. The setting value is in cycles at the rated frequency.		

4.2.2 VT: Signals (Output States)

VT . **Phase seq. wrong**	[Operation / Status Display / Supervision / Phase Sequence]
Signal that the device has detected a phase sequence (L1-L2-L3 / L1-L3-L2) that is different from the one that had been set at [Field settings / General Settings] »Phase Sequence«.	

4.2.3 VT: Values

VT . **f**	[Operation / Measured Values / Voltage]
Measured value: Frequency	

VT . **VL12**	[Operation / Measured Values / Voltage]
Measured value: Phase-to-phase voltage (fundamental)	

VT . **VL23**	[Operation / Measured Values / Voltage]
Measured value: Phase-to-phase voltage (fundamental)	

VT . **VL31**	[Operation / Measured Values / Voltage]
Measured value: Phase-to-phase voltage (fundamental)	

VT . **VL1**	[Operation / Measured Values / Voltage]
Measured value: Phase-to-neutral voltage (fundamental)	

VT . **VL2**	[Operation / Measured Values / Voltage]
⟍	*Measured value: Phase-to-neutral voltage (fundamental)*

VT . **VL3**	[Operation / Measured Values / Voltage]
⟍	*Measured value: Phase-to-neutral voltage (fundamental)*

VT . **VX meas**	[Operation / Measured Values / Voltage]
⟍	*Measured value (measured): VX measured (fundamental)*

VT . **VG calc**	[Operation / Measured Values / Voltage]
⟍	*Measured value (calculated): VG (fundamental)*

VT . **V0**	[Operation / Measured Values / Voltage]
⟍	*Measured value (calculated): Symmetrical components Zero voltage(fundamental)*

VT . **V1**	[Operation / Measured Values / Voltage]
⟍	*Measured value (calculated): Symmetrical components positive phase sequence voltage(fundamental)*

VT . **V2**	[Operation / Measured Values / Voltage]
⟍	*Measured value (calculated): Symmetrical components negative phase sequence voltage(fundamental)*

VT . **%(V2/V1)**	[Operation / Measured Values / Voltage]
⟍	*Measured value (calculated): V2/V1, phase sequence will be taken into account automatically.*

VT . **phi VL12**	[Operation / Measured Values / Voltage]
⟍	*Measured value (calculated): Angle of Phasor VL12* *Reference phasor is required to calculate the angle. This is the first measured voltage (or current) channel with sufficiently high amplitude.*

VT . **phi VL23**	[Operation / Measured Values / Voltage]
⟍	*Measured value (calculated): Angle of Phasor VL23* *Reference phasor is required to calculate the angle. This is the first measured voltage (or current) channel with sufficiently high amplitude.*

VT . **phi VL31**	[Operation / Measured Values / Voltage]
✎	*Measured value (calculated): Angle of Phasor VL31* *Reference phasor is required to calculate the angle. This is the first measured voltage (or current) channel with sufficiently high amplitude.*

VT . **phi VL1**	[Operation / Measured Values / Voltage]
✎	*Measured value (calculated): Angle of Phasor VL1* *Reference phasor is required to calculate the angle. This is the first measured voltage (or current) channel with sufficiently high amplitude.*

VT . **phi VL2**	[Operation / Measured Values / Voltage]
✎	*Measured value (calculated): Angle of Phasor VL2* *Reference phasor is required to calculate the angle. This is the first measured voltage (or current) channel with sufficiently high amplitude.*

VT . **phi VL3**	[Operation / Measured Values / Voltage]
✎	*Measured value (calculated): Angle of Phasor VL3* *Reference phasor is required to calculate the angle. This is the first measured voltage (or current) channel with sufficiently high amplitude.*

VT . **phi VX meas**	[Operation / Measured Values / Voltage]
✎	*Measured value: Angle of Phasor VX meas* *Reference phasor is required to calculate the angle. This is the first measured voltage (or current) channel with sufficiently high amplitude.*

VT . **phi VG calc**	[Operation / Measured Values / Voltage]
✎	*Measured value (calculated): Angle of Phasor VG calc* *Reference phasor is required to calculate the angle. This is the first measured voltage (or current) channel with sufficiently high amplitude.*

VT . **phi V0**	[Operation / Measured Values / Voltage]
✎	*Measured value (calculated): Angle Zero Sequence System* *Reference phasor is required to calculate the angle. This is the first measured voltage (or current) channel with sufficiently high amplitude.*

VT . **phi V1**	[Operation / Measured Values / Voltage]
⟍	*Measured value (calculated): Angle of Positive Sequence System* *Reference phasor is required to calculate the angle. This is the first measured voltage (or current) channel with sufficiently high amplitude.*

VT . **phi V2**	[Operation / Measured Values / Voltage]
⟍	*Measured Value (calculated): Angle of Negative Sequence System* *Reference phasor is required to calculate the angle. This is the first measured voltage (or current) channel with sufficiently high amplitude.*

VT . **df/dt**	[Operation / Measured Values / Voltage]
⟍	*Measured value (calculated): Rate-of-frequency-change.*

VT . **delta phi**	[Operation / Measured Values / Voltage]
⟍	*Measured value (calculated): Vector surge*

VT . **VL12 RMS**	[Operation / Measured Values / Voltage RMS]
⟍	*Measured value: Phase-to-phase voltage (RMS)*

VT . **VL23 RMS**	[Operation / Measured Values / Voltage RMS]
⟍	*Measured value: Phase-to-phase voltage (RMS)*

VT . **VL31 RMS**	[Operation / Measured Values / Voltage RMS]
⟍	*Measured value: Phase-to-phase voltage (RMS)*

VT . **VL1 RMS**	[Operation / Measured Values / Voltage RMS]
⟍	*Measured value: Phase-to-neutral voltage (RMS)*

VT . **VL2 RMS**	[Operation / Measured Values / Voltage RMS]
⟍	*Measured value: Phase-to-neutral voltage (RMS)*

VT . **VL3 RMS**	[Operation / Measured Values / Voltage RMS]
⟍	*Measured value: Phase-to-neutral voltage (RMS)*

VT . **VX meas RMS**	[Operation / Measured Values / Voltage RMS]
⟍	*Measured value (measured): VX measured (RMS)*

VT . **VG calc RMS**	[Operation / Measured Values / Voltage RMS]
⟍	*Measured value (calculated): VG (RMS)*

VT . **%VL12 THD**	[Operation / Measured Values / Voltage RMS]
⟍	*Measured value (calculated): V12 Total Harmonic Distortion / Ground wave*

VT . **%VL23 THD**	[Operation / Measured Values / Voltage RMS]
⟍	*Measured value (calculated): V23 Total Harmonic Distortion / Ground wave*

VT . **%VL31 THD**	[Operation / Measured Values / Voltage RMS]
⟍	*Measured value (calculated): V31 Total Harmonic Distortion / Ground wave*

VT . **%VL1 THD**	[Operation / Measured Values / Voltage RMS]
⟍	*Measured value (calculated): VL1 Total Harmonic Distortion / Ground wave*

VT . **%VL2 THD**	[Operation / Measured Values / Voltage RMS]
⟍	*Measured value (calculated): VL2 Total Harmonic Distortion / Ground wave*

VT . **%VL3 THD**	[Operation / Measured Values / Voltage RMS]
⟍	*Measured value (calculated): VL3 Total Harmonic Distortion / Ground wave*

VT . **VL12 THD**	[Operation / Measured Values / Voltage RMS]
⟍	*Measured value (calculated): V12 Total Harmonic Distortion*

VT . **VL23 THD**	[Operation / Measured Values / Voltage RMS]
⟍	*Measured value (calculated): V23 Total Harmonic Distortion*

VT . **VL31 THD**	[Operation / Measured Values / Voltage RMS]
⟍	*Measured value (calculated): V31 Total Harmonic Distortion*

VT . **VL1 THD**	[Operation / Measured Values / Voltage RMS]
⟍	*Measured value (calculated): VL1 Total Harmonic Distortion*

VT . **VL2 THD**	[Operation / Measured Values / Voltage RMS]
⟍	*Measured value (calculated): VL2 Total Harmonic Distortion*

VT . **VL3 THD**	[Operation / Measured Values / Voltage RMS]
⟍	*Measured value (calculated): VL3 Total Harmonic Distortion*

4.2.4 VT: Statistical Values

VT . **f max**	[Operation / Statistics / Max / Voltage]
☑	*Max. frequency value*

VT . **VL12 max RMS**	[Operation / Statistics / Max / Voltage]
☑	*VL12 maximum value (RMS)*

VT . **VL23 max RMS**	[Operation / Statistics / Max / Voltage]
☑	*VL23 maximum value (RMS)*

VT . **VL31 max RMS**	[Operation / Statistics / Max / Voltage]
☑	*VL31 maximum value (RMS)*

VT . **VL1 max RMS**	[Operation / Statistics / Max / Voltage]
☑	*VL1 maximum value (RMS)*

VT . **VL2 max RMS**	[Operation / Statistics / Max / Voltage]
☑	*VL2 maximum value (RMS)*

VT . **VL3 max RMS**	[Operation / Statistics / Max / Voltage]
☑	*VL3 maximum value (RMS)*

VT . **VX meas max RMS**	[Operation / Statistics / Max / Voltage]
☑	*Measured value: VX maximum value (RMS)*

VT . **VG calc max RMS**	[Operation / Statistics / Max / Voltage]
☑	*Measured value (calculated):VX maximum value (RMS)*

VT . **V1 max**	[Operation / Statistics / Max / Voltage]
☑	*Maximum value: Symmetrical components positive phase sequence voltage(fundamental)*

VT . **V2 max**	[Operation / Statistics / Max / Voltage]
☑	*Maximum value: Symmetrical components negative phase sequence voltage(fundamental)*

VT . **%(V2/V1) max**	[Operation / Statistics / Max / Voltage]
☑	*Measured value (calculated):V2/V1 maximum value, phase sequence will be taken into account automatically*

VT . **f min**	[Operation / Statistics / Min / Voltage]
☑	*Min. frequency value*

VT . **VL12 min RMS**	[Operation / Statistics / Min / Voltage]
☑	*VL12 minimum value (RMS)*

VT . **VL23 min RMS**	[Operation / Statistics / Min / Voltage]
☑	*VL23 minimum value (RMS)*

VT . **VL31 min RMS**	[Operation / Statistics / Min / Voltage]
☑	*VL31 minimum value (RMS)*

VT . **VL1 min RMS**	[Operation / Statistics / Min / Voltage]
☑	*VL1 minimum value (RMS)*

VT . **VL2 min RMS**	[Operation / Statistics / Min / Voltage]
☑	*VL2 minimum value (RMS)*

VT . **VL3 min RMS**	[Operation / Statistics / Min / Voltage]
☑	*VL3 minimum value (RMS)*

VT . **VX meas min RMS**	[Operation / Statistics / Min / Voltage]
☑	*Measured value: VX minimum value (RMS)*

VT . **VG calc min RMS**	[Operation / Statistics / Min / Voltage]
☑	*Measured value (calculated):VX minimum value (RMS)*

VT . **V1 min**	[Operation / Statistics / Min / Voltage]
☑	*Minimum value: Symmetrical components positive phase sequence voltage(fundamental)*

VT . **V2 min**	[Operation / Statistics / Min / Voltage]
☑	*Minimum value: Symmetrical components negative phase sequence voltage(fundamental)*

VT . **%(V2/V1) min**	[Operation / Statistics / Min / Voltage]
☑	*Measured value (calculated):V2/V1 minimum value , phase sequence will be taken into account automatically*

VT . **VL12 avg RMS**	[Operation / Statistics / Vavg]
☑	*VL12 average value (RMS)*

VT . **VL23 avg RMS**	[Operation / Statistics / Vavg]
☑	*VL23 average value (RMS)*

VT . **VL31 avg RMS**	[Operation / Statistics / Vavg]
☑	*VL31 average value (RMS)*

VT . **VL1 avg RMS**	[Operation / Statistics / Vavg]
☑	*VL1 average value (RMS)*

VT . **VL2 avg RMS**	[Operation / Statistics / Vavg]
☑	*VL2 average value (RMS)*

VT . **VL3 avg RMS**	[Operation / Statistics / Vavg]
☑	*VL3 average value (RMS)*

5 System

System

5.1 Sys: Global Parameters

Sys . **Scaling**	[Device Para / Measurem Display / General Settings]	
Per unit values	Per unit values, Primary values, Secondary values ↳ Scaling.	S.3
Display of the measured values as primary, secondary or per unit values		

Sys . **Ack via »C« key**	[Device Para / Acknowledge]	
Ack LEDs w/o passw.	Nothing, Ack LEDs w/o passw., Ack LEDs, Ack LEDs and relays, Ack Everything ↳ Ack via »C« key.	P.2
Select which acknowledgeable elements can be reset via pressing the »C« key.		

Sys . **Remote Reset**	[Device Para / Acknowledge]	
active	inactive, active ↳ Mode.	P.2
Enables or disables the option to acknowledge from external/remote via signals (assignments) and SCADA.		

Sys . **Ack LED**	[Device Para / Acknowledge]	
“-” *Only available if:* • Sys . Remote Reset = active	“-” . . . Sys . Internal test state ↳ 1..n, Assignment List.	S.3
All acknowledgeable LEDs will be acknowledged if the state of the assigned signal becomes true.		

Sys . **Ack BO**	[Device Para / Acknowledge]	
"-" *Only available if:* • Sys . Remote Reset = active	"-" . . . Sys . Internal test state ↳ 1..n, Assignment List.	S.3
All acknowledgeable binary output relays will be acknowledged if the state of the assigned signal becomes true.		

Sys . **Ack Scada**	[Device Para / Acknowledge]	
"-" *Only available if:* • Sys . Remote Reset = active	"-" . . . Sys . Internal test state ↳ 1..n, Assignment List.	S.3
Latched SCADA signals are acknowledged if the state of the assigned signal becomes true.		

Sys . **Setting Lock**	[Field Para / General Settings]	
"-"	"-" . . . Sys . Internal test state ↳ 1..n, Assignment List.	P.2
No parameters can be changed as long as this input is true. The parameter settings are locked.		

Sys . **PSet-Switch**	[Protection Para / PSet-Switch]	
PS1	PS1, PS2, PS3, PS4, PSS via Inp fct, PSS via Scada ↳ PSet-Switch.	P.2
Switching Parameter Set		

Sys . **PS1: activated by** **. . .** Sys . **PS4: activated by**	[Protection Para / PSet-Switch]	
“-”	“-” . . . Logics . LE80.Out inverted ↳ 1..n, PSS.	P.2
This Setting Group will be the active one if: The Parameter Setting Group Switch is set to "Switch via Input" and the other three input functions are inactive at the same time. In case that there is more than one input function active, no Parameter Setting Group Switch will be executed. In case all input functions are inactive, the device will keep working with the Setting Group that was activated lastly.		

5.2 Sys: Direct Controls

Sys . **Ack BO LED Scd TCmd**	[Operation / Acknowledge]	
inactive	inactive, active ↳ Mode.	P.1
Reset the binary output relays, LEDs, SCADA and the Trip Command.		

Sys . **Ack LED**	[Operation / Acknowledge]	
inactive	inactive, active ↳ Mode.	P.1
All acknowledgeable LEDs will be acknowledged.		

Sys . **Ack BO**	[Operation / Acknowledge]	
inactive	inactive, active ↳ Mode.	P.1
All acknowledgeable binary output relays will be acknowledged.		

Sys . **Ack Scada**	[Operation / Acknowledge]	
inactive	inactive, active ↳ Mode.	P.1
Latched SCADA signals are acknowledged.		

Sys . **Setting Lock Bypass**	[Field Para / General Settings]	
inactive	inactive, active ↳ Mode.	P.1
◉	*Short-period unlock of the Setting Lock*	

Sys . **Reboot**	[Service / General]	
no	no, yes ↳ yes/no.	S.3
◉	*Rebooting the device.*	

5.3 Sys: Input States

Sys . **Ack LED-I**	[Operation / Status Display / Sys]
⇩	*Module input state: LEDs acknowledgement by digital input*

Sys . **Ack BO-I**	[Operation / Status Display / Sys]
⇩	*Module input state: Acknowledgement of the binary Output Relays*

Sys . **Ack Scada-I**	[Operation / Status Display / Sys]
⇩	*Module input state: Acknowledge latched SCADA signals.*

Sys . **PS1-I** **. . .** Sys . **PS4-I**	[Operation / Status Display / Sys]
⇩	*State of the module input respectively of the signal, that should activate this Parameter Setting Group.*

Sys . **Setting Lock-I**	[Operation / Status Display / Sys]
⇩	*State of the module input: No parameters can be changed as long as this input is true. The parameter settings are locked.*

5.4 Sys: Signals (Output States)

Sys . **Reboot**	[Operation / Status Display / Sys]
⇧	*Signal: Rebooting the device.* *Device Start-up Codes: 1=Normal Start-up; 2=Reboot by the Operator; 3=Reboot by means of Super Reset; 4=outdated; 5=outdated; 6=Unknown Error Source; 7=Forced Reboot (initiated by the main processor); 8=Exceeded Time Limit of the Protection Cycle; 9= Forced Reboot (initiated by the digital signal processor); 10=Exceeded Time Limit of the Measured Value Processing; 11=Sags of the Supply Voltage; 12=Illegal Memory Access.*

Sys . **Act Set**	[Operation / Status Display / Sys] [Protection Para / PSet-Switch]
⇧	*Signal: Active Parameter Set*

Sys . **PS 1**	[Operation / Status Display / Sys]
⇧	*Signal: The currently active Parameter Set is PS 1*

Sys . **PS 2**	[Operation / Status Display / Sys]
⇧	*Signal: The currently active Parameter Set is PS 2*

Sys . **PS 3**	[Operation / Status Display / Sys]
⇧	*Signal: The currently active Parameter Set is PS 3*

Sys . **PS 4**	[Operation / Status Display / Sys]
⇧	*Signal: The currently active Parameter Set is PS 4*

Sys . **PSS manual**	[Operation / Status Display / Sys]
⇧	*Signal: Manual Switch over of a Parameter Set*

Sys . **PSS via Scada**	[Operation / Status Display / Sys]
⇧	*Signal: Parameter Set Switch via Scada. Write into this output byte the integer of the parameter set that should become active (e.g. 4 => Switch onto parameter set 4).*

Sys . **PSS via Inp fct**	[Operation / Status Display / Sys]
⇧	*Signal: Parameter Set Switch via input function*

Sys . **min 1 param changed**	[Operation / Status Display / Sys]
⇧	*Signal: At least one parameter has been changed*

Sys . **Setting Lock Bypass**	[Operation / Status Display / Sys]
⇧	*Signal: Short-period unlock of the Setting Lock*

Sys . **Ack LED**	[Operation / Status Display / Sys]
⇧	*Signal: LEDs acknowledgement*

Sys . **Ack BO**	[Operation / Status Display / Sys]
⇧	*Signal: Acknowledgement of the Binary Outputs*

Sys . **Ack Scada**	[Operation / Status Display / Sys]
⇧	*Signal: Acknowledge latched SCADA signals*

Sys . **Ack TripCmd**	[Operation / Status Display / Sys]
⇧	*Signal: Reset Trip Command*

Sys . **Ack LED-HMI**	[Operation / Status Display / Sys]
⇧	*Signal: LEDs acknowledgement :HMI*

Sys . **Ack BO-HMI**	[Operation / Status Display / Sys]
⇧	*Signal: Acknowledgement of the Binary Outputs :HMI*

Sys . **Ack Scada-HMI**	[Operation / Status Display / Sys]
⇧	*Signal: Acknowledge latched SCADA signals :HMI*

Sys . **Ack TripCmd-HMI**	[Operation / Status Display / Sys]
⇧	*Signal: Reset Trip Command :HMI*

Sys . **Ack LED-Sca**	[Operation / Status Display / Sys]
⇧	*Signal: LEDs acknowledgement :SCADA*

Sys . **Ack BO-Sca**	[Operation / Status Display / Sys]
⇧	*Signal: Acknowledgement of the Binary Outputs :SCADA*

Sys . **Ack Counter-Sca**	[Operation / Status Display / Sys]
⇧	*Signal: Reset of all Counters :SCADA*

Sys . **Ack Scada-Sca**	[Operation / Status Display / Sys]
⇧	*Signal: Acknowledge latched SCADA signals :SCADA*

Sys . **Ack TripCmd-Sca**	[Operation / Status Display / Sys]
⇧	*Signal: Reset Trip Command :SCADA*

Sys . **Res OperationsCr**	[Operation / Status Display / Sys]
⇧	*Signal:: Res OperationsCr*

Sys . **Res AlarmCr**	[Operation / Status Display / Sys]
⇧	*Signal:: Res AlarmCr*

Sys . **Res TripCmdCr**	[Operation / Status Display / Sys]
⇧	*Signal:: Res TripCmdCr*

Sys . **Res TotalCr**	[Operation / Status Display / Sys]
⇧	*Signal:: Res TotalCr*

5.5 Sys: Values

Sys . **Operating hours Cr**	[Operation / Count and RevData / Sys]
⇘	*Operating hours counter of the protective device*

Sys . **DM version**	[Device Para / Version]	
3.6.b	3.6.b ↳ .	
⇘	*Version of the device model*	

Sys . **SW version**	[Device Para / Version]
⇘	*Version of the device firmware*

Sys . **Build**	[Device Para / Version]
✎	*Build Number*

Sys . **CAT No**	[Device Para / Version]
✎	*»CAT No.«, Order Code as printed on the nameplate of the device.*

Sys . **REV.**	[Device Para / Version]
✎	*Revision (as printed on the nameplate of the device).*

Sys . **S/N**	[Device Para / Version]
✎	*The serial number of the device.*

Sys . **Bootloader Build**	[Device Para / Version]
✎	*Build number of the bootloader*

6 Measured Values

- HMI: ⮡ “HMI: Values”
- VT: ⮡ “VT: Values”
- System: ⮡ “Sys: Values”
- Modbus: ⮡ “Modbus: Values”
- IEC 61850: ⮡ “IEC 61850: Values”
- IEC104: ⮡ “IEC104: Values”
- Profibus: ⮡ “Profibus: Values”
- SNTP: ⮡ “SNTP: Values”
- Sync: ⮡ “Sync: Values”
- Control: ⮡ “Ctrl: Values”
- Disturb rec: ⮡ “Disturb rec: Values”
- Sgen: ⮡ “Sgen: Values”

7 Statistics

- VT: ↳ “VT: Statistical Values”

7.1 Statistics: Global Parameters

Statistics . **ResFc Max**	[Device Para / Statistics / Min / Max]	
“-”	“-” . . . Sys . Internal test state ↳ 1..n, Assignment List.	S.3
Resetting of all Maximum values		

Statistics . **ResFc Min**	[Device Para / Statistics / Min / Max]	
“-”	“-” . . . Sys . Internal test state ↳ 1..n, Assignment List.	S.3
Resetting of all Minimum values		

Statistics . **Start Vavg via:**	[Device Para / Statistics / Vavg]	
Duration	Duration, StartFct ↳ Duration.	S.3
Start sliding average supervision by:		

Statistics . **Start Vavg Fc**	[Device Para / Statistics / Vavg]	
“-” *Only available if:* • Statistics . Start Vavg via: = StartFct	“-” . . . Sys . Internal test state ↳ 1..n, Assignment List.	S.3
Start of the calculation, if the assigned signal becomes true.		

Statistics . **ResFc Vavg**	[Device Para / Statistics / Vavg]	
“-”	“-” . . . Sys . Internal test state ↳ 1..n, Assignment List.	S.3
Resetting of the sliding average calculation.		

Statistics . **Duration Vavg**	[Device Para / Statistics / Vavg]	
10 min *Only available if:* • Statistics . Start Vavg via: = Duration	2 s . . . 30 d ↳ Duration.	S.3
Recording time		

Statistics . **Window Vavg**	[Device Para / Statistics / Vavg]	
sliding	sliding, fixed ↳ Window configuration.	S.3
Window configuration		

7.2 Statistics: Direct Controls

Statistics . **ResFc all**	[Operation / Reset]	
inactive	inactive, active ↳ Mode.	P.1
Resetting of all Statistic values (Current Demand, Power Demand, Min, Max)		

Statistics . **ResFc Max**	[Operation / Reset]	
inactive	inactive, active ↳ Mode.	P.1
Resetting of all Maximum values		

Statistics . **ResFc Min**	[Operation / Reset]	
inactive	inactive, active ↳ Mode.	P.1
Resetting of all Minimum values		

Statistics . **ResFc Vavg**	[Operation / Reset]	
inactive	inactive, active Mode.	P.1
	Resetting of the sliding average calculation.	

7.3 Statistics: Input States

Statistics . **StartFc Vavg-I**	[Operation / Status Display / Statistics]
	State of the module input: Start of Statistics Average Voltage

7.4 Statistics: Signals (Output States)

Statistics . **ResFc all**	[Operation / Status Display / Statistics]
	Signal: Resetting of all Statistic values (Current Demand, Power Demand, Min, Max)

Statistics . **ResFc Vavg**	[Operation / Status Display / Statistics]
	Signal: Resetting of the sliding average calculation.

Statistics . **ResFc Max**	[Operation / Status Display / Statistics]
	Signal: Resetting of all Maximum values

Statistics . **ResFc Min**	[Operation / Status Display / Statistics]
	Signal: Resetting of all Minimum values

7.5 Statistics: Counters

Statistics . **Res Cr Max values**	[Operation / Statistics / Max / Voltage]
	Number of resets since last booting. The timestamp shows date and time of the last reset.

Statistics . **Res Cr Min values**	[Operation / Statistics / Min / Voltage]
	Number of resets since last booting. The timestamp shows date and time of the last reset.

Statistics . **Res Cr Vavg**	[Operation / Statistics / Vavg]
#	*Number of resets since last booting. The timestamp shows date and time of the last reset.*

8 Communication

Scada

8.1 Scada: Device Planning Parameters

Scada . **Protocol**	[Device planning]	
“-”	“-” . . . Profibus Used Protocol.	S.3
Select the SCADA protocol to be used.		

8.2 Scada: Signals (Output States)

Scada . **SCADA connected**	[Operation / Status Display / Scada]
At least one SCADA System is connected to the device.	

Scada . **SCADA not connected**	[Operation / Status Display / Scada]
No SCADA System is connected to the device	

8.3 TcpIp

TcpIp

TCP/IP config	[Device Para / TCP/IP / TCP/IP config]
	This item represents a special dialog. (See the Technical Manual for details.) *configuration of the TCP/IP protocol*

8.3.1 TcpIp: Global Parameters

TcpIp . **Keep Alive Time**	[Device Para / TCP/IP / Advanced Settings]	
720s	1s ... 7200s	S.3
	Keep Alive Time is the duration between two keep alive transmissions in idle condition	

TcpIp . **Keep Alive Interval**	[Device Para / TCP/IP / Advanced Settings]	
15s	1s ... 60s	S.3
	Keep Alive Interval is the duration between two successive keep alive retransmissions, if the acknowledgement to the previous keepalive transmission was not received.	

TcpIp . **Keep Alive Retry**	[Device Para / TCP/IP / Advanced Settings]	
3	3 ... 3	S.3
	Keep alive retry is the number of retransmissions to be carried out before declaring that the remote end is not available.	

8.4 DNP3

Distributed Network Protocol

8.4.1 DNP3: Global Parameters

DNP3 . **Function**	[Device Para / DNP3 / Communication]	
inactive	inactive, active ↳ Mode.	S.3
Permanent activation or deactivation of module/stage.		

DNP3 . **IP Port Number**	[Device Para / DNP3 / Communication]	
20000	0 . . . 65535	S.3
IP Port Number. *In general it is recommended to keep the default value. If this is not possible then select a number out of the private range 49152-52151 or 52164-65535 that is not yet in use within your network.*		

DNP3 . **Baud rate**	[Device Para / DNP3 / Communication]	
19200	1200 . . . 115200 ↳ Baud rate.	S.3
Baud rate for communication		

DNP3 . **Frame Layout**	[Device Para / DNP3 / Communication]	
8E1	8E1, 8O1, 8N1, 8N2 ↳ Byte Frame.	S.3
Frame Layout		

DNP3 . **Optical rest position**	[Device Para / DNP3 / Communication]	
Light on *Avail. depends on HW*	Light off, Light on ↳ Optical rest position.	S.3
Optical rest position		

DNP3 . **SelfAddress**	[Device Para / DNP3 / Communication]	
inactive	inactive, active ↳ Mode.	S.3
Support of self (automatic) addresses		

DNP3 . **DataLink confirm**	[Device Para / DNP3 / Communication]	
Never	Never, Always, On_Large ↳ Communication Start Variants.	S.3
Enables or disables the data layer confirmation (ack).		

DNP3 . **t-DataLink confirm**	[Device Para / DNP3 / Communication]	
1s	0.1s ... 10.0s	S.3
Data layer confirmation timeout		

DNP3 . **DataLink num retries**	[Device Para / DNP3 / Communication]	
3	0 ... 255	S.3
Number of repetition of data link packet sending after failing		

DNP3 . **Direction Bit**	[Device Para / DNP3 / Communication]	
inactive	inactive, active ↳ Mode.	S.3
Enables Direction Bit functionality. The Direction Bit is 0 for SlaveStation and 1 for MasterStation		

DNP3 . **Max Frame Size**	[Device Para / DNP3 / Communication]	
255	64 ... 255	S.3
This value is used to limit the net Frame Size		

DNP3 . **Test Link Period**	[Device Para / DNP3 / Communication]	
0s	0.0s ... 120.0s	S.3
This value specifies the time period when to send a Test Link-Frame		

DNP3 . **AppLink confirm**	[Device Para / DNP3 / Communication]	
Always	Never, Always, Event ↳ _AL_ResponseType_k.	S.3
Determines if the device will request that the Application Layer response be confirmed or not		

DNP3 . **t-AppLink confirm**	[Device Para / DNP3 / Communication]	
5s	0.1s ... 10.0s	S.3
Application layer response timeout		

DNP3 . **AppLink num retries**	[Device Para / DNP3 / Communication]	
0	0 ... 255	S.3
The number of times the device will retransmit an Application Layer fragment		

DNP3 . **Unsol Reporting**	[Device Para / DNP3 / Communication]	
inactive	inactive, active ↳ Mode.	S.3
Enables unsolicited reporting. This is available only for DNP3 TCP connections, and for DNP3 RTU in case of a peer-to-peer connection.		

DNP3 . **Unsol Reporting Timeout**	[Device Para / DNP3 / Communication]	
10s	1.0s ... 60.0s	S.3
Set the amount of time that the outstation will wait for an Application Layer confirmation back from the master indicating that the master received the unsolicited response message.		

DNP3 . **Unsol Reporting Retry**	[Device Para / DNP3 / Communication]	
2	0 ... 255	S.3
Set the number of retries that an outstation transmits in each unsolicited response series if it does not receive confirmation back from the master.		

DNP3 . **TestSeqNo**	[Device Para / DNP3 / Communication]	
inactive	inactive, active ↳ Mode.	S.3
Test if sequence number of request is incremented. If it is not correctly incremented the request will be ignored. It is recommended to have it inactive but some older DNP implementations need it activated.		

DNP3 . **TestSBO**	[Device Para / DNP3 / Communication]	
active	inactive, active ↳ Mode.	S.3
It enables a stricter comparing of SBO and operate command. For older DNP versions it is recommanded to deactivated it.		

DNP3 . **Timeout SBO**	[Device Para / DNP3 / Communication]	
30s	1.0s . . . 60.0s	S.3
DNP Outputs can be controlled in a two stage procedure (SBO: Select Before Operate). These outputs are to be selected first by a Select command. After this the bit is reserved for this Operate request. This setting defines the timer for this reservation: After the timer has elapsed the bit is released.		

DNP3 . **ColdRestart**	[Device Para / DNP3 / Communication]	
inactive	inactive, active ↳ Mode.	S.3
Enables support for Cold Restart function.		

DNP3 . **Deadb integr time**	[Device Para / DNP3 / Communication]	
1	0 . . . 300	S.3
Deadband integration time.		

DNP3 . **BinaryInput 0** **. . .** DNP3 . **BinaryInput 63**	[Device Para / DNP3 / Point map / Binary Inputs]	
“-”	“-” . . . Sys . Internal test state ↳ 1..n, Assignment List.	S.3
Virtual Digital Input (DNP). This corresponds to a virtual binary output of the protective device.		

DNP3 . **DoubleBitInput 0** **...** DNP3 . **DoubleBitInput 5**	[Device Para / DNP3 / Point map / Double Bit Inputs]	
“-”	“-”, SG[1] . Pos ↳ 1..n, Assignment List.	S.3
Double Bit Digital Input (DNP). This corresponds to a double bit binary output of the protective device.		

DNP3 . **BinaryCounter 0** **...** DNP3 . **BinaryCounter 7**	[Device Para / DNP3 / Point map / BinaryCounter]	
“-”	“-” ... Sys . Operating hours Cr ↳ 1..n, Assignment List.	S.3
Counter can be used to report counter values to the DNP master.		

DNP3 . **Analog value 0** **...** DNP3 . **Analog value 31**	[Device Para / DNP3 / Point map / Analog Input]	
“-”	“-” ... VT . VL31 THD ↳ 1..n, TrendRecList.	S.3
Analog value can be used to report values to the master (DNP)		

DNP3 . **Scale Factor 0** **...** DNP3 . **Scale Factor 31**	[Device Para / DNP3 / Point map / Analog Input]	
1	0.001 ... 1000000 ↳ Scale Factor.	S.3
The scale factor is used to convert the measured value in an integer format		

DNP3 . **Dead Band 0** **...** DNP3 . **Dead Band 31**	[Device Para / DNP3 / Point map / Analog Input]	
1%	0.01% ... 100.00%	S.3
If a change of measured value is greater than the deadband value it will be reported to the master.		

8.4.2 DNP3: Direct Controls

DNP3 . **Res all Diag Cr**	[Operation / Count and RevData / DNP3] [Operation / Reset]	
inactive	inactive, active Mode.	S.3
Reset all diagnosis counters		

DNP3 . **Slave Id**	[Device Para / DNP3 / Communication]	
1	0 ... 65519	S.3
SlaveId defines the DNP3 address of this device (Outstation)		

DNP3 . **Master Id**	[Device Para / DNP3 / Communication]	
65500	0 ... 65519	S.3
MasterId defines the DNP3 address of master (SCADA)		

8.4.3 DNP3: Input States

DNP3 . **BinaryInput0-I** **...** DNP3 . **BinaryInput63-I**	[Operation / Status Display / DNP3 / Binary Inputs]
Virtual Digital Input (DNP). This corresponds to a virtual binary output of the protective device.	

DNP3 . **DoubleBitInput0-I** **...** DNP3 . **DoubleBitInput5-I**	[Operation / Status Display / DNP3 / Double Bit Inputs]
⇩	*Double Bit Digital Input (DNP). This corresponds to a double bit binary output of the protective device.*

8.4.4 DNP3: Signals (Output States)

DNP3 . **busy**	[Operation / Status Display / DNP3 / State]
⇧	*This message is set if the protocol is started. It will be reset if the protocol is shut down.*

DNP3 . **ready**	[Operation / Status Display / DNP3 / State]
⇧	*The message will be set if the protocol is successfully started and ready for data exchange.*

DNP3 . **active**	[Operation / Status Display / DNP3 / State]
⇧	*The communication with the Master (SCADA) is active.* *Note that for TCP/UDP, this state is permanently “Low” unless »DataLink confirm« is set to “Always”.*

8.4.5 DNP3: Counters

DNP3 . **NReceived**	[Operation / Count and RevData / DNP3]
#	*Diagnostic counter: Number of received characters*

DNP3 . **NSent**	[Operation / Count and RevData / DNP3]
#	*Diagnostic counter: Number of sent characters*

DNP3 . **NBadFramings**	[Operation / Count and RevData / DNP3]
#	*Diagnostic counter: Number of bad framings. A large number indicates a disturbed serial connection.*

DNP3 . **NBadParities**	[Operation / Count and RevData / DNP3]
#	*Diagnostic counter: Number of parity errrors. A large number indicates a disturbed serial connection.*

DNP3 . **NBreakSignals**	[Operation / Count and RevData / DNP3]
#	*Diagnostic counter: Number of break signals. A large number indicates a disturbed serial connection.*

DNP3 . **NBadChecksum**	[Operation / Count and RevData / DNP3]
#	*Diagnostic counter: Number of frames received with bad checksum.*

8.5 Modbus

Modbus

8.5.1 Modbus: Global Parameters

Modbus . **t-call**	[Device Para / Modbus / Communication / General Settings]	
10s	1s ... 3600s	S.3
If there is no request telegram sent from Scada to the device after expiry of this time - the device concludes a communication failure within the Scada system.		

Modbus . **Scada CmdBlo**	[Device Para / Modbus / Communication / General Settings]	
inactive	inactive, active ↳ Mode.	S.3
Activating (allowing)/ Deactivating (disallowing) the blocking of the Scada Commands		

Modbus . **Disable Latching**	[Device Para / Modbus / Communication / General Settings]	
inactive	inactive, active ↳ Mode.	S.3
Disable Latching: If this parameter is active (true), none of the Modbus states will be latched. That means that trip signals wont be latched by Modbus.		

Modbus . **AllowGap**	[Device Para / Modbus / Communication / General Settings]	
inactive	inactive, active ↳ Mode.	S.3
If this parameter is active (True), the user can request a set of modbus register without getting an exception, because of invalid address in the requested array. The invalid addresses have a special value 0xFAFA, but the user is responsible for ignoring invalid addresses. Attention: This special value can be valid, if address is valid.		

Modbus . **Optical rest position**	[Device Para / Modbus / Communication / General Settings]	
Light on *Avail. depends on HW*	Light off, Light on ↳ Optical rest position.	S.3
Optical rest position		

Modbus . **TCP Port Config**	[Device Para / Modbus / Communication / TCP]	
Default	Default, Private ↳ Port selection.	S.3
TCP Port Configuration. This parameter needs to be set to “Private” only if another TCP Port than the default one shall be used.		

Modbus . **Port**	[Device Para / Modbus / Communication / TCP]	
502	If: Modbus . TCP Port Config = Default • 502 ... 502 If: Modbus . TCP Port Config = Private • 49152 ... 65535	S.3
IP Port Number. *In general it is recommended to keep the default value. if this is not possible then select a number out of the private range 49152-52151 or 52164-65535 that is not yet in use within your network.*		

Modbus . **t-timeout**	[Device Para / Modbus / Communication / RTU]	
1s	0.01s ... 10.00s	S.3
Within this time the answer has to be received by the SCADA system, otherwise the request will be disregarded. In that case the Scada system detects a communication failure and the Scada System has to send a new request.		

Modbus . **Baud rate**	[Device Para / Modbus / Communication / RTU]	
19200	1200, 2400, 4800, 9600, 19200, 38400 ↳ Baud rate.	S.3
Baud rate		

Modbus . **Physical Settings**	[Device Para / Modbus / Communication / RTU]	
8E1	8E1, 8O1, 8N1, 8N2 ↳ Byte Frame.	S.3
Digit 1: Number of bits. Digit 2: E=even parity, O=odd parity, N=no parity. Digit 3: Number of stop bits. More information on the parity: It is possible that the last data bit is followed by a parity bit which is used for recognition of communication errors. The parity bit ensures that with even parity ("EVEN") always an even number of bits with valence "1" or with odd parity ("ODD") an odd number of "1" valence bits are transmitted. But it is also possible to transmit no parity bits (here the setting is "Parity = None"). More information on the stop-bits: The end of a data byte is terminated by the stop-bits.		

Modbus . **Config Bin Inp1** **...** Modbus . **Config Bin Inp32**	[Device Para / Modbus / Configb Registers / States]	
“-”	“-” ... Sys . Internal test state ↳ 1..n, Assignment List.	S.3
Virtual Digital Input. This corresponds to a virtual binary output of the protective device.		

Modbus . **Latched Config Bin Inp1** **...** Modbus . **Latched Config Bin Inp32**	[Device Para / Modbus / Configb Registers / States]	
inactive	inactive, active ↳ Mode.	S.3
Latched Configurable Binary Input		

Modbus . **Mapped Meas 1** **...** Modbus . **Mapped Meas 16**	[Device Para / Modbus / Configb Registers / Measured Values]	
“-”	“-” ... VT . VL31 THD ↳ 1..n, TrendRecList.	S.3
Mapped Measured Values. They can be used to provide measured values to the Modbus Master.		

Modbus . **Type of SCADA mapping**	[Device Para / Modbus / Config. Data Obj.]	
Standard	Standard, User-defined ↳ Type of SCADA mapping.	S.3
*This setting decides whether the communication protocol shall use the default mapping of data objects, or some user-defined mapping that has been loaded from a *.HptSMap file.*		

8.5.2 Modbus: Direct Controls

Modbus . **Res Diagn Cr**	[Operation / Reset]	
inactive	inactive, active ↳ Mode.	P.1
◉	*All Modbus Diagnosis Counters will be reset.*	

Modbus . **Unit ID**	[Device Para / Modbus / Communication / TCP]	
255	1 ... 255	P.1
◉	*The Unit Identifier is used for routing. This parameter is to be set, if a Modbus RTU and a Modbus TCP network should be coupled.*	

Modbus . **Slave ID**	[Device Para / Modbus / Communication / RTU]	
1	1 ... 247	P.1
◉	*Device address (Slave ID) within the bus system. Each device address has to be unique within a bus system.*	

8.5.3 Modbus: Input States

Modbus . **Config Bin Inp1-I** **...** Modbus . **Config Bin Inp32-I**	[Operation / Status Display / Modbus / Configb Registers]
⇩	*State of the module input: Config Bin Inp*

8.5.4 Modbus: Signals (Output States)

Modbus . **Transmission RTU**	[Operation / Status Display / Modbus / State]
⇧	*Signal: SCADA active*

Modbus . **Transmission TCP**	[Operation / Status Display / Modbus / State]
⇧	*Signal: SCADA active*

Modbus . **Device Type**	[Operation / Status Display / Modbus / State]
⇧	*Device Type: Device type code for relationship between device name and its Modbus code.* *Woodward:* *MRI4 - 1000* *MRU4 - 1001* *MRA4 - 1002* *MCA4 - 1003* *MRDT4 - 1005* *MCDTV4 - 1006* *MCDGV4 - 1007* *MRM4 - 1009* *MRMV4 - 1010* *MCDLV4 - 1011*

Modbus . **Comm Version**	[Operation / Status Display / Modbus / State]
⇧	*Modbus Communication version. This version number changes if something becomes incompatible between different Modbus releases.*

Modbus . **Scada Cmd 1** **...** Modbus . **Scada Cmd 16**	[Operation / Status Display / Modbus / Commands]
⇧	*Scada Command*

8.5.5 Modbus: Values

Modbus . **Mapped Meas 1** **...** Modbus . **Mapped Meas 16**	[Operation / Count and RevData / Modbus / Measured Values]
⇘	*Mapped Measured Values. They can be used to provide measured values to the Modbus Master.*

Modbus . **Config info**	[Device Para / Modbus / Config. Data Obj.]
⇘	*Configuration comment (entered by the user during SCADA configuration)*

Modbus . **Config version**	[Device Para / Modbus / Config. Data Obj.]
⟍	*Version of the user-defined SCADA configuration*

Modbus . **Config status**	[Device Para / Modbus / Config. Data Obj.]	
Changing	Changing, OK, Config. not avail., Error ⮡ Config status.	
⟍	*Status of the user-defined SCADA configuration.* *Possible values:* *- New SCADA configuration is being loaded, but not active yet.* *- The SCADA configuration is active.* *- The user-defined SCADA configuration is not available (e.g. has not been loaded into the device).* *- Unexpected error. Please contact our service-team.*	

8.5.6 Modbus: Counters

Modbus . **NoOfRequestsTotal**	[Operation / Count and RevData / Modbus / TCP] [Operation / Count and RevData / Modbus / RTU]
#	*Total number of requests. Includes requests for other slaves.*

Modbus . **NoOfRequestsForMe**	[Operation / Count and RevData / Modbus / TCP] [Operation / Count and RevData / Modbus / RTU]
#	*Total Number of requests for this slave.*

Modbus . **NoOfResponse**	[Operation / Count and RevData / Modbus / TCP] [Operation / Count and RevData / Modbus / RTU]
#	*Total number of requests having been responded.*

Modbus . **NoOfQueryInvalid**	[Operation / Count and RevData / Modbus / TCP]
#	*Total number of Request errors. Request could not be interpreted*

Modbus . **NoOfInternalError**	[Operation / Count and RevData / Modbus / TCP]
#	*Total Number of Internal errors while interpreting the request.*

Modbus . **NoOfFrameErrors**	[Operation / Count and RevData / Modbus / RTU]
#	*Total Number of Frame Errors. Physically corrupted Frame.*

Modbus . **NoOfParityErrors**	[Operation / Count and RevData / Modbus / RTU]
#	*Total number of parity errors. Physically corrupted Frame.*

Modbus . **NoOfResponsTimeOverruns**	[Operation / Count and RevData / Modbus / RTU]
#	*Total number of requests with exceeded response time. Physically corrupted Frame.*

Modbus . **NoOfOverrunErros**	[Operation / Count and RevData / Modbus / RTU]
#	*Total Number of Overrun Failures. Physically corrupted Frame.*

Modbus . **NoOfBreaks**	[Operation / Count and RevData / Modbus / RTU]
#	*Number of detected communication aborts*

8.6 IEC 61850

IEC 61850 communication

8.6.1 IEC 61850: Global Parameters

IEC 61850 . **Function**	[Device Para / IEC 61850 / Communication]	
inactive	inactive, active ↳ 1..n, OnOffList.	S.3
Permanent activation or deactivation of module/stage.		

IEC 61850 . **Deadb integr time**	[Device Para / IEC 61850 / Communication]	
0	0 ... 300	S.3
Deadband integration time.		

8.6.2 IEC 61850: Direct Controls

IEC 61850 . **ResetStatistic**	[Operation / Reset]	
inactive	inactive, active ↳ Mode.	P.1
Reset of all IEC61850 diagnostic counters		

8.6.3 IEC 61850: Signals (Output States)

IEC 61850 . **MMS Client connected**	[Operation / Status Display / IEC 61850 / State]
At least one MMS client is connected to the device	

IEC 61850 . **All Goose Subscriber active**	[Operation / Status Display / IEC 61850 / State]
All Goose subscriber in the device are working	

IEC 61850 . **SPCSO1** **...** IEC 61850 . **SPCSO32**	[Operation / Status Display / IEC 61850 / ControlInputs]
Status bit that can be set by clients like e.g. SCADA (Single Point Controllable Status Output).	

IEC 61850 . **GOSINGGIO1.Ind1.stVal** **...** IEC 61850 . **GOSINGGIO2.Ind32.stVal**	[Operation / Status Display / IEC 61850 / Virtual Inputs 1] [Operation / Status Display / IEC 61850 / Virtual Inputs 2]
⇪	*Signal: Virtual Input (IEC61850 GGIO Ind): State*

IEC 61850 . **GOSINGGIO1.Ind1.q** **...** IEC 61850 . **GOSINGGIO2.Ind32.q**	[Operation / Status Display / IEC 61850 / Virtual Inputs 1] [Operation / Status Display / IEC 61850 / Virtual Inputs 2]
⇪	*Signal: Virtual Input (IEC61850 GGIO Ind): Self-Supervision of the GGIO Input*

8.6.4 IEC 61850: Values

IEC 61850 . **GoosePublisherState**	[Operation / Status Display / IEC 61850 / State]	
Off	Off, On, Error ↳ State.	
⟍	*State of the GOOSE Publisher (on or off)*	

IEC 61850 . **GooseSubscriberState**	[Operation / Status Display / IEC 61850 / State]	
Off	Off, On, Error ↳ State.	
⟍	*State of the GOOSE Subscriber (on or off)*	

IEC 61850 . **MmsServerState**	[Operation / Status Display / IEC 61850 / State]	
Off	Off, On, Error ↳ State.	
⟍	*State of MMS Server (on or off)*	

8.6.5 IEC 61850: Counters

IEC 61850 . **NoOfGooseRxAll**	[Operation / Count and RevData / IEC 61850]
#	*Total number of received GOOSE messages including messages for other devices (subscribed and not subscribed messages).*

IEC 61850 . **NoOfGooseRxSubscribed**	[Operation / Count and RevData / IEC 61850]
#	*Total Number of subscribed GOOSE messages including messages with incorrect content.*

IEC 61850 . **NoOfGooseRxCorrect**	[Operation / Count and RevData / IEC 61850]
#	*Total Number of subscribed and correctly received GOOSE messages.*

IEC 61850 . **NoOfGooseRxNew**	[Operation / Count and RevData / IEC 61850]
#	*Number of subscribed and correctly received GOOSE messages with new content.*

IEC 61850 . **NoOfGooseTxAll**	[Operation / Count and RevData / IEC 61850]
#	*Total Number of GOOSE messages that have been published by this device.*

IEC 61850 . **NoOfGooseTxNew**	[Operation / Count and RevData / IEC 61850]
#	*Total Number of new GOOSE messages (modified content) that have been published by this device.*

IEC 61850 . **NoOfServerRequestsAll**	[Operation / Count and RevData / IEC 61850]
#	*Total number of MMS Server requests including incorrect requests.*

IEC 61850 . **NoOfDataReadAll**	[Operation / Count and RevData / IEC 61850]
#	*Total Number of values read from this device including incorrect requests.*

IEC 61850 . **NoOfDataReadCorrect**	[Operation / Count and RevData / IEC 61850]
#	*Total Number of correctly read values from this device.*

IEC 61850 . **NoOfDataWrittenAll**	[Operation / Count and RevData / IEC 61850]
#	*Total Number of values written by this device including incorrect ones.*

IEC 61850 . **NoOfDataWrittenCorrect**	[Operation / Count and RevData / IEC 61850]
#	*Total Number of correctly written values by this device.*

IEC 61850 . **NoOfDataChangeNotification**	[Operation / Count and RevData / IEC 61850]
#	*Number of detected changes within the datasets that are published with GOOSE messages.*

IEC 61850 . **No of Client Connections**	[Operation / Count and RevData / IEC 61850]
#	*Number of active MMS client connections*

8.6.6 IEC 61850 – Virt.Outp.

IEC 61850 communication

8.6.6.1 IEC 61850: Global Parameters

IEC 61850 . **COUTGGIO1.Ind1.stVal** **. . .** IEC 61850 . **COUTGGIO1.Ind32.stVal**	[Device Para / IEC 61850 / Virtual Outputs 1]	
“-”	“-” . . . Sys . Internal test state 1..n, Assignment List.	S.3
Virtual Output. This signal can be assigned or visualized via the SCD file to other devices within the IEC61850 substation.		

8.6.6.2 IEC 61850: Input States

IEC 61850 . **COUTGGIO1.Ind1.stVal-I** **. . .** IEC 61850 . **COUTGGIO1.Ind32.stVal-I**	[Operation / Status Display / IEC 61850 / Virtual Outputs 1]
Module input state: Binary state of the Virtual Output (GGIO)	

8.7 IEC103

IEC 60870-5-103 communication

8.7.1 IEC103: Global Parameters

IEC103 . **Function**	[Device Para / IEC103]	
inactive	inactive, active ↳ Mode.	S.3
Activation or deactivation of the IEC103 communication.		

IEC103 . **Slave ID**	[Device Para / IEC103]	
1	1 ... 247	S.3
Device address (Slave ID) within the bus system. Each device address has to be unique within a bus system.		

IEC103 . **Baud rate**	[Device Para / IEC103]	
19200	1200, 2400, 4800, 9600, 19200, 38400, 57600 ↳ Baud rate.	S.3
Baud rate		

IEC103 . **Physical Settings**	[Device Para / IEC103]	
8E1	8E1, 8O1, 8N1, 8N2 ↳ Byte Frame.	S.3
Digit 1: Number of bits. Digit 2: E=even parity, O=odd parity, N=no parity. Digit 3: Number of stop bits. More information on the parity: It is possible that the last data bit is followed by a parity bit which is used for recognition of communication errors. The parity bit ensures that with even parity ("EVEN") always an even number of bits with valence "1" or with odd parity ("ODD") an odd number of "1" valence bits are transmitted. But it is also possible to transmit no parity bits (here the setting is "Parity = None"). More information on the stop-bits: The end of a data byte is terminated by the stop-bits.		

IEC103 . **t-call**	[Device Para / IEC103]	
60s	1s ... 3600s	S.3
If there is no request telegram sent from Scada to the device after expiry of this time - the device concludes a communication failure within the Scada system.		

IEC103 . **Transm priv meas val**	[Device Para / IEC103]	
inactive	inactive, active ↳ Mode.	S.3
Transmit additional (private) measuring values		

IEC103 . **Transfer Disturb Rec**	[Device Para / IEC103]	
inactive	inactive, active ↳ Mode.	S.3
Activates the transmission of disturbance records		

IEC103 . **Timezone**	[Device Para / IEC103]	
UTC	UTC, Local Time ↳ Timezone.	S.3
Selection whether the timestamps in IEC103 messages shall be given as UTC or local time. (“Local time” always includes the actual daylight saving settings.)		

IEC103 . **DFC-Compat.**	[Device Para / IEC103]	
inactive	inactive, active ↳ Mode.	S.3
This setting is only required for certain substation implementations. If there should be communication problems related to the Command Response Queue this setting switches the device over to a different behavior.		

IEC103 . **Optical rest position**	[Device Para / IEC103]	
Light on *Avail. depends on HW*	Light off, Light on ↳ Optical rest position.	S.3
Optical rest position		

IEC103 . **Ex activate test mode**	[Service / Test (Prot inhibit) / Scada / IEC103]	
Sgen . Running	“-” . . . Sys . Internal test state ↳ 1..n, Assignment List.	S.3
The signal assigned to this parameter switches the IEC103 communication into Test Mode.		

IEC103 . **Ex activate Block MD**	[Service / Test (Prot inhibit) / Scada / IEC103]	
"-"	"-" . . . Sys . Internal test state ↳ 1..n, Assignment List.	S.3
The signal assigned to this parameter activates the blocking of IEC103 transmission in monitor direction.		

8.7.2 IEC103: Direct Controls

IEC103 . **Res all Diag Cr**	[Operation / Reset]	
inactive	inactive, active ↳ Mode.	S.3
Reset all diagnosis counters		

IEC103 . **Activate test mode**	[Service / Test (Prot inhibit) / Scada / IEC103]	
inactive	inactive, active ↳ Mode.	S.3
This Direct Control parameter switches the IEC103 communication into Test Mode (or back to nomal mode).		

IEC103 . **Activate Block MD**	[Service / Test (Prot inhibit) / Scada / IEC103]	
inactive	inactive, active ↳ Mode.	S.3
This Direct Control parameter activates (or deactivates) the blocking of IEC103 transmission in monitor direction.		

8.7.3 IEC103: Signals (Output States)

IEC103 . **Scada Cmd 1** **. . .** IEC103 . **Scada Cmd 10**	[Operation / Status Display / IEC103]
Scada Command	

IEC103 . **Transmission**	[Operation / Status Display / IEC103]
⇧	*Signal: SCADA active*

IEC103 . **Failure Event lost**	[Operation / Status Display / IEC103]
⇧	*Failure event lost*

IEC103 . **Test mode active**	[Operation / Status Display / IEC103]
⇧	*Signal: IEC103 communication has been switched over into Test Mode.*

IEC103 . **Block MD active**	[Operation / Status Display / IEC103]
⇧	*Signal: The blocking of IEC103 transmission in monitor direction has been activated.*

8.7.4 IEC103: Counters

IEC103 . **NReceived**	[Operation / Count and RevData / IEC103]
#	*Total Number of received Messages*

IEC103 . **NSent**	[Operation / Count and RevData / IEC103]
#	*Total Number of sent Messages*

IEC103 . **NBadFramings**	[Operation / Count and RevData / IEC103]
#	*Number of bad Messages*

IEC103 . **NBadParities**	[Operation / Count and RevData / IEC103]
#	*Number of Parity Errors*

IEC103 . **NBreakSignals**	[Operation / Count and RevData / IEC103]
#	*Number of Communication Interrupts*

IEC103 . **NInternalError**	[Operation / Count and RevData / IEC103]
#	*Number of Internal Errors*

IEC103 . **NBadCharChecksum**	[Operation / Count and RevData / IEC103]
#	*Number of Checksum Errors*

8.8 IEC104

IEC 60870-5-104 communication

8.8.1 IEC104: Global Parameters

IEC104 . **Function**	[Device Para / IEC104 / General Settings]	
inactive	inactive, active ↳ Mode.	S.3
Activation or deactivation of the IEC104 communication.		

IEC104 . **TCP Port Config**	[Device Para / IEC104 / General Settings]	
Default	Default, Private ↳ Port selection.	S.3
TCP Port Configuration. This parameter needs to be set to “Private” only if another TCP Port than the default one shall be used.		

IEC104 . **Port**	[Device Para / IEC104 / General Settings]	
2404	If: IEC104 . TCP Port Config = Default • 2404 ... 2404 If: IEC104 . TCP Port Config = Private • 49152 ... 65535	S.3
IP Port Number. *In general it is recommended to keep the default value. if this is not possible then select a number out of the private range 49152-52151 or 52164-65535 that is not yet in use within your network.*		

IEC104 . **Timezone**	[Device Para / IEC104 / General Settings]	
UTC	UTC, Local Time ↳ Timezone.	S.3
Selection whether the timestamps in the transmitted communication telegrams shall be given as UTC or local time. (“Local time” always includes the actual daylight saving settings.)		

IEC104 . **Deadb integr time**	[Device Para / IEC104 / General Settings]	
1s	0s ... 1000s	S.3
Deadband integration time.		

IEC104 . **Timeout SBE**	[Device Para / IEC104 / General Settings]	
30s	1s ... 60s	S.3
The communication outputs can be controlled in a two-stage procedure (SBE: Select Before Execute). These outputs have to be selected first by a Select command. After this the bit is reserved for this Execute request. This setting defines the timer for this reservation: After the timer has elapsed the bit is released.		

IEC104 . **Timeout t0**	[Device Para / IEC104 / Advanced]	
30s	30s ... 30s	S.3
Timeout of connection establishment		

IEC104 . **Timeout t1**	[Device Para / IEC104 / Advanced]	
15s	15s ... 15s	S.3
Timeout of send or test APDUs		

IEC104 . **Timeout t2**	[Device Para / IEC104 / Advanced]	
10s	10s ... 10s	S.3
Timeout for acknowledges in case of no data messages		

IEC104 . **Timeout t3**	[Device Para / IEC104 / Advanced]	
20s	20s ... 20s	S.3
Timeout for sending test frames in case of a long idle state		

IEC104 . **Param k**	[Device Para / IEC104 / Advanced]	
12	12 ... 12	S.3
Protocol parameter k		

IEC104 . **Param w**	[Device Para / IEC104 / Advanced]	
8	8 ... 8	S.3
Protocol parameter w		

IEC104 . **Length of address**	[Device Para / IEC104 / Advanced]	
2	2 ... 2	S.3
Number of bytes of the Common Address of the ASDU		

IEC104 . **Length of CoT**	[Device Para / IEC104 / Advanced]	
2	2 ... 2	S.3
Number of bytes of the Cause of Transmission		

IEC104 . **Length of Inf Obj addr**	[Device Para / IEC104 / Advanced]	
3	3 ... 3	S.3
Number of bytes of the address of the Information Object		

IEC104 . **Update time**	[Device Para / IEC104 / Advanced]	
1s	1s ... 60s	S.3
This setting specifies the time after which measurement values are refreshed. If cyclic transmission is selected new values are reported after this time has elapsed.		

IEC104 . **Transmit Int. State**	[Device Para / IEC104 / Advanced]	
active	inactive, active ↳ Mode.	S.3
If this parameter is set to “active” (default) then the intermediate position of a switchgear, too, is transmitted. This needs to be changed to “inactive” only in the rare case that the substation communication does not support the reporting of intermediate positions.		

IEC104 . **Trans. Cmd. State**	[Device Para / IEC104 / Advanced]	
active	inactive, active ↳ Mode.	S.3
_ If false it suppress change events for command states (Same address as cmd)		

IEC104 . **Type of SCADA mapping**	[Device Para / IEC104 / Config. Data Obj.]	
Standard	Standard, User-defined ↳ Type of SCADA mapping.	S.3
*This setting decides whether the communication protocol shall use the default mapping of data objects, or some user-defined mapping that has been loaded from a *.HptSMap file.*		

8.8.2 IEC104: Direct Controls

IEC104 . **Res all Diag Cr**	[Operation / Reset]	
inactive	inactive, active Mode.	S.3
◉	*Reset all diagnosis counters*	

IEC104 . **Common address**	[Device Para / IEC104 / General Settings]	
1	1 . . . 65535	S.3
◉	*Common Address of the ASDU*	

8.8.3 IEC104: Signals (Output States)

IEC104 . **Scada Cmd 1** **. . .** IEC104 . **Scada Cmd 16**	[Operation / Status Display / IEC104]
⇧	*Scada Command*

IEC104 . **busy**	[Operation / Status Display / IEC104]
⇧	*This message is set if the protocol is started. It will be reset if the protocol is shut down.*

IEC104 . **ready**	[Operation / Status Display / IEC104]
⇧	*The message will be set if the protocol is successfully started and ready for data exchange.*

IEC104 . **Transmission**	[Operation / Status Display / IEC104]
⇧	*Signal: SCADA active*

IEC104 . **Failure Event lost**	[Operation / Status Display / IEC104]
⇧	*Failure event lost*

8.8.4 IEC104: Values

IEC104 . **Config info**	[Device Para / IEC104 / Config. Data Obj.]
⇘	*Configuration comment (entered by the user during SCADA configuration)*

IEC104 . **Config version**	[Device Para / IEC104 / Config. Data Obj.]
✎	*Version of the user-defined SCADA configuration*

IEC104 . **Config status**	[Device Para / IEC104 / Config. Data Obj.]	
Changing	Changing, OK, Config. not avail., Error ↳ Config status.	
✎	*Status of the user-defined SCADA configuration.* *Possible values:* *- Changing: New SCADA configuration is being loaded, but not active yet.* *- OK: The SCADA configuration is active.* *- Config. not avail.: The user-defined SCADA configuration is not available (e.g. has not been loaded into the device).* *- Error: Unexpected error. Please contact our service-team.*	

8.8.5 IEC104: Counters

IEC104 . **NReceived**	[Operation / Count and RevData / IEC104]
#	*Diagnostic counter: Number of received characters*

IEC104 . **NSent**	[Operation / Count and RevData / IEC104]
#	*Diagnostic counter: Number of sent characters*

IEC104 . **Num. of lost conn.**	[Operation / Count and RevData / IEC104]
#	*Diagnostic counter: Number of lost connections*

IEC104 . **NBadChecksum**	[Operation / Count and RevData / IEC104]
#	*Diagnostic counter: Number of frames received with bad checksum.*

8.9 Profibus

Profibus Module

8.9.1 Profibus: Global Parameters

Profibus . **Config Bin Inp 1** ... Profibus . **Config Bin Inp 32**	[Device Para / Profibus / Config Bin Inp 1-16] [Device Para / Profibus / Config Bin Inp 17-32]	
"-"	"-" ... Sys . Internal test state ↳ 1..n, Assignment List.	S.3
Virtual Digital Input. This corresponds to a virtual binary output of the protective device.		

Profibus . **Latched 1** ... Profibus . **Latched 32**	[Device Para / Profibus / Config Bin Inp 1-16] [Device Para / Profibus / Config Bin Inp 17-32]	
inactive	inactive, active ↳ Mode.	S.3
Defines whether the Input is latched.		

Profibus . **Type of SCADA mapping**	[Device Para / Profibus / Config. Data Obj.]	
Standard	Standard, User-defined ↳ Type of SCADA mapping.	S.3
*This setting decides whether the communication protocol shall use the default mapping of data objects, or some user-defined mapping that has been loaded from a *.HptSMap file.*		

8.9.2 Profibus: Direct Controls

Profibus . **Slave ID**	[Operation / Status Display / Profibus / State] [Device Para / Profibus / Bus parameters]	
2	2 ... 125	P.1
Device address (Slave ID) within the bus system. Each device address has to be unique within a bus system.		

Profibus . **Reset Comds**	[Operation / Reset]	
inactive	inactive, active Mode.	P.1
All Profibus Commands will be reset.		

8.9.3 Profibus: Input States

Profibus . **Assignment 1-I** **...** Profibus . **Assignment 32-I**	[Operation / Status Display / Profibus / Config Bin Inp 1-16] [Operation / Status Display / Profibus / Config Bin Inp 17-32]
Module input state: Scada Assignment	

8.9.4 Profibus: Signals (Output States)

Profibus . **Data OK**	[Operation / Status Display / Profibus / State]
Data within the Input field are OK (Yes=1)	

Profibus . **SubModul Err**	[Operation / Status Display / Profibus / State]
Assignable Signal, Failure in Sub-Module, Communication Failure.	

Profibus . **Connection active**	[Operation / Status Display / Profibus / State]
Connection active	

Profibus . **Scada Cmd 1** **...** Profibus . **Scada Cmd 16**	[Operation / Status Display / Profibus / Commands]
Scada Command	

8.9.5 Profibus: Values

Profibus . **Slave State**	[Operation / Status Display / Profibus / State]
Baud Search	Baud Search . . . Data exchange ↳ State.
✎ *Communication State between Slave and Master.*	

Profibus . **Baud rate**	[Operation / Status Display / Profibus / State]
-.-	12 Mb/s . . . -.- ↳ Baud rate.
✎ *The baud rate that has been detected lastly, will still be shown after a connection issue.*	

Profibus . **PNO Id**	[Operation / Status Display / Profibus / State]
0C50h	0C50h ↳ PNO Id.
✎ *PNO Identification Number. GSD Identification Number.*	

Profibus . **Config info**	[Operation / Status Display / Profibus / State] [Device Para / Profibus / Config. Data Obj.]
✎ *Configuration comment (entered by the user during SCADA configuration)*	

Profibus . **Config version**	[Operation / Status Display / Profibus / State] [Device Para / Profibus / Config. Data Obj.]
✎ *Version of the user-defined SCADA configuration*	

Profibus . **Config status**	[Operation / Status Display / Profibus / State] [Device Para / Profibus / Config. Data Obj.]
Changing	Changing, OK, Config. not avail., Error ↳ Config status.
✎ *Status of the user-defined SCADA configuration.* *Possible values:*	

8.9.6 Profibus: Counters

Profibus . **Master ID**	[Operation / Status Display / Profibus / State]
#	*Device address (Master ID) within the bus system. Each device address has to be unique within a bus system.*

Profibus . **HO Id PSub**	[Operation / Status Display / Profibus / State]
#	*Handoff Id of PbSub*

Profibus . **t-WatchDog**	[Operation / Status Display / Profibus / State]
#	*The Profibus Chip detects a communication issue if this timer is expired without any communication (Parameterising telegram).*

Profibus . **Fr Sync Err**	[Operation / Count and RevData / Profibus]
#	*Frames, that were sent from the Master to the Slave are faulty.*

Profibus . **Num. CRC err.**	[Operation / Count and RevData / Profibus]
#	*Number of CRC errors that the subsystem manager has recognized in the received response frames from the subsystem. (Each error caused a subsystem reset.)*

Profibus . **Num. frame loss err.**	[Operation / Count and RevData / Profibus]
#	*Number of frame loss errors that the subsystem manager has recognized in the received response frames from the subsystem. (Each error caused a subsystem reset.)*

Profibus . **Num. trig. CRC err.**	[Operation / Count and RevData / Profibus]
#	*Number of CRC errors that the subsystem has recognized in the received trigger frames from the host.*

Profibus . **Num. subsys. res.**	[Operation / Count and RevData / Profibus]
#	*Number of subsystem restarts or resets that the subsystem manager has caused.*

8.10 IRIG-B

IRIG-B-Module

8.10.1 IRIG-B: Device Planning Parameters

IRIG-B . **Mode**	[Device planning]	
"-"	"-", use ↳ Mode.	S.3
IRIG-B-Module, general operation mode		

8.10.2 IRIG-B: Global Parameters

IRIG-B . **Function**	[Device Para / Time / TimeSync / IRIG-B]	
inactive	inactive, active ↳ Mode.	S.3
Permanent activation or deactivation of module/stage.		

IRIG-B . **IRIG-B00X**	[Device Para / Time / TimeSync / IRIG-B]	
IRIGB-000	IRIGB-000 . . . IRIGB-007 ↳ IRIG-B00X.	S.3
Determination of the Type: IRIG-B00X. IRIG-B types differ in types of included "Coded Expressions" (year, control-functions, straight-binary-seconds).		

8.10.3 IRIG-B: Direct Controls

IRIG-B . **Res IRIG-B Cr**	[Operation / Reset]	
inactive	inactive, active ↳ Mode.	P.1
Resetting of the Diagnosis Counters: IRIG-B		

8.10.4 IRIG-B: Signals (Output States)

IRIG-B . **IRIG-B active**	[Operation / Status Display / TimeSync / IRIG-B]
⇫	*Signal: If there is no valid IRIG-B signal for 60 sec, IRIG-B is regarded as inactive.*

IRIG-B . **High-Low Invert**	[Operation / Status Display / TimeSync / IRIG-B]
⇫	*Signal: The High and Low signals of the IRIG-B are inverted. This does NOT mean that the wiring is faulty. If the wiring is faulty no IRIG-B signal will be detected.*

IRIG-B . **Control Signal1** **...** IRIG-B . **Control Signal18**	[Operation / Status Display / TimeSync / IRIG-B]
⇫	*Signal: IRIG-B Control Signal. The external IRIG-B generator can set these signals. They can be used for further control procedures inside the device (e.g. logic funtions).*

8.10.5 IRIG-B: Counters

IRIG-B . **NoOfFramesOK**	[Operation / Count and RevData / TimeSync / IRIG-B]
#	*Total Number valid Frames.*

IRIG-B . **NoOfFrameErrors**	[Operation / Count and RevData / TimeSync / IRIG-B]
#	*Total Number of Frame Errors. Physically corrupted Frame.*

IRIG-B . **Edges**	[Operation / Count and RevData / TimeSync / IRIG-B]
#	*Edges: Total number of rising and falling edges. This signal indicates if a signal is available at the IRIG-B input.*

8.11 SNTP

SNTP-Module

8.11.1 SNTP: Device Planning Parameters

SNTP . **Mode**	[Device planning]	
“-”	“-”, use ↳ Mode.	S.3
SNTP-Module, general operation mode		

8.11.2 SNTP: Global Parameters

SNTP . **Server1**	[Device Para / Time / TimeSync / SNTP]	
inactive	inactive, active ↳ Mode.	S.3
Server 1		

SNTP . **IP Byte1** **...** SNTP . **IP Byte4**	[Device Para / Time / TimeSync / SNTP]	
0	0 ... 255	S.3
IP1.IP2.IP3.IP4		

SNTP . **Server2**	[Device Para / Time / TimeSync / SNTP]	
inactive	inactive, active ↳ Mode.	S.3
Server 2		

8.11.3 SNTP: Direct Controls

SNTP . **Res Counter**	[Operation / Reset]	
inactive	inactive, active ↳ Mode.	P.1
◉	*Reset all Counters.*	

8.11.4 SNTP: Signals (Output States)

SNTP . **SNTP active**	[Operation / Status Display / TimeSync / SNTP]
⇪	*Signal: If there is no valid SNTP signal for 120 sec, SNTP is regarded as inactive.*

8.11.5 SNTP: Values

SNTP . **Used Server**	[Operation / Status Display / TimeSync / SNTP]	
None	Server1, Server2, None ↳ Server State.	
⟍	*Which Server is used for SNTP synchronization.*	

SNTP . **PrecServer1**	[Operation / Status Display / TimeSync / SNTP]
⟍	*Precision of Server 1*

SNTP . **PrecServer2**	[Operation / Status Display / TimeSync / SNTP]
⟍	*Precision of Server 2*

SNTP . **ServerQlty**	[Operation / Status Display / TimeSync / SNTP]	
“-”	GOOD, SUFFICIENT, BAD, “-” ↳ State.	
⟍	*Quality of Server used for Synchronization (GOOD, SUFFICIENT, BAD)*	

SNTP . **NetConn**	[Operation / Status Display / TimeSync / SNTP]	
“-”	GOOD, SUFFICIENT, BAD, “-” State.	
Quality of Network Connection (GOOD, SUFFICIENT, BAD).		

8.11.6 SNTP: Counters

SNTP . **StratumServer1**	[Operation / Status Display / TimeSync / SNTP]
Stratum of Server 1	

SNTP . **StratumServer2**	[Operation / Status Display / TimeSync / SNTP]
Stratum of Server 2	

SNTP . **NoOfSyncs**	[Operation / Count and RevData / TimeSync / SNTP]
Total Number of Synchronizations.	

SNTP . **NoOfConnectLost**	[Operation / Count and RevData / TimeSync / SNTP]
Total Number of lost SNTP Connections (no sync for 120 sec).	

SNTP . **NoOfSmallSyncs**	[Operation / Count and RevData / TimeSync / SNTP]
Service counter: Total Number of very small Time Corrections.	

SNTP . **NoOfNormSyncs**	[Operation / Count and RevData / TimeSync / SNTP]
Service counter: Total Number of normal Time Corrections	

SNTP . **NoOfBigSyncs**	[Operation / Count and RevData / TimeSync / SNTP]
Service counter: Total Number of big Time Corrections	

SNTP . **NoOfFiltSyncs**	[Operation / Count and RevData / TimeSync / SNTP]
Service counter: Total Number of filtered Time Corrections	

SNTP . **NoOfSlowTrans**	[Operation / Count and RevData / TimeSync / SNTP]
Service counter: Total Number of slow Transfers.	

SNTP . **NoOfHighOffs**	[Operation / Count and RevData / TimeSync / SNTP]
#	*Service counter: Total Number of high Offsets.*

SNTP . **NoOfIntTimeouts**	[Operation / Count and RevData / TimeSync / SNTP]
#	*Service counter: Total Number of internal timeouts.*

8.12 TimeSync

Time synchronisation

Date and Time	[Device Para / Time / Date and Time]
This item represents a special dialog. (See the Technical Manual for details.) *(Re-)setting Date and Time*	

8.12.1 TimeSync: Global Parameters

TimeSync . **Time Zones**	[Device Para / Time / Timezone]	
UTC+0 London	UTC+14 Kiritimati ... UTC-11 Midway Islands ↳ Time Zones.	S.3
Time Zones		

TimeSync . **DST offset**	[Device Para / Time / Timezone]	
60min	-180min ... 180min	S.3
Difference to wintertime		

TimeSync . **DST manual**	[Device Para / Time / Timezone]	
active	inactive, active ↳ Mode.	S.3
Manual setting of the Daylight Saving Time		

TimeSync . **Summertime**	[Device Para / Time / Timezone]	
inactive	inactive, active ↳ Mode.	S.3
Daylight Saving Time		

TimeSync . **Summertime m**	[Device Para / Time / Timezone]	
March	January ... December ↳ Month of clock change.	S.3
Month of clock change summertime		

TimeSync . **Summertime d**	[Device Para / Time / Timezone]	
Sunday	Sunday ... General day ↳ Date.	S.3
Day of clock change summertime		

TimeSync . **Summertime w**	[Device Para / Time / Timezone]	
Last	First, Second, Third, Fourth, Last ↳ Day of clock change.	S.3
Place of selected day in month (for clock change summertime)		

TimeSync . **Summertime h**	[Device Para / Time / Timezone]	
2h	0h ... 23h	S.3
Hour of clock change summertime		

TimeSync . **Summertime min**	[Device Para / Time / Timezone]	
0min	0min ... 59min	S.3
Minute of clock change summertime		

TimeSync . **Wintertime m**	[Device Para / Time / Timezone]	
October	January ... December ↳ Month of clock change.	S.3
Month of clock change wintertime		

TimeSync . **Wintertime d**	[Device Para / Time / Timezone]	
Sunday	Sunday ... General day ↳ Date.	S.3
Day of clock change wintertime		

TimeSync . **Wintertime w**	[Device Para / Time / Timezone]	
Last	First, Second, Third, Fourth, Last ↳ Day of clock change.	S.3
Place of selected day in month (for clock change wintertime)		

TimeSync . **Wintertime h**	[Device Para / Time / Timezone]	
3h	0h . . . 23h	S.3
Hour of clock change wintertime		

TimeSync . **Wintertime min**	[Device Para / Time / Timezone]	
0min	0min . . . 59min	S.3
Minute of clock change wintertime		

TimeSync . **TimeSync**	[Device Para / Time / TimeSync / TimeSync]	
“-”	“-”, IRIG-B . IRIG-B, SNTP . SNTP, Modbus . Modbus, IEC103 . IEC 60870-5-103, IEC104 . IEC104, DNP3 . DNP3 Used Protocol.	S.3
Time synchronisation		

8.12.2 TimeSync: Signals (Output States)

TimeSync . **synchronized**	[Operation / Status Display / TimeSync / TimeSync]
Clock is synchronized.	

9 Protection Parameter

Module General Protection

9.1 Prot: Global Parameters

Prot . **Function**	[Protection Para / Global Prot Para / Prot]	
active	inactive, active ↳ Mode.	P.2
Permanent activation or deactivation of module/stage.		

Prot . **ExBlo Fc**	[Protection Para / Global Prot Para / Prot]	
inactive	inactive, active ↳ active/inactive.	P.2
Activate (allow) the external blocking of the global protection functionality of the device.		

Prot . **ExBlo1** Prot . **ExBlo2**	[Protection Para / Global Prot Para / Prot]	
“-”	“-” . . . Sys . Internal test state ↳ 1..n, Assignment List.	P.2
If external blocking of this module is activated (allowed), the global protection functionality of the device will be blocked if the state of the assigned signal becomes true.		

Prot . **Blo TripCmd**	[Protection Para / Global Prot Para / Prot]	
inactive	inactive, active ↳ Mode.	P.2
Permanent blocking of the Trip Command of the entire Protection.		

Prot . **ExBlo TripCmd Fc**	[Protection Para / Global Prot Para / Prot]	
inactive	inactive, active ↳ active/inactive.	P.2
Activate (allow) the external blocking of the trip command of the entire device.		

Prot . **ExBlo TripCmd**	[Protection Para / Global Prot Para / Prot]	
"-"	"-" . . . Sys . Internal test state ↳ 1..n, Assignment List.	P.2
If external blocking of the tripping command is activated (allowed), the tripping command of the entire device will be blocked if the state of the assigned signal becomes true.		

9.2 Prot: Direct Controls

Prot . **Res FaultNo a GridFaultNo**	[Operation / Reset]	
inactive	inactive, active ↳ Mode.	P.1
Resetting of fault number and grid fault number.		

9.3 Prot: Input States

Prot . **ExBlo1-I**	[Operation / Status Display / Prot]
Module input state: External blocking1	

Prot . **ExBlo2-I**	[Operation / Status Display / Prot]
Module input state: External blocking2	

Prot . **ExBlo TripCmd-I**	[Operation / Status Display / Prot]
Module input state: External Blocking of the Trip Command	

9.4 Prot: Signals (Output States)

Prot . **active**	[Operation / Status Display / All Actives] [Operation / Status Display / Prot]
Signal: active	

Prot . **Alarm**	[Operation / Status Display / Alarms] [Operation / Status Display / Prot]
Signal: General Alarm	

Prot . **Trip**	[Operation / Status Display / Trips] [Operation / Status Display / Prot]
⇧	*Signal: General Trip*

Prot . **available**	[Operation / Status Display / Prot]
⇧	*Signal: Protection is available*

Prot . **ExBlo**	[Operation / Status Display / Prot]
⇧	*Signal: External Blocking*

Prot . **Blo TripCmd**	[Operation / Status Display / Prot]
⇧	*Signal: Trip Command blocked*

Prot . **ExBlo TripCmd**	[Operation / Status Display / Prot]
⇧	*Signal: External Blocking of the Trip Command*

Prot . **Alarm L1**	[Operation / Status Display / Prot]
⇧	*Signal: General-Alarm L1*

Prot . **Alarm L2**	[Operation / Status Display / Prot]
⇧	*Signal: General-Alarm L2*

Prot . **Alarm L3**	[Operation / Status Display / Prot]
⇧	*Signal: General-Alarm L3*

Prot . **Alarm G**	[Operation / Status Display / Prot]
⇧	*Signal: General-Alarm - Earth fault*

Prot . **Trip L1**	[Operation / Status Display / Prot]
⇧	*Signal: General Trip L1*

Prot . **Trip L2**	[Operation / Status Display / Prot]
⇧	*Signal: General Trip L2*

Prot . **Trip L3**	[Operation / Status Display / Prot]
⇧	*Signal: General Trip L3*

Prot . **Trip G**	[Operation / Status Display / Prot]
⇧	*Signal: General Trip Ground fault*

Prot . **Res FaultNo a GridFaultNo**	[Operation / Status Display / Prot]
⇧	*Signal: Resetting of fault number and grid fault number.*

Prot . **FaultNo**	[Operation / Count and RevData / Prot]
⇧	*Fault number*

Prot . **No. of Grid Fault**	[Operation / Count and RevData / Prot]
⇧	*Number of grid fault: A grid fault, e.g. a short circuit, might cause several faults with trip and autoreclosing; in this case, the fault number counts each fault, but the grid fault number remains the same.*

9.5 V[1] . . . V[6]

Voltage-stage

9.5.1 V[1]: Device Planning Parameters

V[1] . **Mode**	[Device planning]	
V>	"-", V>, V< ↳ Device planning.	S.3
Voltage-stage, general operation mode		

9.5.2 V[1]: Global Parameters

V[1] . **ExBlo1** V[1] . **ExBlo2**	[Protection Para / Global Prot Para / V-Prot / V[1]]	
"-"	"-" . . . Sys . Internal test state ↳ 1..n, Assignment List.	P.2
External blocking of the module, if blocking is activated (allowed) within a parameter set and if the state of the assigned signal is true.		

V[1] . **ExBlo TripCmd**	[Protection Para / Global Prot Para / V-Prot / V[1]]	
"-"	"-" . . . Sys . Internal test state ↳ 1..n, Assignment List.	P.2
External blocking of the Trip Command of the module/the stage, if blocking is activated (allowed) within a parameter set and if the state of the assigned signal is true.		

9.5.3 V[1]: Setting Group Parameters

V[1] . **Function**	[Protection Para / Set 1...4 / V-Prot / V[1]]	
active	inactive, active ↳ Mode.	P.2
Permanent activation or deactivation of module/stage.		

V[1] . **ExBlo Fc**	[Protection Para / Set 1...4 / V-Prot / V[1]]	
inactive	inactive, active ↳ active/inactive.	P.2
Activate (allow) or inactivate (disallow) blocking of the module/stage. This parameter is only effective if a signal is assigned to the corresponding global protection parameter. If the signal becomes true, those modules/stages are blocked that are parameterized "ExBlo Fc=active".		

V[1] . **Blo TripCmd**	[Protection Para / Set 1...4 / V-Prot / V[1]]	
inactive	inactive, active ↳ Mode.	P.2
Permanent blocking of the Trip Command of the module/stage.		

V[1] . **ExBlo TripCmd Fc**	[Protection Para / Set 1...4 / V-Prot / V[1]]	
inactive	inactive, active ↳ active/inactive.	P.2
Activate (allow) or inactivate (disallow) blocking of the module/stage. This parameter is only effective if a signal is assigned to the corresponding global protection parameter. If the signal becomes true, those modules/stages are blocked that are parameterized "ExBlo TripCmd Fc=active".		

V[1] . **Measuring Mode**	[Protection Para / Set 1...4 / V-Prot / V[1]]	
Phase to Ground	Phase to Ground, Phase to Phase ↳ Measuring Mode.	P.2
Measuring/Supervision Mode: Determines if the phase-to-phase or phase-to-earth voltages are to be supervised		

V[1] . **Measuring method**	[Protection Para / Set 1...4 / V-Prot / V[1]]	
Fundamental	Fundamental, True RMS, Vavg ↳ Measuring method.	P.2
Measuring method: fundamental or rms or "sliding average supervision"		

V[1] . **Alarm Mode**	[Protection Para / Set 1...4 / V-Prot / V[1]]	
any one	any one, any two, all ↳ Alarm Mode.	P.2
Alarm criterion for the voltage protection stage.		

V[1] . **V>**	[Protection Para / Set 1...4 / V-Prot / V[1]]	
1.1Vn	0.01Vn . . . 2.000Vn	P.2
If the pickup value is exceeded, the module/element will be started. The definition of Vn is dependent on both the Field Parameter »VT con« and the Setting Group Parameter »Measuring Mode«: If the measuring inputs of the voltage measuring card are fed with phase-to-ground voltages (»VT con« = "Phase-to-Ground") then the setting »Measuring Mode« = "Phase-to-Ground" means that Vn=VTsec/SQRT(3), and »Measuring Mode« = "Phase-to-Phase" means that Vn=VTsec. However, if the measuring inputs of the voltage measuring card are fed with phase-to-phase voltages (»VT con« = "Phase-to-Phase") then the setting of "Measuring Mode" is ignored and internally set to "Phase-to-Phase" instead, so that Vn=VTsec.		

V[1] . **V> Reset%**	[Protection Para / Set 1...4 / V-Prot / V[1]]	
98.5%	80% . . . 99.0%	P.2
Drop Out (is in percent of setting)		

V[1] . **V<**	[Protection Para / Set 1...4 / V-Prot / V[1]]	
0.80Vn	0.01Vn . . . 2.000Vn	P.2
If the pickup value is exceeded, the module/element will be started. The definition of Vn is dependent on both the Field Parameter »VT con« and the Setting Group Parameter »Measuring Mode«: If the measuring inputs of the voltage measuring card are fed with phase-to-ground voltages (»VT con« = "Phase-to-Ground") then the setting »Measuring Mode« = "Phase-to-Ground" means that Vn=VTsec/SQRT(3), and »Measuring Mode« = "Phase-to-Phase" means that Vn=VTsec. However, if the measuring inputs of the voltage measuring card are fed with phase-to-phase voltages (»VT con« = "Phase-to-Phase") then the setting of "Measuring Mode" is ignored and internally set to "Phase-to-Phase" instead, so that Vn=VTsec.		

V[1] . **V< Reset%**	[Protection Para / Set 1...4 / V-Prot / V[1]]	
101.5%	101% . . . 110.0%	P.2
Drop Out (is in percent of setting)		

V[1] . **t**	[Protection Para / Set 1...4 / V-Prot / V[1]]	
1s	0.00s . . . 3000.00s	P.2
Tripping delay		

V[1] . **Meas Circuit Superv**	[Protection Para / Set 1...4 / V-Prot / V[1]]	
Sys . inactive	Sys . inactive, VTS . active VTS Block.	P.2
Activates the use of the measuring circuit supervision. In this case the module will be blocked if a measuring circuit supervision module (e.g. LOP, VTS) signals a disturbed measuring circuit (e.g. caused by a fuse failure).		

9.5.4 V[1]: Input States

V[1] . **ExBlo1-I**	[Operation / Status Display / V-Prot / V[1]]
⇩	*Module input state: External blocking1*

V[1] . **ExBlo2-I**	[Operation / Status Display / V-Prot / V[1]]
⇩	*Module input state: External blocking2*

V[1] . **ExBlo TripCmd-I**	[Operation / Status Display / V-Prot / V[1]]
⇩	*Module input state: External Blocking of the Trip Command*

9.5.5 V[1]: Signals (Output States)

V[1] . **active**	[Operation / Status Display / All Actives] [Operation / Status Display / V-Prot / V[1]]
⇧	*Signal: active*

V[1] . **Alarm**	[Operation / Status Display / Alarms] [Operation / Status Display / V-Prot / V[1]]
⇧	*Signal: Alarm voltage stage*

V[1] . **Trip**	[Operation / Status Display / Trips] [Operation / Status Display / V-Prot / V[1]]
⇧	*Signal: Trip*

V[1] . **TripCmd**	[Operation / Status Display / TripCmds] [Operation / Status Display / V-Prot / V[1]]
⇧	*Signal: Trip Command*

V[1] . **ExBlo**	[Operation / Status Display / V-Prot / V[1]]
⇧	*Signal: External Blocking*

V[1] . **Blo TripCmd**	[Operation / Status Display / V-Prot / V[1]]
⇧	*Signal: Trip Command blocked*

V[1] . **ExBlo TripCmd**	[Operation / Status Display / V-Prot / V[1]]
⇧	*Signal: External Blocking of the Trip Command*

V[1] . **Alarm L1**	[Operation / Status Display / V-Prot / V[1]]
⇧	*Signal: Alarm L1*

V[1] . **Alarm L2**	[Operation / Status Display / V-Prot / V[1]]
⇧	*Signal: Alarm L2*

V[1] . **Alarm L3**	[Operation / Status Display / V-Prot / V[1]]
⇧	*Signal: Alarm L3*

V[1] . **Trip L1**	[Operation / Status Display / V-Prot / V[1]]
⇧	*Signal: General Trip Phase L1*

V[1] . **Trip L2**	[Operation / Status Display / V-Prot / V[1]]
⇧	*Signal: General Trip Phase L2*

V[1] . **Trip L3**	[Operation / Status Display / V-Prot / V[1]]
⇧	*Signal: General Trip Phase L3*

9.6 df/dt

Rate-of-frequency-change.

9.6.1 df/dt: Device Planning Parameters

df/dt . **Mode**	[Device planning]	
“-”	“-”, use Device planning.	S.3
Frequency Protection Module, general operation mode		

9.6.2 df/dt: Global Parameters

df/dt . **ExBlo1** df/dt . **ExBlo2**	[Protection Para / Global Prot Para / Intercon-Prot / Mains Decouplg / df/dt]	
“-”	“-” . . . Sys . Internal test state 1..n, Assignment List.	P.2
External blocking of the module, if blocking is activated (allowed) within a parameter set and if the state of the assigned signal is true.		

df/dt . **ExBlo TripCmd**	[Protection Para / Global Prot Para / Intercon-Prot / Mains Decouplg / df/dt]	
“-”	“-” . . . Sys . Internal test state 1..n, Assignment List.	P.2
External blocking of the Trip Command of the module/the stage, if blocking is activated (allowed) within a parameter set and if the state of the assigned signal is true.		

9.6.3 df/dt: Setting Group Parameters

df/dt . **Function**	[Protection Para / Set 1...4 / Intercon-Prot / Mains Decouplg / df/dt]	
inactive	inactive, active Mode.	P.2
Permanent activation or deactivation of module/stage.		

df/dt . **ExBlo Fc**	[Protection Para / Set 1...4 / Intercon-Prot / Mains Decouplg / df/dt]	
inactive	inactive, active ↳ active/inactive.	P.2
Activate (allow) or inactivate (disallow) blocking of the module/stage. This parameter is only effective if a signal is assigned to the corresponding global protection parameter. If the signal becomes true, those modules/stages are blocked that are parameterized "ExBlo Fc=active".		

df/dt . **Blo TripCmd**	[Protection Para / Set 1...4 / Intercon-Prot / Mains Decouplg / df/dt]	
inactive	inactive, active ↳ Mode.	P.2
Permanent blocking of the Trip Command of the module/stage.		

df/dt . **ExBlo TripCmd Fc**	[Protection Para / Set 1...4 / Intercon-Prot / Mains Decouplg / df/dt]	
inactive	inactive, active ↳ active/inactive.	P.2
Activate (allow) or inactivate (disallow) blocking of the module/stage. This parameter is only effective if a signal is assigned to the corresponding global protection parameter. If the signal becomes true, those modules/stages are blocked that are parameterized "ExBlo TripCmd Fc=active".		

df/dt . **f>**	[Protection Para / Set 1...4 / Intercon-Prot / Mains Decouplg / df/dt]	
51.00Hz	40.00Hz ... 69.00Hz	P.2
Pickup value for overfrequency.		

df/dt . **f<**	[Protection Para / Set 1...4 / Intercon-Prot / Mains Decouplg / df/dt]	
49.00Hz	40.00Hz ... 69.00Hz	P.2
Pickup value for underfrequency.		

df/dt . **Freq. drop-off**	[Protection Para / Set 1...4 / Intercon-Prot / Mains Decouplg / df/dt]	
0.020Hz	0.010Hz ... 0.100Hz	P.2
Drop-off for the Frequency function. This setting modifies the shape of the hysteresis that is used for the frequency protection.		

df/dt . **t**	[Protection Para / Set 1...4 / Intercon-Prot / Mains Decouplg / df/dt]	
1.00s	0.00s ... 3600.00s	P.2
Tripping delay		

df/dt . **df/dt**	[Protection Para / Set 1...4 / Intercon-Prot / Mains Decouplg / df/dt]	
1.000Hz/s	0.100Hz/s ... 10.000Hz/s	P.2
Measured value (calculated): Rate-of-frequency-change.		

df/dt . **t-df/dt**	[Protection Para / Set 1...4 / Intercon-Prot / Mains Decouplg / df/dt]	
1.00s	0.00s ... 300.00s	P.2
Trip delay df/dt		

df/dt . **DF**	[Protection Para / Set 1...4 / Intercon-Prot / Mains Decouplg / df/dt]	
1.00Hz	0.0Hz ... 10.0Hz	P.2
Frequency difference for the maximum admissible variation of the mean of the rate of frequency-change. This function is inactive if DF=0.		

df/dt . **DT**	[Protection Para / Set 1...4 / Intercon-Prot / Mains Decouplg / df/dt]	
1.00s	0.1s ... 10.0s	P.2
Time interval of the maximum admissible rate-of-frequency-change.		

df/dt . **df/dt mode**	[Protection Para / Set 1...4 / Intercon-Prot / Mains Decouplg / df/dt]	
absolute df/dt	absolute df/dt, positive df/dt, negative df/dt Mode.	P.2
df/dt mode		

df/dt . **delta phi**	[Protection Para / Set 1...4 / Intercon-Prot / Mains Decouplg / df/dt]	
10°	1° ... 30°	P.2
Measured value (calculated): Vector surge		

9.6.4 df/dt: Input States

df/dt . **ExBlo1-I**	[Operation / Status Display / Intercon-Prot / Mains Decouplg / df/dt]
⇩	*Module input state: External blocking1*

df/dt . **ExBlo2-I**	[Operation / Status Display / Intercon-Prot / Mains Decouplg / df/dt]
⇩	*Module input state: External blocking2*

df/dt . **ExBlo TripCmd-I**	[Operation / Status Display / Intercon-Prot / Mains Decouplg / df/dt]
⇩	*Module input state: External Blocking of the Trip Command*

9.6.5 df/dt: Signals (Output States)

df/dt . **active**	[Operation / Status Display / All Actives] [Operation / Status Display / Intercon-Prot / Mains Decouplg / df/dt]
⇧	*Signal: active*

df/dt . **Alarm**	[Operation / Status Display / Alarms] [Operation / Status Display / Intercon-Prot / Mains Decouplg / df/dt]
⇧	*Signal: Alarm Frequency Protection (collective signal)*

df/dt . **Trip**	[Operation / Status Display / Trips] [Operation / Status Display / Intercon-Prot / Mains Decouplg / df/dt]
⇧	*Signal: Trip Frequency Protection (collective signal)*

df/dt . **TripCmd**	[Operation / Status Display / TripCmds] [Operation / Status Display / Intercon-Prot / Mains Decouplg / df/dt]
⇧	*Signal: Trip Command*

df/dt . **ExBlo**	[Operation / Status Display / Intercon-Prot / Mains Decouplg / df/dt]
⇧	*Signal: External Blocking*

df/dt . **Blo by V<**	[Operation / Status Display / Intercon-Prot / Mains Decouplg / df/dt]
⇧	*Signal: Module is blocked by undervoltage.*

df/dt . **Blo TripCmd**	[Operation / Status Display / Intercon-Prot / Mains Decouplg / df/dt]
⇧	*Signal: Trip Command blocked*

df/dt . **ExBlo TripCmd**	[Operation / Status Display / Intercon-Prot / Mains Decouplg / df/dt]
⇧	*Signal: External Blocking of the Trip Command*

9.7 delta phi

Vector surge

9.7.1 delta phi: Device Planning Parameters

delta phi . **Mode**	[Device planning]	
“-”	“-”, use Device planning.	S.3
Frequency Protection Module, general operation mode		

9.7.2 delta phi: Global Parameters

delta phi . **ExBlo1** delta phi . **ExBlo2**	[Protection Para / Global Prot Para / Intercon-Prot / Mains Decouplg / delta phi]	
“-”	“-” . . . Sys . Internal test state 1..n, Assignment List.	P.2
External blocking of the module, if blocking is activated (allowed) within a parameter set and if the state of the assigned signal is true.		

delta phi . **ExBlo TripCmd**	[Protection Para / Global Prot Para / Intercon-Prot / Mains Decouplg / delta phi]	
“-”	“-” . . . Sys . Internal test state 1..n, Assignment List.	P.2
External blocking of the Trip Command of the module/the stage, if blocking is activated (allowed) within a parameter set and if the state of the assigned signal is true.		

9.7.3 delta phi: Setting Group Parameters

delta phi . **Function**	[Protection Para / Set 1...4 / Intercon-Prot / Mains Decouplg / delta phi]	
inactive	inactive, active Mode.	P.2
Permanent activation or deactivation of module/stage.		

delta phi . **ExBlo Fc**	[Protection Para / Set 1...4 / Intercon-Prot / Mains Decouplg / delta phi]	
inactive	inactive, active ↳ active/inactive.	P.2
Activate (allow) or inactivate (disallow) blocking of the module/stage. This parameter is only effective if a signal is assigned to the corresponding global protection parameter. If the signal becomes true, those modules/stages are blocked that are parameterized "ExBlo Fc=active".		

delta phi . **Blo TripCmd**	[Protection Para / Set 1...4 / Intercon-Prot / Mains Decouplg / delta phi]	
inactive	inactive, active ↳ Mode.	P.2
Permanent blocking of the Trip Command of the module/stage.		

delta phi . **ExBlo TripCmd Fc**	[Protection Para / Set 1...4 / Intercon-Prot / Mains Decouplg / delta phi]	
inactive	inactive, active ↳ active/inactive.	P.2
Activate (allow) or inactivate (disallow) blocking of the module/stage. This parameter is only effective if a signal is assigned to the corresponding global protection parameter. If the signal becomes true, those modules/stages are blocked that are parameterized "ExBlo TripCmd Fc=active".		

delta phi . **f>**	[Protection Para / Set 1...4 / Intercon-Prot / Mains Decouplg / delta phi]	
51.00Hz	40.00Hz ... 69.00Hz	P.2
Pickup value for overfrequency.		

delta phi . **f<**	[Protection Para / Set 1...4 / Intercon-Prot / Mains Decouplg / delta phi]	
49.00Hz	40.00Hz ... 69.00Hz	P.2
Pickup value for underfrequency.		

delta phi . **Freq. drop-off**	[Protection Para / Set 1...4 / Intercon-Prot / Mains Decouplg / delta phi]	
0.020Hz	0.010Hz ... 0.100Hz	P.2
Drop-off for the Frequency function. This setting modifies the shape of the hysteresis that is used for the frequency protection.		

delta phi . **t**	[Protection Para / Set 1...4 / Intercon-Prot / Mains Decouplg / delta phi]	
1.00s	0.00s ... 3600.00s	P.2
Tripping delay		

delta phi . **df/dt**	[Protection Para / Set 1...4 / Intercon-Prot / Mains Decouplg / delta phi]	
1.000Hz/s	0.100Hz/s ... 10.000Hz/s	P.2
Measured value (calculated): Rate-of-frequency-change.		

delta phi . **t-df/dt**	[Protection Para / Set 1...4 / Intercon-Prot / Mains Decouplg / delta phi]	
1.00s	0.00s ... 300.00s	P.2
Trip delay df/dt		

delta phi . **DF**	[Protection Para / Set 1...4 / Intercon-Prot / Mains Decouplg / delta phi]	
1.00Hz	0.0Hz ... 10.0Hz	P.2
Frequency difference for the maximum admissible variation of the mean of the rate of frequency-change. This function is inactive if DF=0.		

delta phi . **DT**	[Protection Para / Set 1...4 / Intercon-Prot / Mains Decouplg / delta phi]	
1.00s	0.1s ... 10.0s	P.2
Time interval of the maximum admissible rate-of-frequency-change.		

delta phi . **df/dt mode**	[Protection Para / Set 1...4 / Intercon-Prot / Mains Decouplg / delta phi]	
absolute df/dt	absolute df/dt, positive df/dt, negative df/dt Mode.	P.2
df/dt mode		

delta phi . **delta phi**	[Protection Para / Set 1...4 / Intercon-Prot / Mains Decouplg / delta phi]	
10°	1° ... 30°	P.2
Measured value (calculated): Vector surge		

9.7.4 delta phi: Input States

delta phi . **ExBlo1-I**	[Operation / Status Display / Intercon-Prot / Mains Decouplg / delta phi]
⇩	*Module input state: External blocking1*

delta phi . **ExBlo2-I**	[Operation / Status Display / Intercon-Prot / Mains Decouplg / delta phi]
⇩	*Module input state: External blocking2*

delta phi . **ExBlo TripCmd-I**	[Operation / Status Display / Intercon-Prot / Mains Decouplg / delta phi]
⇩	*Module input state: External Blocking of the Trip Command*

9.7.5 delta phi: Signals (Output States)

delta phi . **active**	[Operation / Status Display / All Actives] [Operation / Status Display / Intercon-Prot / Mains Decouplg / delta phi]
⇧	*Signal: active*

delta phi . **Alarm**	[Operation / Status Display / Alarms] [Operation / Status Display / Intercon-Prot / Mains Decouplg / delta phi]
⇧	*Signal: Alarm Frequency Protection (collective signal)*

delta phi . **Trip**	[Operation / Status Display / Trips] [Operation / Status Display / Intercon-Prot / Mains Decouplg / delta phi]
⇧	*Signal: Trip Frequency Protection (collective signal)*

delta phi . **TripCmd**	[Operation / Status Display / TripCmds] [Operation / Status Display / Intercon-Prot / Mains Decouplg / delta phi]
⇧	*Signal: Trip Command*

delta phi . **ExBlo**	[Operation / Status Display / Intercon-Prot / Mains Decouplg / delta phi]
⇧	*Signal: External Blocking*

delta phi . **Blo by V<**	[Operation / Status Display / Intercon-Prot / Mains Decouplg / delta phi]
⇧	*Signal: Module is blocked by undervoltage.*

delta phi . **Blo TripCmd**	[Operation / Status Display / Intercon-Prot / Mains Decouplg / delta phi]
⇧	*Signal: Trip Command blocked*

delta phi . **ExBlo TripCmd**	[Operation / Status Display / Intercon-Prot / Mains Decouplg / delta phi]
⇧	*Signal: External Blocking of the Trip Command*

9.8 Intertripping

Intertripping

9.8.1 Intertripping: Device Planning Parameters

Intertripping . **Mode**	[Device planning]	
“-”	“-”, use ⮡ Device planning.	S.3
External Protection - Module, general operation mode		

9.8.2 Intertripping: Global Parameters

Intertripping . **ExBlo1** Intertripping . **ExBlo2**	[Protection Para / Global Prot Para / Intercon-Prot / Mains Decouplg / Intertripping]	
“-”	“-” . . . Sys . Internal test state ⮡ 1..n, Assignment List.	P.2
External blocking of the module, if blocking is activated (allowed) within a parameter set and if the state of the assigned signal is true.		

Intertripping . **ExBlo TripCmd**	[Protection Para / Global Prot Para / Intercon-Prot / Mains Decouplg / Intertripping]	
“-”	“-” . . . Sys . Internal test state ⮡ 1..n, Assignment List.	P.2
External blocking of the Trip Command of the module/the stage, if blocking is activated (allowed) within a parameter set and if the state of the assigned signal is true.		

Intertripping . **Alarm**	[Protection Para / Global Prot Para / Intercon-Prot / Mains Decouplg / Intertripping]	
“-”	“-” . . . Sys . Internal test state ⮡ 1..n, Assignment List.	P.2
Assignment for External Alarm		

Intertripping . **Trip**	[Protection Para / Global Prot Para / Intercon-Prot / Mains Decouplg / Intertripping]	
“-”	“-” . . . Sys . Internal test state ↳ 1..n, Assignment List.	P.2
External trip of the CB if the state of the assigned signal is true.		

9.8.3 Intertripping: Setting Group Parameters

Intertripping . **Function**	[Protection Para / Set 1…4 / Intercon-Prot / Mains Decouplg / Intertripping]	
inactive	inactive, active ↳ Mode.	P.2
Permanent activation or deactivation of module/stage.		

Intertripping . **ExBlo Fc**	[Protection Para / Set 1…4 / Intercon-Prot / Mains Decouplg / Intertripping]	
inactive	inactive, active ↳ active/inactive.	P.2
Activate (allow) or inactivate (disallow) blocking of the module/stage. This parameter is only effective if a signal is assigned to the corresponding global protection parameter. If the signal becomes true, those modules/stages are blocked that are parameterized "ExBlo Fc=active".		

Intertripping . **Blo TripCmd**	[Protection Para / Set 1…4 / Intercon-Prot / Mains Decouplg / Intertripping]	
inactive	inactive, active ↳ Mode.	P.2
Permanent blocking of the Trip Command of the module/stage.		

Intertripping . **ExBlo TripCmd Fc**	[Protection Para / Set 1...4 / Intercon-Prot / Mains Decouplg / Intertripping]	
inactive	inactive, active ↳ active/inactive.	P.2
Activate (allow) or inactivate (disallow) blocking of the module/stage. This parameter is only effective if a signal is assigned to the corresponding global protection parameter. If the signal becomes true, those modules/stages are blocked that are parameterized "ExBlo TripCmd Fc=active".		

9.8.4 Intertripping: Input States

Intertripping . **ExBlo1-I**	[Operation / Status Display / Intercon-Prot / Mains Decouplg / Intertripping]
Module input state: External blocking1	

Intertripping . **ExBlo2-I**	[Operation / Status Display / Intercon-Prot / Mains Decouplg / Intertripping]
Module input state: External blocking2	

Intertripping . **ExBlo TripCmd-I**	[Operation / Status Display / Intercon-Prot / Mains Decouplg / Intertripping]
Module input state: External Blocking of the Trip Command	

Intertripping . **Alarm-I**	[Operation / Status Display / Intercon-Prot / Mains Decouplg / Intertripping]
Module input state: Alarm	

Intertripping . **Trip-I**	[Operation / Status Display / Intercon-Prot / Mains Decouplg / Intertripping]
Module input state: Trip	

9.8.5 Intertripping: Signals (Output States)

Intertripping . **active**	[Operation / Status Display / All Actives] [Operation / Status Display / Intercon-Prot / Mains Decouplg / Intertripping]
Signal: active	

Intertripping . **Alarm**	[Operation / Status Display / Alarms] [Operation / Status Display / Intercon-Prot / Mains Decouplg / Intertripping]
⇪	*Signal: Alarm*

Intertripping . **Trip**	[Operation / Status Display / Trips] [Operation / Status Display / Intercon-Prot / Mains Decouplg / Intertripping]
⇪	*Signal: Trip*

Intertripping . **TripCmd**	[Operation / Status Display / TripCmds] [Operation / Status Display / Intercon-Prot / Mains Decouplg / Intertripping]
⇪	*Signal: Trip Command*

Intertripping . **ExBlo**	[Operation / Status Display / Intercon-Prot / Mains Decouplg / Intertripping]
⇪	*Signal: External Blocking*

Intertripping . **Blo TripCmd**	[Operation / Status Display / Intercon-Prot / Mains Decouplg / Intertripping]
⇪	*Signal: Trip Command blocked*

Intertripping . **ExBlo TripCmd**	[Operation / Status Display / Intercon-Prot / Mains Decouplg / Intertripping]
⇪	*Signal: External Blocking of the Trip Command*

9.9 LVRT[1] . . . LVRT[2]

Low Voltage Ride Through

9.9.1 LVRT[1]: Device Planning Parameters

LVRT[1] . **Mode**	[Device planning]	
"-"	"-", use ↳ Device planning.	S.3
general operation mode		

9.9.2 LVRT[1]: Global Parameters

LVRT[1] . **ExBlo1** LVRT[1] . **ExBlo2**	[Protection Para / Global Prot Para / Intercon-Prot / LVRT[1]]	
"-"	"-" . . . Sys . Internal test state ↳ 1..n, Assignment List.	P.2
External blocking of the module, if blocking is activated (allowed) within a parameter set and if the state of the assigned signal is true.		

LVRT[1] . **ExBlo TripCmd**	[Protection Para / Global Prot Para / Intercon-Prot / LVRT[1]]	
"-"	"-" . . . Sys . Internal test state ↳ 1..n, Assignment List.	P.2
External blocking of the Trip Command of the module/the stage, if blocking is activated (allowed) within a parameter set and if the state of the assigned signal is true.		

9.9.3 LVRT[1]: Setting Group Parameters

LVRT[1] . **Function**	[Protection Para / Set 1...4 / Intercon-Prot / LVRT[1] / General Settings]	
inactive	inactive, active ↳ Mode.	P.2
Permanent activation or deactivation of module/stage.		

LVRT[1] . **ExBlo Fc**	[Protection Para / Set 1...4 / Intercon-Prot / LVRT[1] / General Settings]	
inactive	inactive, active ↳ active/inactive.	P.2
	Activate (allow) or inactivate (disallow) blocking of the module/stage. This parameter is only effective if a signal is assigned to the corresponding global protection parameter. If the signal becomes true, those modules/stages are blocked that are parameterized "ExBlo Fc=active".	

LVRT[1] . **Blo TripCmd**	[Protection Para / Set 1...4 / Intercon-Prot / LVRT[1] / General Settings]	
inactive	inactive, active ↳ Mode.	P.2
	Permanent blocking of the Trip Command of the module/stage.	

LVRT[1] . **ExBlo TripCmd Fc**	[Protection Para / Set 1...4 / Intercon-Prot / LVRT[1] / General Settings]	
inactive	inactive, active ↳ active/inactive.	P.2
	Activate (allow) or inactivate (disallow) blocking of the module/stage. This parameter is only effective if a signal is assigned to the corresponding global protection parameter. If the signal becomes true, those modules/stages are blocked that are parameterized "ExBlo TripCmd Fc=active".	

LVRT[1] . **Measuring Mode**	[Protection Para / Set 1...4 / Intercon-Prot / LVRT[1] / General Settings]	
Phase to Ground	Phase to Ground, Phase to Phase ↳ Measuring Mode.	P.2
	Measuring/Supervision Mode: Determines if the phase-to-phase or phase-to-earth voltages are to be supervised	

LVRT[1] . **Measuring method**	[Protection Para / Set 1...4 / Intercon-Prot / LVRT[1] / General Settings]	
Fundamental	Fundamental, True RMS ↳ Measuring method.	P.2
	Measuring method: fundamental or rms or 3rd harmonic (only generator protection relays)	

LVRT[1] . **Alarm Mode**	[Protection Para / Set 1...4 / Intercon-Prot / LVRT[1] / General Settings]	
any one	any one, any two, all, only 2 ↳ Alarm Mode.	P.2
Alarm criterion for the voltage protection stage.		

LVRT[1] . **Meas Circuit Superv**	[Protection Para / Set 1...4 / Intercon-Prot / LVRT[1] / General Settings]	
Sys . inactive	Sys . inactive, VTS . active ↳ VTS Block.	P.2
Activates the use of the measuring circuit supervision. In this case the module will be blocked if a measuring circuit supervision module (e.g. LOP, VTS) signals a disturbed measuring circuit (e.g. caused by a fuse failure).		

LVRT[1] . **AR controlled LVRT**	[Protection Para / Set 1...4 / Intercon-Prot / LVRT[1] / General Settings]	
inactive	inactive, active ↳ active/inactive.	P.2
Activates the supervision of the number of voltage dips during a defined time (t-LVRT).		

LVRT[1] . **Number of V dips to trip**	[Protection Para / Set 1...4 / Intercon-Prot / LVRT[1] / General Settings]	
1 *Only available if:* • LVRT[1] . AR controlled LVRT = active	1 . . . 6	P.2
Number of voltage dips until the disconnection signal (trip) will be issued.		

LVRT[1] . **t-LVRT**	[Protection Para / Set 1...4 / Intercon-Prot / LVRT[1] / General Settings]	
30.00s *Only available if:* • LVRT[1] . AR controlled LVRT = active	0.00s . . . 3000.00s	P.2
This timer defines the supervision interval (window/period) for counting the number of voltage dips to trip (“No of V dips to trip”). The first voltage dip will start the timer. The counted number of voltage dips will be reset if the timer is expired. The timer will also be reset if the maximum “No of V dips to trip” is reached.		

LVRT[1] . **Vstart<**	[Protection Para / Set 1...4 / Intercon-Prot / LVRT[1] / LVRT Profile]	
0.90Vn	0.00Vn . . . 2.00Vn	P.2
A voltage dip is detected if the measured voltage falls below this threshold.		

LVRT[1] . **Vrecover>**	[Protection Para / Set 1...4 / Intercon-Prot / LVRT[1] / LVRT Profile]	
0.93Vn	0.10Vn . . . 2.00Vn	P.2
The voltage is recovered if the measured voltage raises above this threshold.		

LVRT[1] . **V(t1)** LVRT[1] . **V(t2)**	[Protection Para / Set 1...4 / Intercon-Prot / LVRT[1] / LVRT Profile]	
0.00Vn	0.00Vn . . . 2.00Vn	P.2
Voltage value of a point V(t(n)). These points define the LVRT profile.		

LVRT[1] . **t1**	[Protection Para / Set 1...4 / Intercon-Prot / LVRT[1] / LVRT Profile]	
0.00s	0.00s . . . 20.00s	P.2
Point in time for the corresponding voltage value V(t(n)). These points define the LVRT profile.		

LVRT[1] . **t2** LVRT[1] . **t3**	[Protection Para / Set 1...4 / Intercon-Prot / LVRT[1] / LVRT Profile]	
0.15s	0.00s . . . 20.00s	P.2
Point in time for the corresponding voltage value V(t(n)). These points define the LVRT profile.		

LVRT[1] . **V(t3)** LVRT[1] . **V(t4)**	[Protection Para / Set 1...4 / Intercon-Prot / LVRT[1] / LVRT Profile]	
0.70Vn	0.00Vn ... 2.00Vn	P.2
Voltage value of a point V(t(n)). These points define the LVRT profile.		

LVRT[1] . **t4**	[Protection Para / Set 1...4 / Intercon-Prot / LVRT[1] / LVRT Profile]	
0.70s	0.00s ... 20.00s	P.2
Point in time for the corresponding voltage value V(t(n)). These points define the LVRT profile.		

LVRT[1] . **V(t5)** **...** LVRT[1] . **V(t10)**	[Protection Para / Set 1...4 / Intercon-Prot / LVRT[1] / LVRT Profile]	
0.90Vn	0.00Vn ... 2.00Vn	P.2
Voltage value of a point V(t(n)). These points define the LVRT profile.		

LVRT[1] . **t5**	[Protection Para / Set 1...4 / Intercon-Prot / LVRT[1] / LVRT Profile]	
1.50s	0.00s ... 20.00s	P.2
Point in time for the corresponding voltage value V(t(n)). These points define the LVRT profile.		

LVRT[1] . **t6** **...** LVRT[1] . **t10**	[Protection Para / Set 1...4 / Intercon-Prot / LVRT[1] / LVRT Profile]	
3.00s	0.00s ... 20.00s	P.2
Point in time for the corresponding voltage value V(t(n)). These points define the LVRT profile.		

9.9.4 LVRT[1]: Direct Controls

LVRT[1] . **Res LVRT Cr**	[Operation / Reset]	
inactive	inactive, active Mode.	P.1
◉	*Reset of the counter for the total number of voltage dips and reset of the counter of the total number of voltage dips that caused a trip.*	

9.9.5 LVRT[1]: Input States

LVRT[1] . **ExBlo1-I**	[Operation / Status Display / Intercon-Prot / LVRT[1]]
⇩	*Module input state: External blocking1*

LVRT[1] . **ExBlo2-I**	[Operation / Status Display / Intercon-Prot / LVRT[1]]
⇩	*Module input state: External blocking2*

LVRT[1] . **ExBlo TripCmd-I**	[Operation / Status Display / Intercon-Prot / LVRT[1]]
⇩	*Module input state: External Blocking of the Trip Command*

9.9.6 LVRT[1]: Signals (Output States)

LVRT[1] . **active**	[Operation / Status Display / All Actives] [Operation / Status Display / Intercon-Prot / LVRT[1]]
⇧	*Signal: active*

LVRT[1] . **Alarm**	[Operation / Status Display / Alarms] [Operation / Status Display / Intercon-Prot / LVRT[1]]
⇧	*Signal: Alarm voltage stage*

LVRT[1] . **Trip**	[Operation / Status Display / Trips] [Operation / Status Display / Intercon-Prot / LVRT[1]]
⇧	*Signal: Trip*

LVRT[1] . **TripCmd**	[Operation / Status Display / TripCmds] [Operation / Status Display / Intercon-Prot / LVRT[1]]
⇧	*Signal: Trip Command*

LVRT[1] . **ExBlo**	[Operation / Status Display / Intercon-Prot / LVRT[1]]
⇧	*Signal: External Blocking*

LVRT[1] . **Blo TripCmd**	[Operation / Status Display / Intercon-Prot / LVRT[1]]
⇧	*Signal: Trip Command blocked*

LVRT[1] . **ExBlo TripCmd**	[Operation / Status Display / Intercon-Prot / LVRT[1]]
⇧	*Signal: External Blocking of the Trip Command*

LVRT[1] . **Alarm L1**	[Operation / Status Display / Intercon-Prot / LVRT[1]]
⇧	*Signal: Alarm L1*

LVRT[1] . **Alarm L2**	[Operation / Status Display / Intercon-Prot / LVRT[1]]
⇧	*Signal: Alarm L2*

LVRT[1] . **Alarm L3**	[Operation / Status Display / Intercon-Prot / LVRT[1]]
⇧	*Signal: Alarm L3*

LVRT[1] . **Trip L1**	[Operation / Status Display / Intercon-Prot / LVRT[1]]
⇧	*Signal: General Trip Phase L1*

LVRT[1] . **Trip L2**	[Operation / Status Display / Intercon-Prot / LVRT[1]]
⇧	*Signal: General Trip Phase L2*

LVRT[1] . **Trip L3**	[Operation / Status Display / Intercon-Prot / LVRT[1]]
⇧	*Signal: General Trip Phase L3*

LVRT[1] . **t-LVRT is running**	[Operation / Status Display / Intercon-Prot / LVRT[1]]
⇧	*Signal: t-LVRT is running*

9.9.7 LVRT[1]: Counters

LVRT[1] . **NumOf Vdips in t-LVRT**	[Operation / Count and RevData / LVRT[1]]
#	*Number of Voltage dips during t-LVRT*

LVRT[1] . **Cr Tot Numb of Vdips**	[Operation / Count and RevData / LVRT[1]]
#	*Counter Total number of voltage dips.*

LVRT[1] . **Cr Tot Numb of Vdips to Trip**	[Operation / Count and RevData / LVRT[1]]
#	*Counter Total number of voltage dips that caused a Trip.*

9.10 VG[1] . . . VG[2]

Residual voltage-Stage

9.10.1 VG[1]: Device Planning Parameters

VG[1] . **Mode**	[Device planning]	
"-"	"-", V>, V< ↳ Device planning.	S.3
Residual voltage-Stage, general operation mode		

VG[1] . **Superv. only**	[Device planning]	
no	no, yes ↳ yes/no.	S.3
Residual voltage-Stage, if set to "Yes": Restriction of the function to a supervision functionality, i.e. there is no general alarm, no general trip and no trip command.		

9.10.2 VG[1]: Global Parameters

VG[1] . **ExBlo1** VG[1] . **ExBlo2**	[Protection Para / Global Prot Para / V-Prot / VG[1]]	
"-"	"-" . . . Sys . Internal test state ↳ 1..n, Assignment List.	P.2
External blocking of the module, if blocking is activated (allowed) within a parameter set and if the state of the assigned signal is true.		

VG[1] . **ExBlo TripCmd**	[Protection Para / Global Prot Para / V-Prot / VG[1]]	
"-" *Only available if:* • VG[1] . Superv. only = no	"-" . . . Sys . Internal test state ↳ 1..n, Assignment List.	P.2
External blocking of the Trip Command of the module/the stage, if blocking is activated (allowed) within a parameter set and if the state of the assigned signal is true.		

9.10.3 VG[1]: Setting Group Parameters

VG[1] . **Function**	[Protection Para / Set 1...4 / V-Prot / VG[1]]	
inactive	inactive, active ↳ Mode.	P.2
Permanent activation or deactivation of module/stage.		

VG[1] . **ExBlo Fc**	[Protection Para / Set 1...4 / V-Prot / VG[1]]	
inactive	inactive, active ↳ active/inactive.	P.2
Activate (allow) or inactivate (disallow) blocking of the module/stage. This parameter is only effective if a signal is assigned to the corresponding global protection parameter. If the signal becomes true, those modules/stages are blocked that are parameterized "ExBlo Fc=active".		

VG[1] . **Blo TripCmd**	[Protection Para / Set 1...4 / V-Prot / VG[1]]	
inactive *Only available if:* • VG[1] . Superv. only = no	inactive, active ↳ Mode.	P.2
Permanent blocking of the Trip Command of the module/stage.		

VG[1] . **ExBlo TripCmd Fc**	[Protection Para / Set 1...4 / V-Prot / VG[1]]	
inactive *Only available if:* • VG[1] . Superv. only = no	inactive, active ↳ active/inactive.	P.2
Activate (allow) or inactivate (disallow) blocking of the module/stage. This parameter is only effective if a signal is assigned to the corresponding global protection parameter. If the signal becomes true, those modules/stages are blocked that are parameterized "ExBlo TripCmd Fc=active".		

VG[1] . **VX Source**	[Protection Para / Set 1...4 / V-Prot / VG[1]]	
measured	measured, calculated ↳ VX Source.	P.2
Selection if VG is measured or calculated (neutral voltage or residual voltage)		

VG[1] . **Measuring method**	[Protection Para / Set 1...4 / V-Prot / VG[1]]	
Fundamental	Fundamental, True RMS ↳ Measuring method.	P.2
Measuring method: fundamental or rms or 3rd harmonic (only generator protection relays)		

VG[1] . **VG>**	[Protection Para / Set 1...4 / V-Prot / VG[1]]	
1Vn	0.01Vn . . . 2.00Vn	P.2
If the pickup value is exceeded, the module/stage will be started.		

VG[1] . **VG<**	[Protection Para / Set 1...4 / V-Prot / VG[1]]	
0.8Vn	0.01Vn . . . 2.00Vn	P.2
Undervoltage Threshold		

VG[1] . **t**	[Protection Para / Set 1...4 / V-Prot / VG[1]]	
0.00s	0.00s . . . 300.00s	P.2
Tripping delay		

VG[1] . **Meas Circuit Superv**	[Protection Para / Set 1...4 / V-Prot / VG[1]]	
Sys . inactive	Sys . inactive, VTS . active ↳ VTS Block.	P.2
Activates the use of the measuring circuit supervision. In this case the module will be blocked if a measuring circuit supervision module (e.g. LOP, VTS) signals a disturbed measuring circuit (e.g. caused by a fuse failure).		

9.10.4 VG[1]: Input States

VG[1] . **ExBlo1-I**	[Operation / Status Display / V-Prot / VG[1]]
Module input state: External blocking1	

VG[1] . **ExBlo2-I**	[Operation / Status Display / V-Prot / VG[1]]
Module input state: External blocking2	

VG[1] . **ExBlo TripCmd-I**	[Operation / Status Display / V-Prot / VG[1]]
⇩	*Only available if:* • VG[1] . Superv. only = no *Module input state: External Blocking of the Trip Command*

9.10.5 VG[1]: Signals (Output States)

VG[1] . **active**	[Operation / Status Display / All Actives] [Operation / Status Display / V-Prot / VG[1]]
⇧	*Signal: active*

VG[1] . **Alarm**	[Operation / Status Display / Alarms] [Operation / Status Display / V-Prot / VG[1]]
⇧	*Signal: Alarm Residual Voltage Supervision-stage*

VG[1] . **Trip**	[Operation / Status Display / Trips] [Operation / Status Display / V-Prot / VG[1]]
⇧	*Signal: Trip*

VG[1] . **TripCmd**	[Operation / Status Display / TripCmds] [Operation / Status Display / V-Prot / VG[1]]
⇧	*Only available if:* • VG[1] . Superv. only = no *Signal: Trip Command*

VG[1] . **ExBlo**	[Operation / Status Display / V-Prot / VG[1]]
⇧	*Signal: External Blocking*

VG[1] . **Blo TripCmd**	[Operation / Status Display / V-Prot / VG[1]]
⇧	*Only available if:* • VG[1] . Superv. only = no *Signal: Trip Command blocked*

VG[1] . **ExBlo TripCmd**	[Operation / Status Display / V-Prot / VG[1]]
⇫	*Only available if:* • VG[1] . Superv. only = no *Signal: External Blocking of the Trip Command*

9.11 V012[1] . . . V012[6]

Symmetrical Components: Supervision of the Positive Phase Sequence or Negative Phase Sequence

9.11.1 V012[1]: Device Planning Parameters

V012[1] . **Mode**	[Device planning]	
“-”	“-”, V1>, V1<, V2> ⮡ Device planning.	S.3
Unbalance Protection: Supervision of the Voltage System		

9.11.2 V012[1]: Global Parameters

V012[1] . **ExBlo1**	[Protection Para / Global Prot Para / V-Prot / V012[1]]	
“-”	“-” . . . Sys . Internal test state ⮡ 1..n, Assignment List.	P.2
External blocking of the module, if blocking is activated (allowed) within a parameter set and if the state of the assigned signal is true.1		

V012[1] . **ExBlo2**	[Protection Para / Global Prot Para / V-Prot / V012[1]]	
“-”	“-” . . . Sys . Internal test state ⮡ 1..n, Assignment List.	P.2
External blocking of the module, if blocking is activated (allowed) within a parameter set and if the state of the assigned signal is true.2		

V012[1] . **ExBlo TripCmd**	[Protection Para / Global Prot Para / V-Prot / V012[1]]	
“-”	“-” . . . Sys . Internal test state ⮡ 1..n, Assignment List.	P.2
External blocking of the Trip Command of the module/the stage, if blocking is activated (allowed) within a parameter set and if the state of the assigned signal is true.		

9.11.3 V012[1]: Setting Group Parameters

V012[1] . **Function**	[Protection Para / Set 1...4 / V-Prot / V012[1]]	
inactive	inactive, active ↳ Mode.	P.2
Permanent activation or deactivation of module/stage.		

V012[1] . **ExBlo Fc**	[Protection Para / Set 1...4 / V-Prot / V012[1]]	
inactive	inactive, active ↳ active/inactive.	P.2
Activate (allow) or inactivate (disallow) blocking of the module/stage. This parameter is only effective if a signal is assigned to the corresponding global protection parameter. If the signal becomes true, those modules/stages are blocked that are parameterized "ExBlo Fc=active".		

V012[1] . **Blo TripCmd**	[Protection Para / Set 1...4 / V-Prot / V012[1]]	
inactive	inactive, active ↳ Mode.	P.2
Permanent blocking of the Trip Command of the module/stage.		

V012[1] . **ExBlo TripCmd Fc**	[Protection Para / Set 1...4 / V-Prot / V012[1]]	
inactive	inactive, active ↳ active/inactive.	P.2
Activate (allow) or inactivate (disallow) blocking of the module/stage. This parameter is only effective if a signal is assigned to the corresponding global protection parameter. If the signal becomes true, those modules/stages are blocked that are parameterized "ExBlo TripCmd Fc=active".		

V012[1] . **V1>**	[Protection Para / Set 1...4 / V-Prot / V012[1]]	
1.00Vn	0.01Vn . . . 2.00Vn	P.2
Positive Phase Sequence Overvoltage		

V012[1] . **V1<**	[Protection Para / Set 1...4 / V-Prot / V012[1]]	
1.00Vn	0.01Vn . . . 2.00Vn	P.2
Positive Phase Sequence Undervoltage		

V012[1] . **V2>**	[Protection Para / Set 1...4 / V-Prot / V012[1]]	
1.00Vn	0.01Vn . . . 2.00Vn	P.2
Negative Phase Sequence Overvoltage		

V012[1] . **%(V2/V1)**	[Protection Para / Set 1...4 / V-Prot / V012[1]]	
inactive	inactive, active ↳ Mode.	P.2
The %(V2/V1) setting is the unbalance trip pickup setting. It is defined by the ratio of negative sequence voltage to positive sequence voltage (% Unbalance=V2/V1). Phase sequence will be taken into account automatically.		

V012[1] . **%(V2/V1)**	[Protection Para / Set 1...4 / V-Prot / V012[1]]	
20%	2% . . . 40%	P.2
The %(V2/V1) setting is the unbalance trip pickup setting. It is defined by the ratio of negative sequence voltage to positive sequence voltage (% Unbalance=V2/V1). Phase sequence will be taken into account automatically.		

V012[1] . **t**	[Protection Para / Set 1...4 / V-Prot / V012[1]]	
0.00s	0.00s . . . 300.00s	P.2
Tripping delay		

V012[1] . **Meas Circuit Superv**	[Protection Para / Set 1...4 / V-Prot / V012[1]]	
Sys . inactive	Sys . inactive, VTS . active ↳ VTS Block.	P.2
Activates the use of the measuring circuit supervision. In this case the module will be blocked if a measuring circuit supervision module (e.g. LOP, VTS) signals a disturbed measuring circuit (e.g. caused by a fuse failure).		

9.11.4 V012[1]: Input States

V012[1] . **ExBlo1-I**	[Operation / Status Display / V-Prot / V012[1]]
Module input state: External blocking1	

V012[1] . **ExBlo2-I**	[Operation / Status Display / V-Prot / V012[1]]
Module input state: External blocking2	

V012[1] . **ExBlo TripCmd-I**	[Operation / Status Display / V-Prot / V012[1]]
⇩	*Module input state: External Blocking of the Trip Command*

9.11.5 V012[1]: Signals (Output States)

V012[1] . **active**	[Operation / Status Display / All Actives] [Operation / Status Display / V-Prot / V012[1]]
⇧	*Signal: active*

V012[1] . **Alarm**	[Operation / Status Display / Alarms] [Operation / Status Display / V-Prot / V012[1]]
⇧	*Signal: Alarm voltage asymmetry*

V012[1] . **Trip**	[Operation / Status Display / Trips] [Operation / Status Display / V-Prot / V012[1]]
⇧	*Signal: Trip*

V012[1] . **TripCmd**	[Operation / Status Display / TripCmds] [Operation / Status Display / V-Prot / V012[1]]
⇧	*Signal: Trip Command*

V012[1] . **ExBlo**	[Operation / Status Display / V-Prot / V012[1]]
⇧	*Signal: External Blocking*

V012[1] . **Blo TripCmd**	[Operation / Status Display / V-Prot / V012[1]]
⇧	*Signal: Trip Command blocked*

V012[1] . **ExBlo TripCmd**	[Operation / Status Display / V-Prot / V012[1]]
⇧	*Signal: External Blocking of the Trip Command*

9.12 f[1] . . . f[6]

Frequency Protection Module

9.12.1 f[1]: Device Planning Parameters

f[1] . **Mode**	[Device planning]	
f<	"-" . . . delta phi ↳ Device planning.	S.3
Frequency Protection Module, general operation mode		

9.12.2 f[1]: Global Parameters

f[1] . **ExBlo1** f[1] . **ExBlo2**	[Protection Para / Global Prot Para / f-Prot / f[1]]	
"-"	"-" . . . Sys . Internal test state ↳ 1..n, Assignment List.	P.2
External blocking of the module, if blocking is activated (allowed) within a parameter set and if the state of the assigned signal is true.		

f[1] . **ExBlo TripCmd**	[Protection Para / Global Prot Para / f-Prot / f[1]]	
"-"	"-" . . . Sys . Internal test state ↳ 1..n, Assignment List.	P.2
External blocking of the Trip Command of the module/the stage, if blocking is activated (allowed) within a parameter set and if the state of the assigned signal is true.		

9.12.3 f[1]: Setting Group Parameters

f[1] . **Function**	[Protection Para / Set 1...4 / f-Prot / f[1]]	
active	inactive, active ↳ Mode.	P.2
Permanent activation or deactivation of module/stage.		

f[1] . **ExBlo Fc**	[Protection Para / Set 1...4 / f-Prot / f[1]]	
inactive	inactive, active ↳ active/inactive.	P.2
Activate (allow) or inactivate (disallow) blocking of the module/stage. This parameter is only effective if a signal is assigned to the corresponding global protection parameter. If the signal becomes true, those modules/stages are blocked that are parameterized "ExBlo Fc=active".		

f[1] . **Blo TripCmd**	[Protection Para / Set 1...4 / f-Prot / f[1]]	
inactive	inactive, active ↳ Mode.	P.2
Permanent blocking of the Trip Command of the module/stage.		

f[1] . **ExBlo TripCmd Fc**	[Protection Para / Set 1...4 / f-Prot / f[1]]	
inactive	inactive, active ↳ active/inactive.	P.2
Activate (allow) or inactivate (disallow) blocking of the module/stage. This parameter is only effective if a signal is assigned to the corresponding global protection parameter. If the signal becomes true, those modules/stages are blocked that are parameterized "ExBlo TripCmd Fc=active".		

f[1] . **f>**	[Protection Para / Set 1...4 / f-Prot / f[1]]	
51.00Hz	40.00Hz ... 69.00Hz	P.2
Pickup value for overfrequency.		

f[1] . **f<**	[Protection Para / Set 1...4 / f-Prot / f[1]]	
49.00Hz	40.00Hz ... 69.00Hz	P.2
Pickup value for underfrequency.		

f[1] . **Freq. drop-off**	[Protection Para / Set 1...4 / f-Prot / f[1]]	
0.020Hz	0.010Hz ... 0.100Hz	P.2
Drop-off for the Frequency function. This setting modifies the shape of the hysteresis that is used for the frequency protection.		

f[1] . **t**	[Protection Para / Set 1...4 / f-Prot / f[1]]	
1.00s	0.00s ... 3600.00s	P.2
Tripping delay		

f[1] . **df/dt**	[Protection Para / Set 1...4 / f-Prot / f[1]]	
1.000Hz/s	0.100Hz/s ... 10.000Hz/s	P.2
Measured value (calculated): Rate-of-frequency-change.		

f[1] . **t-df/dt**	[Protection Para / Set 1...4 / f-Prot / f[1]]	
1.00s	0.00s ... 300.00s	P.2
Trip delay df/dt		

f[1] . **DF**	[Protection Para / Set 1...4 / f-Prot / f[1]]	
1.00Hz	0.0Hz ... 10.0Hz	P.2
Frequency difference for the maximum admissible variation of the mean of the rate of frequency-change. This function is inactive if DF=0.		

f[1] . **DT**	[Protection Para / Set 1...4 / f-Prot / f[1]]	
1.00s	0.1s ... 10.0s	P.2
Time interval of the maximum admissible rate-of-frequency-change.		

f[1] . **df/dt mode**	[Protection Para / Set 1...4 / f-Prot / f[1]]	
absolute df/dt	absolute df/dt, positive df/dt, negative df/dt Mode.	P.2
df/dt mode		

f[1] . **delta phi**	[Protection Para / Set 1...4 / f-Prot / f[1]]	
10°	1° ... 30°	P.2
Measured value (calculated): Vector surge		

9.12.4 f[1]: Input States

f[1] . **ExBlo1-I**	[Operation / Status Display / f-Prot / f[1]]
Module input state: External blocking1	

f[1] . **ExBlo2-I**	[Operation / Status Display / f-Prot / f[1]]
Module input state: External blocking2	

f[1] . **ExBlo TripCmd-I**	[Operation / Status Display / f-Prot / f[1]]
⇩	*Module input state: External Blocking of the Trip Command*

9.12.5 f[1]: Signals (Output States)

f[1] . **active**	[Operation / Status Display / All Actives] [Operation / Status Display / f-Prot / f[1]]
⇧	*Signal: active*

f[1] . **Alarm**	[Operation / Status Display / Alarms] [Operation / Status Display / f-Prot / f[1]]
⇧	*Signal: Alarm Frequency Protection (collective signal)*

f[1] . **Trip**	[Operation / Status Display / Trips] [Operation / Status Display / f-Prot / f[1]]
⇧	*Signal: Trip Frequency Protection (collective signal)*

f[1] . **TripCmd**	[Operation / Status Display / TripCmds] [Operation / Status Display / f-Prot / f[1]]
⇧	*Signal: Trip Command*

f[1] . **ExBlo**	[Operation / Status Display / f-Prot / f[1]]
⇧	*Signal: External Blocking*

f[1] . **Blo by V<**	[Operation / Status Display / f-Prot / f[1]]
⇧	*Signal: Module is blocked by undervoltage.*

f[1] . **Blo TripCmd**	[Operation / Status Display / f-Prot / f[1]]
⇧	*Signal: Trip Command blocked*

f[1] . **ExBlo TripCmd**	[Operation / Status Display / f-Prot / f[1]]
⇧	*Signal: External Blocking of the Trip Command*

f[1] . **Alarm f**	[Operation / Status Display / f-Prot / f[1]]
⇧	*Signal: Alarm Frequency Protection*

f[1] . **Alarm df/dt | DF/DT**	[Operation / Status Display / f-Prot / f[1]]
⇧	*Alarm instantaneous or average value of the rate-of-frequency-change*

f[1] . **Alarm delta phi**	[Operation / Status Display / f-Prot / f[1]]
⇧	*Signal: Alarm Vector Surge*

f[1] . **Trip f**	[Operation / Status Display / f-Prot / f[1]]
⇧	*Signal: Frequency has exceeded the limit.*

f[1] . **Trip df/dt | DF/DT**	[Operation / Status Display / f-Prot / f[1]]
⇧	*Signal: Trip df/dt or DF/DT*

f[1] . **Trip delta phi**	[Operation / Status Display / f-Prot / f[1]]
⇧	*Signal: Trip Vector Surge*

9.13 ReCon[1] . . . ReCon[2]

Reconnection

9.13.1 ReCon[1]: Device Planning Parameters

ReCon[1] . **Mode**	[Device planning]	
"-"	"-", use ↳ Mode.	S.3
general operation mode		

9.13.2 ReCon[1]: Global Parameters

ReCon[1] . **ExBlo1** ReCon[1] . **ExBlo2**	[Protection Para / Global Prot Para / Intercon-Prot / ReCon[1] / General Settings]	
"-"	"-" . . . Sys . Internal test state ↳ 1..n, Assignment List.	P.2
External blocking of the module, if blocking is activated (allowed) within a parameter set and if the state of the assigned signal is true.		

ReCon[1] . **V Ext Release PCC**	[Protection Para / Global Prot Para / Intercon-Prot / ReCon[1] / General Settings]	
"-"	"-" . . . Sys . Internal test state ↳ 1..n, Assignment List.	P.2
Release Signal by the Point of Common Coupling. The line-to-line voltage is greater than 95% of VN.		

ReCon[1] . **PCC Fuse Fail VT**	[Protection Para / Global Prot Para / Intercon-Prot / ReCon[1] / General Settings]	
"-"	"-" . . . DI Slot X1 . DI 8 ↳ 1..n, Dig Inputs.	P.2
Blocking if the fuse of a voltage transformer has tripped at the PCC.		

ReCon[1] . **reconnected**	[Protection Para / Global Prot Para / Intercon-Prot / ReCon[1] / General Settings]	
“-”	“-” . . . Sys . Internal test state ↳ 1..n, Assignment List.	P.2
This signal indicates the state "reconnected" (mains parallel).		

ReCon[1] . **Decoupling1** **. . .** ReCon[1] . **Decoupling6**	[Protection Para / Global Prot Para / Intercon-Prot / ReCon[1] / Decoupling]	
“-”	“-” . . . Logics . LE80.Out inverted ↳ Decoupling Functions.	P.2
Decoupling function, that blocks the reconnection.		

9.13.3 ReCon[1]: Setting Group Parameters

ReCon[1] . **Function**	[Protection Para / Set 1...4 / Intercon-Prot / ReCon[1] / General Settings]	
inactive	inactive, active ↳ Mode.	P.2
Permanent activation or deactivation of module/stage.		

ReCon[1] . **ExBlo Fc**	[Protection Para / Set 1...4 / Intercon-Prot / ReCon[1] / General Settings]	
inactive	inactive, active ↳ active/inactive.	P.2
Activate (allow) or inactivate (disallow) blocking of the module/stage. This parameter is only effective if a signal is assigned to the corresponding global protection parameter. If the signal becomes true, those modules/stages are blocked that are parameterized "ExBlo Fc=active".		

ReCon[1] . **Meas Circuit Superv**	[Protection Para / Set 1...4 / Intercon-Prot / ReCon[1] / General Settings]	
Sys . inactive	Sys . inactive, VTS . active ↳ VTS Block.	P.2
Activates the use of the measuring circuit supervision. In this case the module will be blocked if a measuring circuit supervision module (e.g. LOP, VTS) signals a disturbed measuring circuit (e.g. caused by a fuse failure).		

ReCon[1] . **V Ext Release PCC Fc**	[Protection Para / Set 1...4 / Intercon-Prot / ReCon[1] / General Settings]	
inactive	inactive, active ↳ Mode.	P.2
Activate the release signal of the Point of Common Coupling. The line-to-line voltage is greater than 95% of VN.		

ReCon[1] . **Reconnect. Release Cond**	[Protection Para / Set 1...4 / Intercon-Prot / ReCon[1] / Release Para]	
Both	V Internal Release, V Ext Release PCC, Both ↳ Reconnect. Release Cond.	P.2
This parameter ensures that the mains voltage is recovered.		

ReCon[1] . **PCC Fuse Fail VT Fk**	[Protection Para / Set 1...4 / Intercon-Prot / ReCon[1] / Release Para]	
inactive *Only available if:* • ReCon[1] . Reconnect. Release Cond = V Ext Release PCC • ReCon[1] . Reconnect. Release Cond = Both	inactive, active ↳ Mode.	P.2
Blocking if the fuse of a voltage transformer has tripped at the PCC.		

ReCon[1] . **Measuring method**	[Protection Para / Set 1...4 / Intercon-Prot / ReCon[1] / Release Para]	
Fundamental	Fundamental, True RMS, Vavg ↳ Measuring method.	P.2
Measuring method: fundamental or rms or "sliding average supervision"		

ReCon[1] . **VLL< Release**	[Protection Para / Set 1...4 / Intercon-Prot / ReCon[1] / Release Para]	
1.10Vn *Only available if:* • ReCon[1] . Reconnect. Release Cond = V Internal Release • ReCon[1] . Reconnect. Release Cond = Both	1.00Vn ... 1.50Vn	P.2
Maximum voltage (line-to-line) for reclosure (Restoration Voltage)		

ReCon[1] . **VLL> Release**	[Protection Para / Set 1...4 / Intercon-Prot / ReCon[1] / Release Para]	
0.95Vn *Only available if:* • ReCon[1] . Reconnect. Release Cond = V Internal Release • ReCon[1] . Reconnect. Release Cond = Both	0.70Vn ... 1.00Vn	P.2
Minimum voltage (line-to-line) for reclosure (Restoration Voltage)		

ReCon[1] . **f>**	[Protection Para / Set 1...4 / Intercon-Prot / ReCon[1] / Release Para]	
50.05Hz	40.00Hz ... 69.90Hz	P.2
Upper frequency limit for the reclosure		

ReCon[1] . **f<**	[Protection Para / Set 1...4 / Intercon-Prot / ReCon[1] / Release Para]	
47.5Hz	40.00Hz ... 69.90Hz	P.2
Lower frequency limit for the reclosure (Restoration Voltage)		

ReCon[1] . **t-Release Blo**	[Protection Para / Set 1...4 / Intercon-Prot / ReCon[1] / Release Para]	
600s	0.00s ... 3600.00s	P.2
Time stage (delay) for the reclosure of the energy resources. The Mains seddle time takes based on exirience approx. 10 - 15 minutes.		

9.13.4 ReCon[1]: Input States

ReCon[1] . **ExBlo1-I**	[Operation / Status Display / Intercon-Prot / ReCon[1]]
⇩	*Module input state: External blocking1*

ReCon[1] . **ExBlo2-I**	[Operation / Status Display / Intercon-Prot / ReCon[1]]
⇩	*Module input state: External blocking2*

ReCon[1] . **V Ext Release PCC-I**	[Operation / Status Display / Intercon-Prot / ReCon[1]]
⇩	*Module input state: Release signal is being generated by the PCC (External Release)*

ReCon[1] . **PCC Fuse Fail VT-I**	[Operation / Status Display / Intercon-Prot / ReCon[1]]
⇩	*State of the module input: Blocking if the fuse of a voltage transformer has tripped at the PCC.*

ReCon[1] . **reconnected-I**	[Operation / Status Display / Intercon-Prot / ReCon[1]]
⇩	*This signal indicates the state "reconnected" (mains parallel).*

ReCon[1] . **Decoupling1-I** **. . .** ReCon[1] . **Decoupling6-I**	[Operation / Status Display / Intercon-Prot / ReCon[1]]
⇩	*Decoupling function, that blocks the reconnection.*

9.13.5 ReCon[1]: Signals (Output States)

ReCon[1] . **active**	[Operation / Status Display / All Actives] [Operation / Status Display / Intercon-Prot / ReCon[1]]
⇧	*Signal: active*

ReCon[1] . **ExBlo**	[Operation / Status Display / Intercon-Prot / ReCon[1]]
⇧	*Signal: External Blocking*

ReCon[1] . **Blo by Meas Ciruit Superv**	[Operation / Status Display / Intercon-Prot / ReCon[1]]
⇧	*Signal: Module blocked by measuring cirucuit supervision*

ReCon[1] . **Release Energy Resource**	[Operation / Status Display / Intercon-Prot / ReCon[1]]
⇧	*Signal: Release Energy Resource.*

9.14 Sync

Synchrocheck

9.14.1 Sync: Device Planning Parameters

Sync . **Mode**	[Device planning]	
“-”	“-”, use ↳ Mode.	S.3
Synchrocheck, general operation mode		

9.14.2 Sync: Global Parameters

Sync . **ExBlo1** Sync . **ExBlo2**	[Protection Para / Global Prot Para / Intercon-Prot / Sync]	
“-”	“-” . . . Sys . Internal test state ↳ 1..n, Assignment List.	C.2
External blocking of the module, if blocking is activated (allowed) within a parameter set and if the state of the assigned signal is true.		

Sync . **Bypass**	[Protection Para / Global Prot Para / Intercon-Prot / Sync]	
“-”	“-” . . . Logics . LE80.Out inverted ↳ 1..n, DI-LogicList.	C.2
The Synchrocheck will be bypassed if the state of the assigned signal (logic input) becomes true.		

Sync . **CB Pos Detect**	[Protection Para / Global Prot Para / Intercon-Prot / Sync]	
SG[1] . Pos	“-”, SG[1] . Pos ↳ CB Manager.	C.2
Criterion by which the Circuit Breaker Switch Position is to be detected.		

Sync . **CBCloseInitiate**	[Protection Para / Global Prot Para / Intercon-Prot / Sync]	
"-"	"-" . . . Logics . LE80.Out inverted ↳ 1..n, SyncRequestList.	C.2
Breaker Close Initiate with synchronism check from any control sources (e.g. HMI / SCADA). If the state of the assigned signal becomes true, a Breaker Close will be initiated (Trigger Source).		

9.14.3 Sync: Setting Group Parameters

Sync . **Function**	[Protection Para / Set 1...4 / Intercon-Prot / Sync / General Settings]	
inactive	inactive, active ↳ Mode.	P.2
Permanent activation or deactivation of module/stage.		

Sync . **ExBlo Fc**	[Protection Para / Set 1...4 / Intercon-Prot / Sync / General Settings]	
inactive	inactive, active ↳ active/inactive.	P.2
Activate (allow) or inactivate (disallow) blocking of the module/stage. This parameter is only effective if a signal is assigned to the corresponding global protection parameter. If the signal becomes true, those modules/stages are blocked that are parameterized "ExBlo Fc=active".		

Sync . **Bypass Fc**	[Protection Para / Set 1...4 / Intercon-Prot / Sync / General Settings]	
inactive	inactive, active ↳ active/inactive.	P.2
Allowing to bypass the Synchrocheck, if the state signal that is assigned to the parameter with the same name within the Global Parameters (logic input) becomes true.		

Sync . **SyncMode**	[Protection Para / Set 1...4 / Intercon-Prot / Sync / Mode / Times]	
System2System	System2System, Generator2System ↳ SyncMode.	P.2
Synchrocheck mode: GENERATOR2SYSTEM = Synchronizing generator to system (breaker close initiate needed). SYSTEM2SYSTEM = SynchronCheck between two systems (Stand-Alone, no breaker info needed)		

Sync . **t-MaxCBCloseDelay**	[Protection Para / Set 1...4 / Intercon-Prot / Sync / Mode / Times]	
0.05s *Only available if:* • Sync . SyncMode = Generator2System	0.00s ... 300.00s	P.2
Maximum circuit breaker close time delay (Only used for GENERATOR-SYSTEM working mode and is critical for a correct synchronized switching)		

Sync . **t-MaxSyncSuperv**	[Protection Para / Set 1...4 / Intercon-Prot / Sync / Mode / Times]	
30.00s *Only available if:* • Sync . SyncMode = Generator2System	0.00s ... 3000.00s	P.2
Synchron-Run timer: Max. time allowed for synchronizing process after a close initiate. Only used for GENERATOR2SYSTEM working mode.		

Sync . **MinLiveBusVoltage**	[Protection Para / Set 1...4 / Intercon-Prot / Sync / DeadLiveVLevels]	
0.65Vn	0.10Vn ... 2.00Vn	P.2
Minimum Live Bus voltage (Live bus detected, when all three phase bus voltages are above this limit).		

Sync . **MaxDeadBusVoltage**	[Protection Para / Set 1...4 / Intercon-Prot / Sync / DeadLiveVLevels]	
0.03Vn	0.01Vn ... 1.00Vn	P.2
Maximum Dead Bus voltage (Dead bus detected, when all three phase bus voltages are below this limit).		

Sync . **MinLiveLineVoltage**	[Protection Para / Set 1...4 / Intercon-Prot / Sync / DeadLiveVLevels]	
0.65Vn	0.10Vn ... 2.00Vn	P.2
Minimum Live Line voltage (Live line detected, when line voltage above this limit).		

Sync . **MaxDeadLineVoltage**	[Protection Para / Set 1...4 / Intercon-Prot / Sync / DeadLiveVLevels]	
0.03Vn	0.01Vn ... 1.00Vn	P.2
Maximum Dead Line voltage (Dead Line detected, when line voltage below this limit).		

Sync . **t-VoltDead**	[Protection Para / Set 1...4 / Intercon-Prot / Sync / DeadLiveVLevels]	
0.167s	0.000s ... 300.000s	P.2
Voltage dead time (A Dead Bus/Line condition will be accepted only if the voltage falls below the set dead voltage levels longer than this time setting).		

Sync . **MaxVoltageDiff**	[Protection Para / Set 1...4 / Intercon-Prot / Sync / Conditions]	
0.24Vn	0.01Vn ... 1.00Vn	P.2
Maximum voltage difference between bus and line voltage phasors (Delta V)for synchronism (Related to bus voltage secondary rating)		

Sync . **MaxSlipFrequency**	[Protection Para / Set 1...4 / Intercon-Prot / Sync / Conditions]	
0.20Hz	0.01Hz ... 2.00Hz	P.2
Maximum frequency difference (Slip: Delta f) between bus and line voltage allowed for synchronism		

Sync . **MaxAngleDiff**	[Protection Para / Set 1...4 / Intercon-Prot / Sync / Conditions]	
20°	1° ... 60°	P.2
Maximum phase angle difference (Delta-Phi in degree) between bus and line voltages allowed for synchronism		

Sync . **DBDL**	[Protection Para / Set 1...4 / Intercon-Prot / Sync / Override]	
inactive	inactive, active ↳ active/inactive.	P.2
Enable/disable Dead-Bus AND Dead-Line synchronism overriding		

Sync . **DBLL**	[Protection Para / Set 1...4 / Intercon-Prot / Sync / Override]	
inactive	inactive, active ↳ active/inactive.	P.2
Enable/disable Dead-Bus AND Live-Line synchronism overriding		

Sync . **LBDL**	[Protection Para / Set 1...4 / Intercon-Prot / Sync / Override]	
inactive	inactive, active ⇒ active/inactive.	P.2
Enable/disable Live-Bus AND Dead-Line synchronism overriding		

9.14.4 Sync: Input States

Sync . **ExBlo1-I**	[Operation / Status Display / Intercon-Prot / Sync]
Module input state: External blocking1	

Sync . **ExBlo2-I**	[Operation / Status Display / Intercon-Prot / Sync]
Module input state: External blocking2	

Sync . **Bypass-I**	[Operation / Status Display / Intercon-Prot / Sync]
State of the module input: The Synchrocheck will be bypassed if the state of the assigned signal (logic input) becomes true.	

Sync . **CBCloseInitiate-I**	[Operation / Status Display / Intercon-Prot / Sync]
State of the module input: Breaker Close Initiate with synchronism check from any control sources (e.g. HMI / SCADA). If the state of the assigned signal becomes true, a Breaker Close will be initiated (Trigger Source).	

9.14.5 Sync: Signals (Output States)

Sync . **active**	[Operation / Status Display / All Actives] [Operation / Status Display / Intercon-Prot / Sync]
Signal: active	

Sync . **ExBlo**	[Operation / Status Display / Intercon-Prot / Sync]
Signal: External Blocking	

Sync . **LiveBus**	[Operation / Status Display / Intercon-Prot / Sync]
Signal: Live-Bus flag: 1=Live-Bus, 0=Voltage is below the LiveBus threshold	

Sync . **LiveLine**	[Operation / Status Display / Intercon-Prot / Sync]
⇧	*Signal: Live Line flag: 1=Live-Line, 0=Voltage is below the LiveLine threshold*

Sync . **SynchronRunTiming**	[Operation / Status Display / Intercon-Prot / Sync]
⇧	*Signal: Synchron-Run-timer is timing (This timer starts when Close-Initiate is coming and stops if breaker is closed. Timeout means synchronizing failed.)*

Sync . **SynchronFailed**	[Operation / Status Display / Intercon-Prot / Sync]
⇧	*Signal: This signal indicates a failed synchronization. It is set for 5s when the circuit breaker is still open after the Synchron-Run-timer has timed out.*

Sync . **SyncOverridden**	[Operation / Status Display / Intercon-Prot / Sync]
⇧	*Signal:Synchronism Check is overridden because one of the Synchronism overriding conditions (DB/DL or ExtBypass) is met.*

Sync . **VDiffTooHigh**	[Operation / Status Display / Intercon-Prot / Sync]
⇧	*Signal: Voltage difference between bus and line too high.*

Sync . **SlipTooHigh**	[Operation / Status Display / Intercon-Prot / Sync]
⇧	*Signal: Frequency difference (slip frequency) between bus and line voltages too high.*

Sync . **AngleDiffTooHigh**	[Operation / Status Display / Intercon-Prot / Sync]
⇧	*Signal: Phase Angle difference between bus and line voltages too high.*

Sync . **Sys-in-Sync**	[Operation / Status Display / Intercon-Prot / Sync]
⇧	*Signal: Bus and line voltages are in synchronism according to the system synchronism criteria.*

Sync . **Ready to Close**	[Operation / Status Display / Intercon-Prot / Sync]
⇧	*Signal: Ready to Close*

9.14.6 Sync: Values

Sync . **Slip Freq**	[Operation / Measured Values / Synchronism]
⇘	*Slip frequency*

Sync . **Volt Diff**	[Operation / Measured Values / Synchronism]
⇘	*Voltage difference between bus and line.*

Sync . **Angle Diff**	[Operation / Measured Values / Synchronism]
⟍	*Angle difference between bus and line voltages.*

Sync . **f Bus**	[Operation / Measured Values / Synchronism]
⟍	*Bus frequency*

Sync . **f Line**	[Operation / Measured Values / Synchronism]
⟍	*Line frequency*

Sync . **V Bus**	[Operation / Measured Values / Synchronism]
⟍	*Bus Voltage*

Sync . **V Line**	[Operation / Measured Values / Synchronism]
⟍	*Line Voltage*

Sync . **Angle Bus**	[Operation / Measured Values / Synchronism]
⟍	*Bus Angle (Reference)*

Sync . **Angle Line**	[Operation / Measured Values / Synchronism]
⟍	*Line Angle*

9.15 ExP[1] . . . ExP[4]

External Protection - Module

9.15.1 ExP[1]: Device Planning Parameters

ExP[1] . **Mode**	[Device planning]	
"-"	"-", use ↳ Device planning.	S.3
External Protection - Module, general operation mode		

9.15.2 ExP[1]: Global Parameters

ExP[1] . **ExBlo1** ExP[1] . **ExBlo2**	[Protection Para / Global Prot Para / ExP / ExP[1]]	
"-"	"-" . . . Sys . Internal test state ↳ 1..n, Assignment List.	P.2
External blocking of the module, if blocking is activated (allowed) within a parameter set and if the state of the assigned signal is true.		

ExP[1] . **ExBlo TripCmd**	[Protection Para / Global Prot Para / ExP / ExP[1]]	
"-"	"-" . . . Sys . Internal test state ↳ 1..n, Assignment List.	P.2
External blocking of the Trip Command of the module/the stage, if blocking is activated (allowed) within a parameter set and if the state of the assigned signal is true.		

ExP[1] . **Alarm**	[Protection Para / Global Prot Para / ExP / ExP[1]]	
"-"	"-" . . . Sys . Internal test state ↳ 1..n, Assignment List.	P.2
Assignment for External Alarm		

ExP[1] . **Trip**	[Protection Para / Global Prot Para / ExP / ExP[1]]	
"-"	"-" ... Sys . Internal test state ↳ 1..n, Assignment List.	P.2
External trip of the CB if the state of the assigned signal is true.		

9.15.3 ExP[1]: Setting Group Parameters

ExP[1] . **Function**	[Protection Para / Set 1...4 / ExP / ExP[1]]	
inactive	inactive, active ↳ Mode.	P.2
Permanent activation or deactivation of module/stage.		

ExP[1] . **ExBlo Fc**	[Protection Para / Set 1...4 / ExP / ExP[1]]	
inactive	inactive, active ↳ active/inactive.	P.2
Activate (allow) or inactivate (disallow) blocking of the module/stage. This parameter is only effective if a signal is assigned to the corresponding global protection parameter. If the signal becomes true, those modules/stages are blocked that are parameterized "ExBlo Fc=active".		

ExP[1] . **Blo TripCmd**	[Protection Para / Set 1...4 / ExP / ExP[1]]	
inactive	inactive, active ↳ Mode.	P.2
Permanent blocking of the Trip Command of the module/stage.		

ExP[1] . **ExBlo TripCmd Fc**	[Protection Para / Set 1...4 / ExP / ExP[1]]	
inactive	inactive, active ↳ active/inactive.	P.2
Activate (allow) or inactivate (disallow) blocking of the module/stage. This parameter is only effective if a signal is assigned to the corresponding global protection parameter. If the signal becomes true, those modules/stages are blocked that are parameterized "ExBlo TripCmd Fc=active".		

9.15.4 ExP[1]: Input States

ExP[1] . **ExBlo1-I**	[Operation / Status Display / ExP / ExP[1]]
⇩	*Module input state: External blocking1*

ExP[1] . **ExBlo2-I**	[Operation / Status Display / ExP / ExP[1]]
⇩	*Module input state: External blocking2*

ExP[1] . **ExBlo TripCmd-I**	[Operation / Status Display / ExP / ExP[1]]
⇩	*Module input state: External Blocking of the Trip Command*

ExP[1] . **Alarm-I**	[Operation / Status Display / ExP / ExP[1]]
⇩	*Module input state: Alarm*

ExP[1] . **Trip-I**	[Operation / Status Display / ExP / ExP[1]]
⇩	*Module input state: Trip*

9.15.5 ExP[1]: Signals (Output States)

ExP[1] . **active**	[Operation / Status Display / All Actives] [Operation / Status Display / ExP / ExP[1]]
⇧	*Signal: active*

ExP[1] . **Alarm**	[Operation / Status Display / Alarms] [Operation / Status Display / ExP / ExP[1]]
⇧	*Signal: Alarm*

ExP[1] . **Trip**	[Operation / Status Display / Trips] [Operation / Status Display / ExP / ExP[1]]
⇧	*Signal: Trip*

ExP[1] . **TripCmd**	[Operation / Status Display / TripCmds] [Operation / Status Display / ExP / ExP[1]]
⇧	*Signal: Trip Command*

ExP[1] . **ExBlo**	[Operation / Status Display / ExP / ExP[1]]
⇪	*Signal: External Blocking*

ExP[1] . **Blo TripCmd**	[Operation / Status Display / ExP / ExP[1]]
⇪	*Signal: Trip Command blocked*

ExP[1] . **ExBlo TripCmd**	[Operation / Status Display / ExP / ExP[1]]
⇪	*Signal: External Blocking of the Trip Command*

9.16 Supervision

9.16.1 CBF

Circuit breaker failure protection module

9.16.1.1 CBF: Device Planning Parameters

CBF . **Mode**	[Device planning]	
“-”	“-”, use ↳ Device planning.	S.3
Module Circuit Breaker Failure protection, general operation mode		

9.16.1.2 CBF: Global Parameters

CBF . **ExBlo1** CBF . **ExBlo2**	[Protection Para / Global Prot Para / Supervision / CBF]	
“-”	“-” . . . Sys . Internal test state ↳ 1..n, Assignment List.	P.2
External blocking of the module, if blocking is activated (allowed) within a parameter set and if the state of the assigned signal is true.		

CBF . **Trigger**	[Protection Para / Global Prot Para / Supervision / CBF]	
All Trips	- . -, All Trips, External Trips ↳ Trigger.	P.2
Determining the trigger mode for the Breaker Failure.		

CBF . **Trigger1** CBF . **Trigger2** CBF . **Trigger3**	[Protection Para / Global Prot Para / Supervision / CBF]	
“-”	“-” . . . Logics . LE80.Out inverted ↳ Trigger.	P.2
Trigger that will start the CBF		

9.16.1.3 CBF: Setting Group Parameters

CBF . **Function**	[Protection Para / Set 1...4 / Supervision / CBF]	
inactive	inactive, active ↳ Mode.	P.2
Permanent activation or deactivation of module/stage.		

CBF . **ExBlo Fc**	[Protection Para / Set 1...4 / Supervision / CBF]	
inactive	inactive, active ↳ active/inactive.	P.2
Activate (allow) or inactivate (disallow) blocking of the module/stage. This parameter is only effective if a signal is assigned to the corresponding global protection parameter. If the signal becomes true, those modules/stages are blocked that are parameterized "ExBlo Fc=active".		

CBF . **t-CBF**	[Protection Para / Set 1...4 / Supervision / CBF]	
0.20s	0.00s ... 10.00s	P.2
If the delay time is expired, an CBF alarm is given out.		

9.16.1.4 CBF: Direct Controls

CBF . **Res Lockout**	[Operation / Reset]	
inactive	inactive, active ↳ Mode.	P.1
Reset Lockout		

9.16.1.5 CBF: Input States

CBF . **ExBlo1-I**	[Operation / Status Display / Supervision / CBF]
Module input state: External blocking1	

CBF . **ExBlo2-I**	[Operation / Status Display / Supervision / CBF]
Module input state: External blocking2	

CBF . **Trigger1-I** CBF . **Trigger2-I** CBF . **Trigger3-I**	[Operation / Status Display / Supervision / CBF]
⇩	*Module Input: Trigger that will start the CBF*

9.16.1.6 CBF: Signals (Output States)

CBF . **active**	[Operation / Status Display / All Actives] [Operation / Status Display / Supervision / CBF]
⇧	*Signal: active*

CBF . **Alarm**	[Operation / Status Display / Alarms] [Operation / Status Display / Supervision / CBF]
⇧	*Signal: Circuit Breaker Failure*

CBF . **ExBlo**	[Operation / Status Display / Supervision / CBF]
⇧	*Signal: External Blocking*

CBF . **Waiting for Trigger**	[Operation / Status Display / Supervision / CBF]
⇧	*Waiting for Trigger*

CBF . **running**	[Operation / Status Display / Supervision / CBF]
⇧	*Signal: CBF-Module started*

CBF . **Lockout**	[Operation / Status Display / Supervision / CBF]
⇧	*Signal: Lockout*

CBF . **Res Lockout**	[Operation / Status Display / Supervision / CBF]
⇧	*Signal: Reset Lockout*

9.16.2 TCS

Trip circuit supervision

9.16.2.1 TCS: Device Planning Parameters

TCS . **Mode**	[Device planning]	
“-”	“-”, use ↳ Device planning.	S.3
Trip circuit supervision, general operation mode		

9.16.2.2 TCS: Global Parameters

TCS . **Mode**	[Protection Para / Global Prot Para / Supervision / TCS]	
Closed	Closed, Either ↳ Mode.	P.2
Select if trip circuit is going to be monitored when the breaker is closed or when the breaker is either open or close.		

TCS . **Input 1**	[Protection Para / Global Prot Para / Supervision / TCS]	
“-”	“-” . . . DI Slot X1 . DI 8 ↳ 1..n, Dig Inputs.	P.2
Select the input configured to monitor the trip coil when the breaker is closed.		

TCS . **Input 2**	[Protection Para / Global Prot Para / Supervision / TCS]	
“-” *Only available if:* • TCS . Mode = Either	“-” . . . DI Slot X1 . DI 8 ↳ 1..n, Dig Inputs.	P.2
Select the input configured to monitor the trip coil when the breaker is open. Only available if Mode set to “Either”.		

TCS . **ExBlo1** TCS . **ExBlo2**	[Protection Para / Global Prot Para / Supervision / TCS]	
“-”	“-” . . . Sys . Internal test state 1..n, Assignment List.	P.2
External blocking of the module, if blocking is activated (allowed) within a parameter set and if the state of the assigned signal is true.		

9.16.2.3 TCS: Setting Group Parameters

TCS . **Function**	[Protection Para / Set 1...4 / Supervision / TCS]	
inactive	inactive, active Mode.	P.2
Permanent activation or deactivation of module/stage.		

TCS . **ExBlo Fc**	[Protection Para / Set 1...4 / Supervision / TCS]	
inactive	inactive, active active/inactive.	P.2
Activate (allow) or inactivate (disallow) blocking of the module/stage. This parameter is only effective if a signal is assigned to the corresponding global protection parameter. If the signal becomes true, those modules/stages are blocked that are parameterized "ExBlo Fc=active".		

TCS . **t-TCS**	[Protection Para / Set 1...4 / Supervision / TCS]	
0.2s	0.10s . . . 10.00s	P.2
Delay time of the Trip Circuit Supervision		

9.16.2.4 TCS: Input States

TCS . **Aux ON-I**	[Operation / Status Display / Supervision / TCS]
Module Input State: Position indicator/check-back signal of the CB (52a)	

TCS . **Aux OFF-I**	[Operation / Status Display / Supervision / TCS]
Module input state: Position indicator/check-back signal of the CB (52b)	

TCS . **ExBlo1-I**	[Operation / Status Display / Supervision / TCS]
⇩	*Module input state: External blocking1*

TCS . **ExBlo2-I**	[Operation / Status Display / Supervision / TCS]
⇩	*Module input state: External blocking2*

9.16.2.5 TCS: Signals (Output States)

TCS . **active**	[Operation / Status Display / All Actives] [Operation / Status Display / Supervision / TCS]
⇧	*Signal: active*

TCS . **Alarm**	[Operation / Status Display / Alarms] [Operation / Status Display / Supervision / TCS]
⇧	*Signal: Alarm Trip Circuit Supervision*

TCS . **ExBlo**	[Operation / Status Display / Supervision / TCS]
⇧	*Signal: External Blocking*

TCS . **Not Possible**	[Operation / Status Display / Supervision / TCS]
⇧	*Not possible because no state indicator assigned to the breaker.*

9.16.3 VTS

Voltage transformer supervision

9.16.3.1 VTS: Device Planning Parameters

VTS . **Mode**	[Device planning]	
“-”	“-”, use Device planning.	S.3
Voltage transformer supervision, general operation mode		

9.16.3.2 VTS: Global Parameters

VTS . **ExBlo1** VTS . **ExBlo2**	[Protection Para / Global Prot Para / Supervision / VTS]	
“-”	“-” . . . Sys . Internal test state 1..n, Assignment List.	P.2
External blocking of the module, if blocking is activated (allowed) within a parameter set and if the state of the assigned signal is true.		

VTS . **Ex FF VT-I**	[Protection Para / Global Prot Para / Supervision / VTS]	
“-”	“-” . . . Sys . Internal test state 1..n, Assignment List.	P.2
State of the module input: Alarm Fuse Failure Voltage Transformers		

VTS . **Ex FF EVT-I**	[Protection Para / Global Prot Para / Supervision / VTS]	
“-”	“-” . . . Sys . Internal test state 1..n, Assignment List.	P.2
State of the module input: Alarm Fuse Failure Earth Voltage Transformers		

9.16.3.3 VTS: Setting Group Parameters

VTS . **Function**	[Protection Para / Set 1...4 / Supervision / VTS]	
inactive	inactive, active Mode.	P.2
Permanent activation or deactivation of module/stage.		

VTS . **ExBlo Fc**	[Protection Para / Set 1...4 / Supervision / VTS]	
inactive	inactive, active active/inactive.	P.2
Activate (allow) or inactivate (disallow) blocking of the module/stage. This parameter is only effective if a signal is assigned to the corresponding global protection parameter. If the signal becomes true, those modules/stages are blocked that are parameterized "ExBlo Fc=active".		

VTS . **▲V**	[Protection Para / Set 1...4 / Supervision / VTS]	
0.50Vn	0.20Vn ... 1.00Vn	P.2
In order to prevent faulty tripping of phase selective protection functions that use the voltage as tripping criterion. If the difference of the residual voltage and the calculated value V0 is higher than the pick up value ΔV, an alarm event effected after the excitation time. In such a case, the existence of a fuse failure, a broken wire or a faulty measuring circuit can be assumed.		

VTS . **Alarm delay**	[Protection Para / Set 1...4 / Supervision / VTS]	
1.0s	0.0s ... 9999.0s	P.2
Alarm delay		

9.16.3.4 VTS: Input States

VTS . **Ex Fuse Fail VT-I**	[Operation / Status Display / Supervision / VTS]
Module input state: External fuse failure voltage transformers	

VTS . **Ex Fuse Fail EVT-I**	[Operation / Status Display / Supervision / VTS]
Module input state: External fuse failure earth voltage transformer	

VTS . **ExBlo1-I**	[Operation / Status Display / Supervision / VTS]
Module input state: External blocking1	

VTS . **ExBlo2-I**	[Operation / Status Display / Supervision / VTS]
⇩	*Module input state: External blocking2*

9.16.3.5 VTS: Signals (Output States)

VTS . **active**	[Operation / Status Display / All Actives] [Operation / Status Display / Supervision / VTS]
⇧	*Signal: active*

VTS . **Alarm**	[Operation / Status Display / Alarms] [Operation / Status Display / Supervision / VTS]
⇧	*Signal: Alarm Voltage Transformer Measuring Circuit Supervision*

VTS . **ExBlo**	[Operation / Status Display / Supervision / VTS]
⇧	*Signal: External Blocking*

VTS . **Alarm ΔV**	[Operation / Status Display / Supervision / VTS]
⇧	*Signal: Alarm ΔV Voltage Transformer Measuring Circuit Supervision*

VTS . **Ex FF VT**	[Operation / Status Display / Supervision / VTS]
⇧	*Signal: Ex FF VT*

VTS . **Ex FF EVT**	[Operation / Status Display / Supervision / VTS]
⇧	*Signal: Alarm Fuse Failure Earth Voltage Transformers*

10 Control

Control

Control Page	[Control / Control Page]
This item represents a special dialog. (See the Technical Manual for details.) *Control Page*	

10.1 Ctrl: Device Planning Parameters

10.2 Ctrl: Global Parameters

Ctrl . **Res NonIL**	[Control / General Settings]	
single Operation	single Operation, timeout, permanent ↳ NonIL ResetMode.	C.2
Resetmode Non-Interlocking		

Ctrl . **Timeout NonIL**	[Control / General Settings]	
60s	2s . . . 3600s	C.2
Timeout Non-Interlocking		

Ctrl . **NonIL Assign**	[Control / General Settings]	
“-”	“-” . . . Sys . Internal test state ↳ 1..n, Assignment List.	C.2
Assignment Non-Interlocking		

10.3 Ctrl: Direct Controls

Ctrl . **Switching Authority**	[Control / General Settings]	
Local	None, Local, Remote, Local and Remote ↳ Switching Authority.	C.2
Switching Authority		

Ctrl . **NonInterl**	[Control / General Settings]	
inactive	inactive, active Mode.	C.2
◉	*DC for Non-Interlocking*	

10.4 Ctrl: Input States

Ctrl . **NonInterl-I**	[Operation / Status Display / Control / General Control]
⇩	*Non-Interlocking*

10.5 Ctrl: Signals (Output States)

Ctrl . **Local**	[Operation / Status Display / Control / General Control]
⇧	*Switching Authority: Local*

Ctrl . **Remote**	[Operation / Status Display / Control / General Control]
⇧	*Switching Authority: Remote*

Ctrl . **NonInterl**	[Operation / Status Display / Control / General Control]
⇧	*Non-Interlocking is active*

Ctrl . **SG Indeterm**	[Operation / Status Display / Control / General Control]
⇧	*(At least one) Switchgear is moving (Position cannot be determined).*

Ctrl . **SG Disturb**	[Operation / Status Display / Control / General Control]
⇧	*(At least one) Switchgear is disturbed.*

Ctrl . **CES SAuthority**	[Operation / Status Display / Control / General Control]
⇧	*Command Execution Supervision: Number of rejected Commands because of missing switching authority.*

Ctrl . **CES DoubleOperating**	[Operation / Status Display / Control / General Control]
⇧	*Command Execution Supervision: Number of rejected Commands because a second switch command is in conflict with a pending one.*

10.6 Ctrl: Values

Ctrl . **Switching Authority**	[Operation / Security / Security States]	
Local	None, Local, Remote, Local and Remote ↳ Switching Authority.	
✎	*Switching Authority*	

10.7 SG[1]

Switchgear

10.7.1 SG[1]: Global Parameters

SG[1] . **ON incl Prot ON**	[Control / SG / SG[1] / General Settings]	
active	inactive, active ↳ Mode.	C.2
The ON Command includes the ON Command issued by the Protection module.		

SG[1] . **OFF incl TripCmd**	[Control / SG / SG[1] / General Settings]	
active	inactive, active ↳ Mode.	C.2
The OFF Command includes the OFF Command issued by the Protection module.		

SG[1] . **t-Move ON**	[Control / SG / SG[1] / General Settings]	
0.1s	0.01s ... 100.00s	C.2
Time to move to the ON Position		

SG[1] . **t-Move OFF**	[Control / SG / SG[1] / General Settings]	
0.1s	0.01s ... 100.00s	C.2
Time to move to the OFF Position		

SG[1] . **t-Dwell**	[Control / SG / SG[1] / General Settings]	
0s	0s ... 100.00s	C.2
Dwell time		

SG[1] . **t-TripCmd**	[Control / SG / SG[1] / Trip Manager]	
0.2s	0s ... 300.00s	P.2
Minimum hold time of the OFF-command (circuit breaker, load break switch)		

SG[1] . **Latched**	[Control / SG / SG[1] / Trip Manager]	
inactive	inactive, active ↳ Mode.	P.2
Defines whether the Trip Command is latched.		

SG[1] . **Ack TripCmd**	[Control / SG / SG[1] / Trip Manager]	
“-”	“-” . . . Sys . Internal test state ↳ 1..n, Assignment List.	P.2
Ack TripCmd		

SG[1] . **Off Cmd1**	[Control / SG / SG[1] / Trip Manager]	
V[1] . TripCmd	“-” . . . ExP[4] . TripCmd ↳ 1..n, Trip Cmds.	P.2
Off Command to the Circuit Breaker if the state of the assigned signal becomes true.		

SG[1] . **Off Cmd2**	[Control / SG / SG[1] / Trip Manager]	
V[2] . TripCmd	“-” . . . ExP[4] . TripCmd ↳ 1..n, Trip Cmds.	P.2
Off Command to the Circuit Breaker if the state of the assigned signal becomes true.		

SG[1] . **Off Cmd3**	[Control / SG / SG[1] / Trip Manager]	
f[1] . TripCmd	“-” . . . ExP[4] . TripCmd ↳ 1..n, Trip Cmds.	P.2
Off Command to the Circuit Breaker if the state of the assigned signal becomes true.		

SG[1] . **Off Cmd4**	[Control / SG / SG[1] / Trip Manager]	
f[2] . TripCmd	“-” . . . ExP[4] . TripCmd ↳ 1..n, Trip Cmds.	P.2
Off Command to the Circuit Breaker if the state of the assigned signal becomes true.		

SG[1] . **Off Cmd5** **...** SG[1] . **Off Cmd30**	[Control / SG / SG[1] / Trip Manager]	
"-"	"-" ... ExP[4] . TripCmd ↳ 1..n, Trip Cmds.	P.2
Off Command to the Circuit Breaker if the state of the assigned signal becomes true.		

SG[1] . **Aux ON**	[Control / SG / SG[1] / Pos Indicatrs Wirng]	
DI Slot X1 . DI 1	"-" ... Logics . LE80.Out inverted ↳ 1..n, DI-LogicList.	C.2
The CB is in ON-position if the state of the assigned signal is true (52a).		

SG[1] . **Aux OFF**	[Control / SG / SG[1] / Pos Indicatrs Wirng]	
DI Slot X1 . DI 2	"-" ... Logics . LE80.Out inverted ↳ 1..n, DI-LogicList.	C.2
The CB is in OFF-position if the state of the assigned signal is true (52b).		

SG[1] . **Ready**	[Control / SG / SG[1] / Pos Indicatrs Wirng]	
"-"	"-" ... Logics . LE80.Out inverted ↳ 1..n, DI-LogicList.	C.2
Circuit breaker is ready for operation if the state of the assigned signal is true. This digital input can be used by some protective elements (if they are available within the device) like Auto Reclosure (AR), e.g. as a trigger signal.		

SG[1] . **Removed**	[Control / SG / SG[1] / Pos Indicatrs Wirng]	
"-"	"-" ... Logics . LE80.Out inverted ↳ 1..n, DI-LogicList.	C.2
The withdrawable circuit breaker is Removed		

SG[1] . **SCmd ON**	[Control / SG / SG[1] / Ex ON/OFF Cmd]	
"-"	"-" . . . Logics . LE80.Out inverted ↳ 1..n, DI-LogicList.	C.2
Switching ON Command, e.g. the state of the Logics or the state of the digital input		

SG[1] . **SCmd OFF**	[Control / SG / SG[1] / Ex ON/OFF Cmd]	
"-"	"-" . . . Logics . LE80.Out inverted ↳ 1..n, DI-LogicList.	C.2
Switching OFF Command, e.g. the state of the Logics or the state of the digital input		

SG[1] . **Interl ON1** SG[1] . **Interl ON2** SG[1] . **Interl ON3**	[Control / SG / SG[1] / Interlockings]	
"-"	"-" . . . Sys . Internal test state ↳ 1..n, Assignment List.	C.2
Interlocking of the ON command		

SG[1] . **Interl OFF1** SG[1] . **Interl OFF2** SG[1] . **Interl OFF3**	[Control / SG / SG[1] / Interlockings]	
"-"	"-" . . . Sys . Internal test state ↳ 1..n, Assignment List.	C.2
Interlocking of the OFF command		

SG[1] . **Synchronism**	[Control / SG / SG[1] / Synchron Switchg]	
"-"	"-" . . . Logics . LE80.Out inverted ↳ 1..n, In-SyncList.	C.2
Synchronism		

SG[1] . **t-MaxSyncSuperv**	[Control / SG / SG[1] / Synchron Switchg]	
0.2s	0s . . . 3000.00s	C.2
Synchron-Run timer: Max. time allowed for synchronizing process after a close initiate. Only used for GENERATOR2SYSTEM working mode.		

10.7.2 SG[1]: Direct Controls

SG[1] . **Ack TripCmd**	[Operation / Acknowledge]	
inactive	inactive, active ↳ Mode.	P.1
Acknowledge Trip Command		

SG[1] . **Res SGwear Sl SG**	[Operation / Reset]	
inactive	inactive, active ↳ Mode.	P.1
Resetting the slow Switchgear Alarm		

SG[1] . **Manipulate Position**	[Control / SG / SG[1] / General Settings]	
inactive	inactive, Pos OFF, Pos ON ↳ Manipulate Position.	C.2
WARNING! Fake Position - Manual Position Manipulation		

10.7.3 SG[1]: Input States

SG[1] . **Interl ON1-I** SG[1] . **Interl ON2-I** SG[1] . **Interl ON3-I**	[Operation / Status Display / Control / SG[1]]
State of the module input: Interlocking of the ON command	

SG[1] . **Interl OFF1-I** SG[1] . **Interl OFF2-I** SG[1] . **Interl OFF3-I**	[Operation / Status Display / Control / SG[1]]
⇩	*State of the module input: Interlocking of the OFF command*

SG[1] . **SCmd ON-I**	[Operation / Status Display / Control / SG[1]]
⇩	*State of the module input: Switching ON Command, e.g. the state of the Logics or the state of the digital input*

SG[1] . **SCmd OFF-I**	[Operation / Status Display / Control / SG[1]]
⇩	*State of the module input: Switching OFF Command, e.g. the state of the Logics or the state of the digital input*

SG[1] . **Aux ON-I**	[Operation / Status Display / Control / SG[1]]
⇩	*Module Input State: Position indicator/check-back signal of the CB (52a)*

SG[1] . **Aux OFF-I**	[Operation / Status Display / Control / SG[1]]
⇩	*Module input state: Position indicator/check-back signal of the CB (52b)*

SG[1] . **Ready-I**	[Operation / Status Display / Control / SG[1]]
⇩	*Module input state: CB ready*

SG[1] . **Sys-in-Sync-I**	[Operation / Status Display / Control / SG[1]]
⇩	*State of the module input: This signals has to become true within the synchronization time. If not, switching is unsuccessful.*

SG[1] . **Removed-I**	[Operation / Status Display / Control / SG[1]]
⇩	*State of the module input: The withdrawable circuit breaker is Removed*

SG[1] . **Ack TripCmd-I**	[Operation / Status Display / Control / SG[1]]
⇩	*State of the module input: Acknowledgement Signal (for the Trip Command) Module input signal*

10.7.4 SG[1]: Signals (Output States)

SG[1] . **TripCmd**	[Operation / Status Display / TripCmds] [Operation / Status Display / Control / SG[1]]
⇧	*Signal: Trip Command*

SG[1] . **SI SingleContactInd**	[Operation / Status Display / Control / SG[1]]
⇧	*Signal: The Position of the Switchgear is detected by one auxiliary contact (pole) only. Thus indeterminate and disturbed Positions cannot be detected.*

SG[1] . **Pos not ON**	[Operation / Status Display / Control / SG[1]]
⇧	*Signal: Pos not ON*

SG[1] . **Pos ON**	[Operation / Status Display / Control / SG[1]]
⇧	*Signal: Circuit Breaker is in ON-Position*

SG[1] . **Pos OFF**	[Operation / Status Display / Control / SG[1]]
⇧	*Signal: Circuit Breaker is in OFF-Position*

SG[1] . **Pos Indeterm**	[Operation / Status Display / Control / SG[1]]
⇧	*Signal: Circuit Breaker is in Indeterminate Position*

SG[1] . **Pos Disturb**	[Operation / Status Display / Control / SG[1]]
⇧	*Signal: Circuit Breaker Disturbed - Undefined Breaker Position. The Position Indicators contradict themselves. After expiring of a supervision timer this signal becomes true.*

SG[1] . **Pos**	[Operation / Status Display / Control / SG[1]]
⇧	*Signal: Circuit Breaker Position (0 = Indeterminate, 1 = OFF, 2 = ON, 3 = Disturbed)*

SG[1] . **Ready**	[Operation / Status Display / Control / SG[1]]
⇧	*Signal: Circuit breaker is ready for operation.*

SG[1] . **t-Dwell**	[Operation / Status Display / Control / SG[1]]
⇧	*Signal: Dwell time*

SG[1] . **Removed**	[Operation / Status Display / Control / SG[1]]
⇧	*Signal: The withdrawable circuit breaker is Removed*

SG[1] . **Interl ON**	[Operation / Status Display / Control / SG[1]]
⇧	*Signal: One or more IL_On inputs are active.*

SG[1] . **Interl OFF**	[Operation / Status Display / Control / SG[1]]
⇧	*Signal: One or more IL_Off inputs are active.*

SG[1] . **CES succesf**	[Operation / Status Display / Control / SG[1]]
⇧	*Signal: Command Execution Supervision: Switching command executed successfully.*

SG[1] . **CES Disturbed**	[Operation / Status Display / Control / SG[1]]
⇧	*Signal: Command Execution Supervision: Switching Command unsuccessful. Switchgear in disturbed position.*

SG[1] . **CES Fail TripCmd**	[Operation / Status Display / Control / SG[1]]
⇧	*Signal: Command Execution Supervision: Command execution failed because trip command is pending.*

SG[1] . **CES SwitchDir**	[Operation / Status Display / Control / SG[1]]
⇧	*Signal: Command Execution Supervision respectively Switching Direction Control: This signal becomes true, if a switch command is issued even though the switchgear is already in the requested position. Example: A switchgear that is already OFF should be switched OFF again (doubly). The same applies to CLOSE commands.*

SG[1] . **CES ON d OFF**	[Operation / Status Display / Control / SG[1]]
⇧	*Signal: Command Execution Supervision: On Command during a pending OFF Command.*

SG[1] . **CES SG not ready**	[Operation / Status Display / Control / SG[1]]
⇧	*Signal: Command Execution Supervision: Switchgear not ready*

SG[1] . **CES Fiel Interl**	[Operation / Status Display / Control / SG[1]]
⇧	*Signal: Command Execution Supervision: Switching Command not executed because of field interlocking.*

SG[1] . **CES SyncTimeout**	[Operation / Status Display / Control / SG[1]]
⇧	*Signal: Command Execution Supervision: Switching Command not executed. No Synchronization signal while t-sync was running.*

SG[1] . **CES SG removed**	[Operation / Status Display / Control / SG[1]]
⇧	*Signal: Command Execution Supervision: Switching Command unsuccessful, Switchgear removed.*

SG[1] . **Prot ON**	[Operation / Status Display / Control / SG[1]]
⇧	*Signal: ON Command issued by the Prot module*

SG[1] . **Ack TripCmd**	[Operation / Status Display / Control / SG[1]]
⇧	*Signal: Acknowledge Trip Command*

SG[1] . **ON incl Prot ON**	[Operation / Status Display / Control / SG[1]]
⇧	*Signal: The ON Command includes the ON Command issued by the Protection module.*

SG[1] . **OFF incl TripCmd**	[Operation / Status Display / Control / SG[1]]
⇧	*Signal: The OFF Command includes the OFF Command issued by the Protection module.*

SG[1] . **Position Ind manipul**	[Operation / Status Display / Control / SG[1]]
⇧	*Signal: Position Indicators faked*

SG[1] . **SGwear Slow SG**	[Operation / Status Display / Control / SG[1]]
⇧	*Signal: Alarm, the circuit breaker (load-break switch) becomes slower*

SG[1] . **Res SGwear Sl SG**	[Operation / Status Display / Control / SG[1]]
⇧	*Signal: Resetting the slow Switchgear Alarm*

SG[1] . **ON Cmd**	[Operation / Status Display / Control / SG[1]]
⇧	*Signal: ON Command issued to the switchgear. Depending on the setting the signal may include the ON command of the Prot module.*

SG[1] . **OFF Cmd**	[Operation / Status Display / Control / SG[1]]
⇧	*Signal: OFF Command issued to the switchgear. Depending on the setting the signal may include the OFF command of the Prot module.*

SG[1] . **ON Cmd manual**	[Operation / Status Display / Control / SG[1]]
⇧	*Signal: ON Cmd manual*

SG[1] . **OFF Cmd manual**	[Operation / Status Display / Control / SG[1]]
⇪	*Signal: OFF Cmd manual*

SG[1] . **Sync ON request**	[Operation / Status Display / Control / SG[1]]
⇪	*Signal: Synchronous ON request*

10.7.5 Breaker Wear

Switchgear

10.7.5.1 SG[1]: Global Parameters

SG[1] . **Operations Alarm**	[Control / SG / SG[1] / SG Wear]	
9999	1 ... 100000	C.2
Maximum number of operations. If the operations counter »TripCmd Cr« exceeds this limit then the signal »Operations Alarm« is set.		

10.7.5.2 SG[1]: Direct Controls

SG[1] . **Res TripCmd Cr**	[Operation / Reset]	
inactive	inactive, active Mode.	P.1
Resetting of the Counter: Total number of trips of the switchgear		

10.7.5.3 SG[1]: Signals (Output States)

SG[1] . **Operations Alarm**	[Operation / Status Display / Control / SG[1]]
Signal: Too many Operations. (The operations counter »TripCmd Cr« has exceeded the limit set at »Operations Alarm«.)	

SG[1] . **Res TripCmd Cr**	[Operation / Status Display / Control / SG[1]]
Signal: Resetting of the Counter: Total number of trips of the switchgear	

10.7.5.4 SG[1]: Counters

SG[1] . **TripCmd Cr**	[Operation / Count and RevData / Control / SG[1]]
Counter: Total number of trips of the switchgear.	

11 System Alarms

System Alarms

11.1 SysA: Device Planning Parameters

SysA . **Mode**	[Device planning]	
“-”	“-”, use ↳ Mode.	S.3
general operation mode		

11.2 SysA: Global Parameters

SysA . **Function**	[SysA / General Settings]	
inactive	inactive, active ↳ Mode.	P.2
Permanent activation or deactivation of module/stage.		

SysA . **ExBlo Fc**	[SysA / General Settings]	
“-”	“-” . . . Sys . Internal test state ↳ 1..n, Assignment List.	P.2
Activate (allow) or inactivate (disallow) blocking of the module/stage. This parameter is only effective if a signal is assigned to the corresponding global protection parameter. If the signal becomes true, those modules/stages are blocked that are parameterized "ExBlo Fc=active".		

SysA . **Alarm**	[SysA / THD / V THD]	
inactive	inactive, active ↳ active/inactive.	P.2
Alarm		

SysA . **Threshold**	[SysA / THD / V THD]	
10000V	1V . . . 500000V	P.2
Threshold (to be entered as primary value)		

SysA . **t-Delay**	[SysA / THD / V THD]	
0s	0s ... 3600s	P.2
Tripping Delay		

11.3 SysA: Input States

SysA . **ExBlo-I**	[Operation / Status Display / SysA]
Module input state: External blocking	

11.4 SysA: Signals (Output States)

SysA . **active**	[Operation / Status Display / SysA]
Signal: active	

SysA . **ExBlo**	[Operation / Status Display / SysA]
Signal: External Blocking	

SysA . **Alarm V THD**	[Operation / Status Display / SysA]
Signal: Alarm Total Harmonic Distortion Voltage	

SysA . **Trip V THD**	[Operation / Status Display / SysA]
Signal: Trip Total Harmonic Distortion Voltage	

12 Records

12.1 Event rec

The event recorder logs all events like switching operations, change of parameters, alarms, trips, operating mode selections, blockings and state transitions of inputs and outputs.

Event rec	[Operation / Recorders / Event rec]
	This item represents a special dialog. (See the Technical Manual for details.) *The event recorder logs all events like switching operations, change of parameters, alarms, trips, operating mode selections, blockings and state transitions of inputs and outputs.*

12.1.1 Event rec: Direct Controls

Event rec . **Res all rec**	[Operation / Reset]	
inactive	inactive, active Mode.	P.1
	Reset all records	

12.1.2 Event rec: Signals (Output States)

Event rec . **Res all records**	[Operation / Status Display / Recorders / Event rec]
	Signal: All records are being deleted. (Remark: Immediately afterwards, this signal becomes inactive again.)

12.2 Disturb rec

After a trigger event has become true, the disturbance recorder writes analogue and digital tracks

Disturb rec	[Operation / Recorders / Disturb rec]
	This item represents a special dialog. (See the Technical Manual for details.) *After a trigger event has become true, the disturbance recorder writes analogue and digital tracks*

12.2.1 Disturb rec: Global Parameters

Disturb rec . **Start: 1**	[Device Para / Recorders / Disturb rec]	
Prot . Trip	“-” . . . Sys . Internal test state ↳ 1..n, Assignment List.	S.3
	Start recording if the assigned signal is true.	

Disturb rec . **Start: 2** **. . .** Disturb rec . **Start: 8**	[Device Para / Recorders / Disturb rec]	
“-”	“-” . . . Sys . Internal test state ↳ 1..n, Assignment List.	S.3
	Start recording if the assigned signal is true.	

Disturb rec . **Auto overwriting**	[Device Para / Recorders / Disturb rec]	
active	inactive, active ↳ Mode.	S.3
	If there is no more free memory capacity left, the oldest file will be overwritten.	

Disturb rec . **Pre-trigger time**	[Device Para / Recorders / Disturb rec]	
20%	0% . . . 99%	S.3
	The pre trigger time is set in percent of the »Max file size« value. It corresponds to the part of recording before the onset of the trigger event.	

Disturb rec . **Post-trigger time**	[Device Para / Recorders / Disturb rec]	
20%	0% ... 99%	S.3
The post trigger time is set in percent of the »Max file size« value. It is the remaining time of the »Max file size«, depending on the »Pre-trigger time« setting and the duration of the trigger event, but at maximum the »Post-trigger time« set here.		

Disturb rec . **Max file size**	[Device Para / Recorders / Disturb rec]	
2s	0.1s ... 15.0s	S.3
The maximum storage capacity per record, including pre-trigger and post-trigger time. The amount of records depends on the size of each record, on the max. file size (set here), and on the total storage capacity.		

12.2.2 Disturb rec: Direct Controls

Disturb rec . **Man Trigger**	[Operation / Recorders / Man Trigger]	
False	False, True ↳ true or not true.	P.1
Manual Trigger		

Disturb rec . **Res all rec**	[Operation / Reset]	
inactive	inactive, active ↳ Mode.	P.1
Reset all records		

12.2.3 Disturb rec: Input States

Disturb rec . **Start1-I** ... Disturb rec . **Start8-I**	[Operation / Status Display / Recorders / Disturb rec]
State of the module input:: Trigger event / start recording	

12.2.4 Disturb rec: Signals (Output States)

Disturb rec . **recording**	[Operation / Status Display / Recorders / Disturb rec]
Signal: Recording	

Disturb rec . **memory full**	[Operation / Status Display / Recorders / Disturb rec]
⇧	*Signal: Memory full*

Disturb rec . **Clear fail**	[Operation / Status Display / Recorders / Disturb rec]
⇧	*Signal: Clear failure in memory*

Disturb rec . **Res all records**	[Operation / Status Display / Recorders / Disturb rec]
⇧	*Signal: All records are being deleted. (Remark: Immediately afterwards, this signal becomes inactive again.)*

Disturb rec . **Res all records**	[Operation / Status Display / Recorders / Disturb rec]
⇧	*Signal: All records are being deleted. (Remark: Immediately afterwards, this signal becomes inactive again.)*

Disturb rec . **Man Trigger**	[Operation / Status Display / Recorders / Disturb rec]
⇧	*Signal: Manual Trigger*

12.2.5 Disturb rec: Values

Disturb rec . **Rec state**	[Operation / Status Display / Recorders / Disturb rec]	
Ready	Ready, Recording, Writing file, Trigger Blo ↳ Rec state.	
⇘	*Recording state*	

Disturb rec . **Error code**	[Operation / Status Display / Recorders / Disturb rec]	
OK	OK, Write err, Clear fail, Calculation err, File not found, Auto overwriting off ↳ Fault.	
⇘	*Error code*	

12.3 Fault rec

The values measured at the time of tripping are saved by the Fault Recorder.

Fault rec	[Operation / Recorders / Fault rec]
This item represents a special dialog. (See the Technical Manual for details.) *The values measured at the time of tripping are saved by the Fault Recorder.*	

12.3.1 Fault rec: Global Parameters

Fault rec . **Record-Mode**	[Device Para / Recorders / Fault rec]	
Trips only	Alarms and Trips, Trips only ↳ Record-Mode.	S.3
Recorder Mode (Set the behaviour of the recorder)		

Fault rec . **t-meas-delay**	[Device Para / Recorders / Fault rec]	
0ms	0ms . . . 60ms	S.3
After the Trip, the measurement will be delayed for this time.		

12.3.2 Fault rec: Direct Controls

Fault rec . **Res all rec**	[Operation / Reset]	
inactive	inactive, active ↳ Mode.	P.1
Reset all records		

12.3.3 Fault rec: Signals (Output States)

Fault rec . **Res all records**	[Operation / Status Display / Recorders / Fault rec]
Signal: All records are being deleted. (Remark: Immediately afterwards, this signal becomes inactive again.)	

12.4 Trend rec

Trend Recorder

Trend rec	[Operation / Recorders / Trend rec]
This item represents a special dialog. (See the Technical Manual for details.) *Trend Recorder*	

12.4.1 Trend rec: Global Parameters

Trend rec . **Resolution**	[Device Para / Recorders / Trend rec]	
15 min	60 min, 30 min, 15 min, 10 min, 5 min ↳ Resolution.	S.3
Resolution (recording frequency)		

Trend rec . **Trend1**	[Device Para / Recorders / Trend rec]	
VT . VL1 RMS	“-” . . . VT . VL31 THD ↳ 1..n, TrendRecList.	S.3
Observed Value1		

Trend rec . **Trend2**	[Device Para / Recorders / Trend rec]	
VT . VL2 RMS	“-” . . . VT . VL31 THD ↳ 1..n, TrendRecList.	S.3
Observed Value2		

Trend rec . **Trend3**	[Device Para / Recorders / Trend rec]	
VT . VL3 RMS	“-” . . . VT . VL31 THD ↳ 1..n, TrendRecList.	S.3
Observed Value3		

Trend rec . **Trend4**	[Device Para / Recorders / Trend rec]	
VT . VX meas RMS	“-” . . . VT . VL31 THD ↳ 1..n, TrendRecList.	S.3
Observed Value4		

Trend rec . **Trend5**	[Device Para / Recorders / Trend rec]	
VT . VL12 RMS	“-” . . . VT . VL31 THD ↳ 1..n, TrendRecList.	S.3
Observed Value5		

Trend rec . **Trend6**	[Device Para / Recorders / Trend rec]	
VT . VL23 RMS	“-” . . . VT . VL31 THD ↳ 1..n, TrendRecList.	S.3
Observed Value6		

Trend rec . **Trend7**	[Device Para / Recorders / Trend rec]	
VT . VL31 RMS	“-” . . . VT . VL31 THD ↳ 1..n, TrendRecList.	S.3
Observed Value7		

Trend rec . **Trend8**	[Device Para / Recorders / Trend rec]	
VT . f	“-” . . . VT . VL31 THD ↳ 1..n, TrendRecList.	S.3
Observed Value8		

Trend rec . **Trend9**	[Device Para / Recorders / Trend rec]	
VT . V1	“-” . . . VT . VL31 THD ↳ 1..n, TrendRecList.	S.3
Observed Value9		

Trend rec . **Trend10**	[Device Para / Recorders / Trend rec]	
VT . V2	“-” . . . VT . VL31 THD ↳ 1..n, TrendRecList.	S.3
Observed Value10		

12.4.2 Trend rec: Direct Controls

Trend rec . **Res all rec**	[Operation / Reset]	
inactive	inactive, active ↳ Mode.	P.1
◉	*Reset all records*	

12.4.3 Trend rec: Signals (Output States)

Trend rec . **Res all records**	[Operation / Status Display / Recorders / Trend rec]
⇧	*Signal: All records are being deleted. (Remark: Immediately afterwards, this signal becomes inactive again.)*

12.4.4 Trend rec: Counters

Trend rec . **Max avail Entries**	[Operation / Count and RevData / Trend rec]
#	*Maximum available entries in the current configuration*

13 Logic

13.1 Logics

Logic

13.1.1 Logics: Device Planning Parameters

Logics . **No of Equations:**	[Device planning]	
20	0, 5, 10, 20, 40, 80 ↳ No of Equations:.	S.3
Number of required Logic Equations:		

13.1.2 Logics . . . Logics

Logic

13.1.2.1 Logics: Global Parameters

Logics . **LE1.Gate**	[Logics / LE 1]	
AND	AND, OR, NAND, NOR ↳ LE1.Gate.	S.3
Logic gate		

Logics . **LE1.Input1** **. . .** Logics . **LE1.Input4**	[Logics / LE 1]	
“-”	“-” . . . Sys . Internal test state ↳ 1..n, Assignment List.	S.3
Assignment of the Input Signal		

Logics . **LE1.Inverting1** **. . .** Logics . **LE1.Inverting4**	[Logics / LE 1]	
inactive	inactive, active ↳ Mode.	S.3
Inverting the input signals.		

Logics . **LE1.t-On Delay**	[Logics / LE 1]	
0.00s	0.00s . . . 36000.00s	S.3
Switch On Delay		

Logics . **LE1.t-Off Delay**	[Logics / LE 1]	
0.00s	0.00s . . . 36000.00s	S.3
Switch Off Delay		

Logics . **LE1.Reset Latched**	[Logics / LE 1]	
"-"	"-" . . . Sys . Internal test state ↳ 1..n, Assignment List.	S.3
Reset Signal for the Latching		

Logics . **LE1.Inverting Reset**	[Logics / LE 1]	
inactive	inactive, active ↳ Mode.	S.3
Inverting Reset Signal for the Latching		

Logics . **LE1.Inverting Set**	[Logics / LE 1]	
inactive	inactive, active ↳ Mode.	S.3
Inverting the Setting Signal for the Latching		

13.1.2.2 Logics: Input States

Logics . **LE1.Gate In1-I** **. . .** Logics . **LE1.Gate In4-I**	[Operation / Status Display / Logics]
State of the module input: Assignment of the Input Signal	

Logics . **LE1.Reset Latch-I**	[Operation / Status Display / Logics]
State of the module input: Reset Signal for the Latching	

13.1.2.3 Logics: Signals (Output States)

Logics . **LE1.Gate Out**	[Operation / Status Display / Logics]
Signal: Output of the logic gate	

Logics . **LE1.Timer Out**	[Operation / Status Display / Logics]
Signal: Timer Output	

Logics . **LE1.Out**	[Operation / Status Display / Logics]
⇫	*Signal: Latched Output (Q)*

Logics . **LE1.Out inverted**	[Operation / Status Display / Logics]
⇫	*Signal: Negated Latched Output (Q NOT)*

14 Self-Supervision

SelfSupervision

Messages	[Operation / Self-Supervision / Messages]
	This item represents a special dialog. (See the Technical Manual for details.) *Internal messages*

14.1 SSV: Direct Controls

SSV . **Ack System LED**	[Operation / Acknowledge]	
False	False, True true or not true.	P.1
	Acknowledge System LED (red/green flashing LED)	

14.2 SSV: Signals (Output States)

SSV . **System Error**	[Operation / Self-Supervision / System State]
	Signal: Device Failure

SSV . **SelfSuperVision Contact**	[Operation / Self-Supervision / System State]
	Signal: SelfSuperVision Contact

SSV . **New error**	[Operation / Self-Supervision / System State]
	Signal: A new error message has been issued.

SSV . **New warning**	[Operation / Self-Supervision / System State]
	Signal: A new warning message has been issued.

14.3 SSV: Counters

SSV . **Cr No of free sockets**	[Operation / Self-Supervision / System State]
	Counter for network diagnosis. Number of free sockets.

15 Service

- Sys . Reboot: ⮡ Tab.

15.1 Sgen

Sine wave generator

15.1.1 Sgen: Device Planning Parameters

Sgen . **Mode**	[Device planning]	
use	“-”, use ↳ Mode.	S.3
Sine wave generator, general operation mode		

15.1.2 Sgen: Global Parameters

Sgen . **TripCmd Mode**	[Service / Test (Prot inhibit) / Sgen / Process]	
No TripCmd	No TripCmd, With TripCmd ↳ TripCmd Mode.	S.3
Trip Command Mode: Select between two operating modes for the Fault Simulator: "cold simulation” (without tripping the circuit breaker), or "hot simulation” (i.e. the simulation is authorized to trip the circuit breaker)		

Sgen . **Ex Start Simulation**	[Service / Test (Prot inhibit) / Sgen / Process]	
“-”	“-” . . . Sys . Internal test state ↳ 1..n, Assignment List.	S.3
External Start of Fault Simulation (Using the test parameters)		

Sgen . **ExBlo1**	[Service / Test (Prot inhibit) / Sgen / Process]	
SG[1] . Pos ON	“-” . . . Sys . Internal test state ↳ 1..n, Assignment List.	S.3
External blocking of the module, if blocking is activated (allowed) within a parameter set and if the state of the assigned signal is true.1		

Sgen . **ExBlo2**	[Service / Test (Prot inhibit) / Sgen / Process]	
“-”	“-” . . . Sys . Internal test state ↳ 1..n, Assignment List.	S.3
External blocking of the module, if blocking is activated (allowed) within a parameter set and if the state of the assigned signal is true.2		

Sgen . **Ex ForcePost**	[Service / Test (Prot inhibit) / Sgen / Process]	
"-"	"-" ... Sys . Internal test state ↳ 1..n, Assignment List.	S.3
Force Post state. Abort simulation.		

Sgen . **PreFault**	[Service / Test (Prot inhibit) / Sgen / Configuration / Times]	
0.0s	0.00s ... 300.00s	S.3
Pre Fault Duration		

Sgen . **FaultSimulation**	[Service / Test (Prot inhibit) / Sgen / Configuration / Times]	
0.0s	0.00s ... 10800.00s	S.3
Duration of Fault Simulation		

Sgen . **PostFault**	[Service / Test (Prot inhibit) / Sgen / Configuration / Times]	
0.0s	0.00s ... 300.00s	S.3
Post Fault Duration		

15.1.3 Sgen: Direct Controls

Sgen . **Start Simulation**	[Service / Test (Prot inhibit) / Sgen / Process]	
inactive	inactive, active ↳ Mode.	S.3
Start Fault Simulation (Using the test parameters)		

Sgen . **Stop Simulation**	[Service / Test (Prot inhibit) / Sgen / Process]	
inactive	inactive, active ↳ Mode.	S.3
Stopp Fault Simulation (Using the test parameters)		

15.1.4 Sgen: Input States

Sgen . **Ex Start Simulation-I**	[Operation / Status Display / Sgen]
State of the module input:External Start of Fault Simulation (Using the test parameters)	

Sgen . **ExBlo1-I**	[Operation / Status Display / Sgen] [Service / Test (Prot inhibit) / Sgen / State]
⇩	*Module input state: External blocking1*

Sgen . **ExBlo2-I**	[Operation / Status Display / Sgen] [Service / Test (Prot inhibit) / Sgen / State]
⇩	*Module input state: External blocking2*

Sgen . **Ex ForcePost-I**	[Operation / Status Display / Sgen] [Service / Test (Prot inhibit) / Sgen / State]
⇩	*State of the module input:Force Post state. Abort simulation.*

15.1.5 Sgen: Signals (Output States)

Sgen . **Manual Start**	[Operation / Status Display / Sgen]
⇧	*Fault Simulation has been started manually.*

Sgen . **Manual Stop**	[Operation / Status Display / Sgen]
⇧	*Fault Simulation has been stopped manually.*

Sgen . **Running**	[Operation / Status Display / Sgen] [Service / Test (Prot inhibit) / Sgen / State]
⇧	*Signal; Measuring value simulation is running*

Sgen . **Started**	[Operation / Status Display / Sgen]
⇧	*Fault Simulation has been started*

Sgen . **Stopped**	[Operation / Status Display / Sgen]
⇧	*Fault Simulation has been stopped*

Sgen . **State**	[Operation / Status Display / Sgen]
⇧	*Signal: Wave generation states: 0=Off, 1=PreFault, 2=Fault, 3=PostFault, 4=InitReset*

15.1.6 Sgen: Values

Sgen . **State**	[Service / Test (Prot inhibit) / Sgen / State]	
Off	Off, PreFault, FaultSimulation, PostFault, Init Res ↳ State.	
⟍	*Wave generation states: 0=Off, 1=PreFault, 2=Fault, 3=PostFault, 4=InitReset*	

15.1.7 Sgen

Sine wave generator

15.1.7.1 Sgen: Global Parameters

Sgen . **VL1**	[Service / Test (Prot inhibit) / Sgen / Configuration / PreFault / VT]	
0.57Vn	0.00Vn ... 2.00Vn	S.3
Voltage Fundamental Magnitude in Pre State: phase L1		

Sgen . **VL2**	[Service / Test (Prot inhibit) / Sgen / Configuration / PreFault / VT]	
0.57Vn	0.00Vn ... 2.00Vn	S.3
Voltage Fundamental Magnitude in Pre State: phase L2		

Sgen . **VL3**	[Service / Test (Prot inhibit) / Sgen / Configuration / PreFault / VT]	
0.57Vn	0.00Vn ... 2.00Vn	S.3
Voltage Fundamental Magnitude in Pre State: phase L3		

Sgen . **VX**	[Service / Test (Prot inhibit) / Sgen / Configuration / PreFault / VT]	
0.0Vn	0.00Vn ... 2.00Vn	S.3
Voltage Fundamental Magnitude in Pre State: VX		

Sgen . **phi VL1**	[Service / Test (Prot inhibit) / Sgen / Configuration / PreFault / VT]	
0°	-360° ... 360°	S.3
Start Position respectively Start Angle of the Voltage Phasor during Pre-Phase:phase L1		

Sgen . **phi VL2**	[Service / Test (Prot inhibit) / Sgen / Configuration / PreFault / VT]	
240°	-360° ... 360°	S.3
Start Position respectively Start Angle of the Voltage Phasor during Pre-Phase:phase L2		

Sgen . **phi VL3**	[Service / Test (Prot inhibit) / Sgen / Configuration / PreFault / VT]	
120°	-360° ... 360°	S.3
Start Position respectively Start Angle of the Voltage Phasor during Pre-Phase:phase L3		

Sgen . **phi VX meas**	[Service / Test (Prot inhibit) / Sgen / Configuration / PreFault / VT]	
0°	-360° ... 360°	S.3
Start Position respectively Start Angle of the Voltage Phasor during Pre-Phase: VX		

Sgen . **VL1**	[Service / Test (Prot inhibit) / Sgen / Configuration / FaultSimulation / VT]	
0.29Vn	0.00Vn ... 2.00Vn	S.3
Voltage Fundamental Magnitude in Fault State: phase L1		

Sgen . **VL2**	[Service / Test (Prot inhibit) / Sgen / Configuration / FaultSimulation / VT]	
0.29Vn	0.00Vn ... 2.00Vn	S.3
Voltage Fundamental Magnitude in Fault State: phase L2		

Sgen . **VL3**	[Service / Test (Prot inhibit) / Sgen / Configuration / FaultSimulation / VT]	
0.29Vn	0.00Vn ... 2.00Vn	S.3
Voltage Fundamental Magnitude in Fault State: phase L3		

Sgen . **VX**	[Service / Test (Prot inhibit) / Sgen / Configuration / FaultSimulation / VT]	
0.29Vn	0.00Vn ... 2.00Vn	S.3
Voltage Fundamental Magnitude in Fault State: phase VX		

Sgen . **phi VL1**	[Service / Test (Prot inhibit) / Sgen / Configuration / FaultSimulation / VT]	
0°	-360° ... 360°	S.3
Start Position respectively Start Angle of the Voltage Phasor during Fault-Phase:phase L1		

Sgen . **phi VL2**	[Service / Test (Prot inhibit) / Sgen / Configuration / FaultSimulation / VT]	
240°	-360° ... 360°	S.3
Start Position respectively Start Angle of the Voltage Phasor during Fault-Phase:phase L2		

Sgen . **phi VL3**	[Service / Test (Prot inhibit) / Sgen / Configuration / FaultSimulation / VT]	
120°	-360° ... 360°	S.3
Start Position respectively Start Angle of the Voltage Phasor during Fault-Phase:phase L3		

Sgen . **phi VX meas**	[Service / Test (Prot inhibit) / Sgen / Configuration / FaultSimulation / VT]	
0°	-360° ... 360°	S.3
Start Position respectively Start Angle of the Voltage Phasor during Fault-Phase: VX		

Sgen . **VL1**	[Service / Test (Prot inhibit) / Sgen / Configuration / PostFault / VT]	
0.57Vn	0.00Vn ... 2.00Vn	S.3
Voltage Fundamental Magnitude during Post phase: phase L1		

Sgen . **VL2**	[Service / Test (Prot inhibit) / Sgen / Configuration / PostFault / VT]	
0.57Vn	0.00Vn ... 2.00Vn	S.3
Voltage Fundamental Magnitude during Post phase: phase L2		

Sgen . **VL3**	[Service / Test (Prot inhibit) / Sgen / Configuration / PostFault / VT]	
0.57Vn	0.00Vn ... 2.00Vn	S.3
Voltage Fundamental Magnitude during Post phase: phase L3		

Sgen . **VX**	[Service / Test (Prot inhibit) / Sgen / Configuration / PostFault / VT]	
0.0Vn	0.00Vn ... 2.00Vn	S.3
Voltage Fundamental Magnitude during Post phase: phase VX		

Sgen . **phi VL1**	[Service / Test (Prot inhibit) / Sgen / Configuration / PostFault / VT]	
0°	-360° ... 360°	S.3
Start Position respectively Start Angle of the Voltage Phasor during Post phase: phase L1		

Sgen . **phi VL2**	[Service / Test (Prot inhibit) / Sgen / Configuration / PostFault / VT]	
240°	-360° ... 360°	S.3
Start Position respectively Start Angle of the Voltage Phasor during Post phase: phase L2		

Sgen . **phi VL3**	[Service / Test (Prot inhibit) / Sgen / Configuration / PostFault / VT]	
120°	-360° ... 360°	S.3
Start Position respectively Start Angle of the Voltage Phasor during Post phase: phase L3		

Sgen . **phi VX meas**	[Service / Test (Prot inhibit) / Sgen / Configuration / PostFault / VT]	
0°	-360° ... 360°	S.3
Start Position respectively Start Angle of the Voltage Phasor during Post phase: phase VX		

16 Selection Lists

Rec state

Recording state

Selection list referenced by the following parameters:

- ⮡ Disturb rec . Rec state

Rec state	Description
Ready	*Ready*
Recording	*Recording*
Writing file	*Signal: Writing file*
Trigger Blo	*Trigger signal is still active - wait for fallback. A new record can only be started if and only the trigger signal that started the previous record has fallen back once. Therewith endless records are prevented.*

Fault

Selection list referenced by the following parameters:

- ⮡ Disturb rec . Error code

Fault	Description
OK	*OK*
Write err	*Signal: Writing error in memory*
Clear fail	*Signal: Clear failure in memory*
Calculation err	*Calculation error*
File not found	*File not found*
Auto overwriting off	*If there is no more memory available the record is being stopped.*

State

Selection list referenced by the following parameters:

- ⮡ IEC 61850 . GoosePublisherState
- ⮡ IEC 61850 . GooseSubscriberState
- ⮡ IEC 61850 . MmsServerState

State	Description
Off	*Off*
On	*On*
Error	*Error*

State

Selection list referenced by the following parameters:

- ⮡ Profibus . Slave State

State	Description
Baud Search	*No connection to the PROFIBUS-DP Master*
Baud Found	*The PROFIBUS DP Slave is connected to the bus. The Slave has not yet been addressed by the Master Device (and it was not yet addressed since the last break of the connection).*
PRM OK	*The slave was addressed by the master, the parameter setting message was received and is OK, a configuration message is expected from the master.*
PRM REQ	*The slave is no longer addressed by the master (modified parameters within the master without having the connection stopped, master software is tuned off but lower PROFIBUS layer is still active)*
PRM Fault	*An Error in the parameter setting message (e.g. wrong PNO identification number)*
CFG Fault	*Configuration error the number of input/output bytes parameterised in the master does not match the number parametrised in the device (slave).*
Clear Data	*Master sends a General Control command to clear the data.*
Data exchange	*Master and slave exchange data.*

Baud rate

Selection list referenced by the following parameters:

- ⮡ Profibus . Baud rate

Baud rate	Description
12 Mb/s	*12 Mb/s*

Baud rate	Description
6 Mb/s	*6 Mb/s*
3 Mb/s	*3 Mb/s*
1.5 Mb/s	*1.5 Mb/s*
0.5 Mb/s	*0.5 Mb/s*
187500 baud	*187500 baud*
93750 baud	*93750 baud*
45450 baud	*45450 baud*
19200 baud	*19200 baud*
9600 baud	*9600 baud*
-.-	*-.-*

PNO Id

PNO Identification Number. GSD Identification Number.

Selection list referenced by the following parameters:

- ⮡ Profibus . PNO Id

PNO Id	Description
0C50h	*PnodID for the Config file.*

Config status

Status of the user-defined SCADA configuration.\nPossible values:

Selection list referenced by the following parameters:

- ⮡ Profibus . Config status

Config status	Description
Changing	*New SCADA configuration is being loaded, but not active yet.*
OK	*The SCADA configuration is active.*
Config. not avail.	*The user-defined SCADA configuration is not available (e.g. has not been loaded into the device).*
Error	*Unexpected error. Please contact our service-team.*

Server State

Server State.

Selection list referenced by the following parameters:

- ⮡ SNTP . Used Server

Server State	Description
Server1	*Server1 used.*
Server2	*Server2 used.*
None	*No Server used.*

State

Selection list referenced by the following parameters:

- ⮡ SNTP . ServerQlty
- ⮡ SNTP . NetConn

State	Description
GOOD	*GOOD*
SUFFICIENT	*SUFFICIENT*
BAD	*BAD*
“-”	*NO CONNECTION*

Mode

general operation mode

Selection list referenced by the following parameters:

- ⮡ DI Slot X1 . Inverting 1
- ⮡ BO Slot X2 . Latched
- ⮡ BO Slot X2 . Inverting
- ⮡ BO Slot X2 . Inverting 1

- ⮡ BO Slot X2 . Latched
- ⮡ BO Slot X2 . Inverting
- *[. . .]*

Mode	Description
inactive	*inactive*
active	*active*

true or not true

Selection list referenced by the following parameters:

- ⮡ Disturb rec . Man Trigger
- ⮡ SSV . Ack System LED

true or not true	Description
False	*False*
True	*True*

Type of passw. def.

Type of the password definition. This value is directly related to the security-level of the access to the device.

Selection list referenced by the following parameters:

- ⮡ Sys . Passw. for USB conn.
- ⮡ Sys . Passw.remote net.conn.

Type of passw. def.	Description
disabled	*The password disabled.*
default	*The password is the same as the factory default, i.e. it has not been altered by the user. (However, for devices with a disabled default password the password type is displayed as “disabled”, not as “default”.)*
def. by user	*The password has been defined by the user. This corresponds to the highest security-level of the access to the device.*

TLS Certificate

Type of certificate that the device uses for the encrypted communication. This value is directly related to the security-level of the communication.

Selection list referenced by the following parameters:

- ⮡ Sys . TLS Certificate

TLS Certificate	Description
Device-specific	*The device uses a device-specific certificate for the encrypted communication. This corresponds to the highest security-level of the communication.*
Basic	*The device uses a basic certificate for the encrypted communication. Compared with a device-specific certificate, this means a slightly reduced security level.*
Corrupt	*The certificate for the encrypted communication is corrupt and therefore unusable.*

Switching Authority

Selection list referenced by the following parameters:

- ⮡ Ctrl . Switching Authority
- ⮡ Ctrl . Switching Authority
- ⮡ Ctrl . Switching Authority

Switching Authority	Description
None	*None*
Local	*Local*
Remote	*Remote*
Local and Remote	*Local and Remote*

Config. Device Reset

If the »C« key is pressed while the device is performing a cold restart a general Reset Dialog appears on the screen. Select which options shall be available with this dialog.

Selection list referenced by the following parameters:

- ⮡ HMI . Config. Device Reset

- ⮡ HMI . Config. Device Reset
- ⮡ HMI . Config. Device Reset
- ⮡ HMI . Config. Device Reset

Config. Device Reset	Description
"Fact.def.", "PW rst"	*Two Reset Options shall be available:* *- "Reset to factory defaults",* *- "Reset passwords".*
Only “Fact.defaults”	*Only one Reset Option shall be available:* *- "Reset to factory defaults".* *CAUTION: If this option has been chosen and the password should ever get lost then the only chance to recover control is to reset the protection device to factory defaults.*
Reset deact.	*The Reset Options shall be deactivated.* *CAUTION: If this option has been chosen and the password should ever get lost, then the protection device has to be sent to the manufacturer as a service request.*

Device planning

Selection list referenced by the following parameters:

- ⮡ V[1] . Mode

Device planning	Description
“-”	*do not use*
V>	*V>*
V<	*Pickup value*

Device planning

Selection list referenced by the following parameters:

- ⮡ df/dt . Mode

Device planning	Description
“-”	*do not use*
use	*use*

Device planning

Selection list referenced by the following parameters:

- ⮡ delta phi . Mode

Device planning	Description
“-”	*do not use*
use	*use*

Device planning

Selection list referenced by the following parameters:

- ⮡ Intertripping . Mode

Device planning	Description
“-”	*do not use*
use	*use*

Device planning

Selection list referenced by the following parameters:

- ⮡ LVRT[1] . Mode

Device planning	Description
“-”	*do not use*
use	*use*

Device planning

Selection list referenced by the following parameters:

- ⮡ VG[1] . Mode

Device planning	Description
“-”	*do not use*
V>	*V>*
V<	*Pickup value*

yes/no

Selection list referenced by the following parameters:

- ⮡ Sys . Reboot
- ⮡ VG[1] . Superv. only
- ⮡ Sys . Reboot

yes/no	Description
no	*no*
yes	*yes*

Device planning

Selection list referenced by the following parameters:

- ⮡ V012[1] . Mode

Device planning	Description
“-”	*do not use*
V1>	*Positive Phase Sequence Overvoltage*
V1<	*Positive Phase Sequence Undervoltage*
V2>	*Negative Phase Sequence Overvoltage*

Device planning

Selection list referenced by the following parameters:

- ⮡ f[1] . Mode

Device planning	Description
“-”	*do not use*
f<	*Underfrequency*
f>	*Overfrequency*
f< and df/dt	*Underfrequency and (instantaneous) rate of frequency change*
f> and df/dt	*Overfrequency and (instantaneous) rate of frequency change*
f< and DF/DT	*Underfrequency and (averaged) rate of frequency change*
f> and DF/DT	*Overfrequency and (averaged) rate of frequency change*
df/dt	*Measured value (calculated): Rate-of-frequency-change.*
delta phi	*Measured value (calculated): Vector surge*

Mode

general operation mode

Selection list referenced by the following parameters:

- ⮡ ReCon[1] . Mode

Mode	Description
“-”	*do not use*
use	*use*

Mode

general operation mode

Selection list referenced by the following parameters:

- ⮡ Sync . Mode

Mode	Description
“-”	*do not use*

Mode	Description
use	*use*

Device planning

Selection list referenced by the following parameters:

- ExP[1] . Mode

Device planning	Description
“-”	*do not use*
use	*use*

Device planning

Selection list referenced by the following parameters:

- CBF . Mode

Device planning	Description
“-”	*do not use*
use	*use*

Device planning

Selection list referenced by the following parameters:

- TCS . Mode

Device planning	Description
“-”	*do not use*
use	*use*

Device planning

Selection list referenced by the following parameters:

- ⮡ VTS . Mode

Device planning	Description
“-”	*do not use*
use	*use*

Mode

general operation mode

Selection list referenced by the following parameters:

- ⮡ SysA . Mode

Mode	Description
“-”	*do not use*
use	*use*

Used Protocol

Used SCADA Protocol

Selection list referenced by the following parameters:

- ⮡ Scada . Protocol

Used Protocol	Description
“-”	*do not use*
Modbus RTU	*Modbus Protocol RTU*
Modbus TCP	*Modbus Protocol TCP*
Modbus TCP/RTU	*Modbus Protocol TCP/RTU*
DNP3 RTU	*Distributed Network Protocol RTU*
DNP3 TCP	*Distributed Network Protocol TCP*
DNP3 UDP	*Distributed Network Protocol UDP*
IEC 60870-5-103	*IEC 60870-5-103 Protocol*

Used Protocol	Description
IEC 60870-5-104	*IEC 60870-5-104 Protocol*
IEC 61850	*IEC 61850 communication*
Profibus	*Profibus Module*

Mode

general operation mode

Selection list referenced by the following parameters:

- ⮡ IRIG-B . Mode

Mode	Description
“-”	*do not use*
use	*use*

Mode

general operation mode

Selection list referenced by the following parameters:

- ⮡ SNTP . Mode

Mode	Description
“-”	*do not use*
use	*use*

No of Equations:

Number of required Logic Equations:

Selection list referenced by the following parameters:

- ⮡ Logics . No of Equations:

No of Equations:	Description
0	*0*
5	*5*
10	*10*
20	*20*
40	*40*
80	*80*

Mode

general operation mode

Selection list referenced by the following parameters:

- ⮡ Sgen . Mode

Mode	Description
“-”	*do not use*
use	*use*

Scaling

Display of the measured values as primary, secondary or per unit values

Selection list referenced by the following parameters:

- ⮡ Sys . Scaling

Scaling	Description
Per unit values	*Per unit values*
Primary values	*Primary values*
Secondary values	*Secondary values*

Nom voltage

Nominal voltage of the digital inputs

Selection list referenced by the following parameters:

- ⮡ DI Slot X1 . Nom voltage

Nom voltage	Description
24 VDC	*24 VDC*
48 VDC	*48 VDC*
60 VDC	*60 VDC*
110 VDC	*110 VDC*
230 VDC	*230 VDC*
110 VAC	*110 VAC*
230 VAC	*230 VAC*

Debouncing time

A change of the state of a digital input will only be recognized after the debouncing time has expired (become effective). Thus, transient signals will not be misinterpreted.

Selection list referenced by the following parameters:

- ⮡ DI Slot X1 . Debouncing time 1

Debouncing time	Description
no debouncing time	*no debouncing time*
20 ms	*20 ms*
50 ms	*50 ms*
100 ms	*100 ms*

1...n Operating Modes

Selection list referenced by the following parameters:

- ⮡ BO Slot X2 . Operating Mode
- ⮡ BO Slot X2 . Operating Mode
- ⮡ BO Slot X2 . Operating Mode
- ⮡ BO Slot X2 . Operating Mode

- ⮡ BO Slot X2 . Operating Mode

1...n Operating Modes	Description
Normally open (NO)	*The working principle of the relay corresponds to a normally open contact.*
Normally closed (NC)	*The working principle of the relay corresponds to a normally closed contact.*

1..n, Assignment List

Assignment List

Selection list referenced by the following parameters:

- ⮡ BO Slot X2 . Acknowledgement
- ⮡ BO Slot X2 . Assignment 1
- ⮡ BO Slot X2 . Assignment 2
- ⮡ BO Slot X2 . Acknowledgement
- ⮡ BO Slot X2 . Assignment 1
- ⮡ BO Slot X2 . Assignment 2
- *[. . .]*

1..n, Assignment List	Description
“-”	*No assignment*
Prot . **available**	*Signal: Protection is available*
Prot . **active**	*Signal: active*
Prot . **ExBlo**	*Signal: External Blocking*
Prot . **Blo TripCmd**	*Signal: Trip Command blocked*
Prot . **ExBlo TripCmd**	*Signal: External Blocking of the Trip Command*
Prot . **Alarm L1**	*Signal: General-Alarm L1*
Prot . **Alarm L2**	*Signal: General-Alarm L2*
Prot . **Alarm L3**	*Signal: General-Alarm L3*
Prot . **Alarm G**	*Signal: General-Alarm - Earth fault*
Prot . **Alarm**	*Signal: General Alarm*
Prot . **Trip L1**	*Signal: General Trip L1*
Prot . **Trip L2**	*Signal: General Trip L2*

1..n, Assignment List	Description
Prot . **Trip L3**	*Signal: General Trip L3*
Prot . **Trip G**	*Signal: General Trip Ground fault*
Prot . **Trip**	*Signal: General Trip*
Prot . **Res FaultNo a GridFaultNo**	*Signal: Resetting of fault number and grid fault number.*
Prot . **ExBlo1-I**	*Module input state: External blocking1*
Prot . **ExBlo2-I**	*Module input state: External blocking2*
Prot . **ExBlo TripCmd-I**	*Module input state: External Blocking of the Trip Command*
VT . **Phase seq. wrong**	*Signal that the device has detected a phase sequence (L1-L2-L3 / L1-L3-L2) that is different from the one that had been set at [Field settings / General Settings] »Phase Sequence«.*
Ctrl . **Local**	*Switching Authority: Local*
Ctrl . **Remote**	*Switching Authority: Remote*
Ctrl . **NonInterl**	*Non-Interlocking is active*
Ctrl . **SG Indeterm**	*(At least one) Switchgear is moving (Position cannot be determined).*
Ctrl . **SG Disturb**	*(At least one) Switchgear is disturbed.*
Ctrl . **NonInterl-I**	*Non-Interlocking*
SG[1] . **SI SingleContactInd**	*Signal: The Position of the Switchgear is detected by one auxiliary contact (pole) only. Thus indeterminate and disturbed Positions cannot be detected.*
SG[1] . **Pos not ON**	*Signal: Pos not ON*
SG[1] . **Pos ON**	*Signal: Circuit Breaker is in ON-Position*
SG[1] . **Pos OFF**	*Signal: Circuit Breaker is in OFF-Position*
SG[1] . **Pos Indeterm**	*Signal: Circuit Breaker is in Indeterminate Position*
SG[1] . **Pos Disturb**	*Signal: Circuit Breaker Disturbed - Undefined Breaker Position. The Position Indicators contradict themselves. After expiring of a supervision timer this signal becomes true.*
SG[1] . **Ready**	*Signal: Circuit breaker is ready for operation.*
SG[1] . **t-Dwell**	*Signal: Dwell time*
SG[1] . **Removed**	*Signal: The withdrawable circuit breaker is Removed*
SG[1] . **Interl ON**	*Signal: One or more IL_On inputs are active.*
SG[1] . **Interl OFF**	*Signal: One or more IL_Off inputs are active.*
SG[1] . **CES succesf**	*Signal: Command Execution Supervision: Switching command executed successfully.*
SG[1] . **CES Disturbed**	*Signal: Command Execution Supervision: Switching Command unsuccessful. Switchgear in disturbed position.*

1..n, Assignment List	Description
SG[1] . **CES Fail TripCmd**	*Signal: Command Execution Supervision: Command execution failed because trip command is pending.*
SG[1] . **CES SwitchDir**	*Signal: Command Execution Supervision respectively Switching Direction Control: This signal becomes true, if a switch command is issued even though the switchgear is already in the requested position. Example: A switchgear that is already OFF should be switched OFF again (doubly). The same applies to CLOSE commands.*
SG[1] . **CES ON d OFF**	*Signal: Command Execution Supervision: On Command during a pending OFF Command.*
SG[1] . **CES SG not ready**	*Signal: Command Execution Supervision: Switchgear not ready*
SG[1] . **CES Fiel Interl**	*Signal: Command Execution Supervision: Switching Command not executed because of field interlocking.*
SG[1] . **CES SyncTimeout**	*Signal: Command Execution Supervision: Switching Command not executed. No Synchronization signal while t-sync was running.*
SG[1] . **CES SG removed**	*Signal: Command Execution Supervision: Switching Command unsuccessful, Switchgear removed.*
SG[1] . **Prot ON**	*Signal: ON Command issued by the Prot module*
SG[1] . **TripCmd**	*Signal: Trip Command*
SG[1] . **Ack TripCmd**	*Signal: Acknowledge Trip Command*
SG[1] . **ON incl Prot ON**	*Signal: The ON Command includes the ON Command issued by the Protection module.*
SG[1] . **OFF incl TripCmd**	*Signal: The OFF Command includes the OFF Command issued by the Protection module.*
SG[1] . **Position Ind manipul**	*Signal: Position Indicators faked*
SG[1] . **SGwear Slow SG**	*Signal: Alarm, the circuit breaker (load-break switch) becomes slower*
SG[1] . **Res SGwear Sl SG**	*Signal: Resetting the slow Switchgear Alarm*
SG[1] . **ON Cmd**	*Signal: ON Command issued to the switchgear. Depending on the setting the signal may include the ON command of the Prot module.*
SG[1] . **OFF Cmd**	*Signal: OFF Command issued to the switchgear. Depending on the setting the signal may include the OFF command of the Prot module.*
SG[1] . **ON Cmd manual**	*Signal: ON Cmd manual*
SG[1] . **OFF Cmd manual**	*Signal: OFF Cmd manual*
SG[1] . **Sync ON request**	*Signal: Synchronous ON request*
SG[1] . **Aux ON-I**	*Module Input State: Position indicator/check-back signal of the CB (52a)*
SG[1] . **Aux OFF-I**	*Module input state: Position indicator/check-back signal of the CB (52b)*

1..n, Assignment List	Description
SG[1] . **Ready-I**	*Module input state: CB ready*
SG[1] . **Sys-in-Sync-I**	*State of the module input: This signals has to become true within the synchronization time. If not, switching is unsuccessful.*
SG[1] . **Removed-I**	*State of the module input: The withdrawable circuit breaker is Removed*
SG[1] . **Ack TripCmd-I**	*State of the module input: Acknowledgement Signal (for the Trip Command) Module input signal*
SG[1] . **Interl ON1-I**	*State of the module input: Interlocking of the ON command*
SG[1] . **Interl ON2-I**	*State of the module input: Interlocking of the ON command*
SG[1] . **Interl ON3-I**	*State of the module input: Interlocking of the ON command*
SG[1] . **Interl OFF1-I**	*State of the module input: Interlocking of the OFF command*
SG[1] . **Interl OFF2-I**	*State of the module input: Interlocking of the OFF command*
SG[1] . **Interl OFF3-I**	*State of the module input: Interlocking of the OFF command*
SG[1] . **SCmd ON-I**	*State of the module input: Switching ON Command, e.g. the state of the Logics or the state of the digital input*
SG[1] . **SCmd OFF-I**	*State of the module input: Switching OFF Command, e.g. the state of the Logics or the state of the digital input*
SG[1] . **Operations Alarm**	*Signal: Too many Operations. (The operations counter »TripCmd Cr« has exceeded the limit set at »Operations Alarm«.)*
SG[1] . **Res TripCmd Cr**	*Signal: Resetting of the Counter: Total number of trips of the switchgear*
V[1] . **active**	*Signal: active*
V[1] . **ExBlo**	*Signal: External Blocking*
V[1] . **Blo TripCmd**	*Signal: Trip Command blocked*
V[1] . **ExBlo TripCmd**	*Signal: External Blocking of the Trip Command*
V[1] . **Alarm L1**	*Signal: Alarm L1*
V[1] . **Alarm L2**	*Signal: Alarm L2*
V[1] . **Alarm L3**	*Signal: Alarm L3*
V[1] . **Alarm**	*Signal: Alarm voltage stage*
V[1] . **Trip L1**	*Signal: General Trip Phase L1*
V[1] . **Trip L2**	*Signal: General Trip Phase L2*
V[1] . **Trip L3**	*Signal: General Trip Phase L3*
V[1] . **Trip**	*Signal: Trip*
V[1] . **TripCmd**	*Signal: Trip Command*
V[1] . **ExBlo1-I**	*Module input state: External blocking1*
V[1] . **ExBlo2-I**	*Module input state: External blocking2*

1..n, Assignment List	Description
V[1] . **ExBlo TripCmd-I**	*Module input state: External Blocking of the Trip Command*
V[2] . **active**	*Signal: active*
V[2] . **ExBlo**	*Signal: External Blocking*
V[2] . **Blo TripCmd**	*Signal: Trip Command blocked*
V[2] . **ExBlo TripCmd**	*Signal: External Blocking of the Trip Command*
V[2] . **Alarm L1**	*Signal: Alarm L1*
V[2] . **Alarm L2**	*Signal: Alarm L2*
V[2] . **Alarm L3**	*Signal: Alarm L3*
V[2] . **Alarm**	*Signal: Alarm voltage stage*
V[2] . **Trip L1**	*Signal: General Trip Phase L1*
V[2] . **Trip L2**	*Signal: General Trip Phase L2*
V[2] . **Trip L3**	*Signal: General Trip Phase L3*
V[2] . **Trip**	*Signal: Trip*
V[2] . **TripCmd**	*Signal: Trip Command*
V[2] . **ExBlo1-I**	*Module input state: External blocking1*
V[2] . **ExBlo2-I**	*Module input state: External blocking2*
V[2] . **ExBlo TripCmd-I**	*Module input state: External Blocking of the Trip Command*
V[3] . **active**	*Signal: active*
V[3] . **ExBlo**	*Signal: External Blocking*
V[3] . **Blo TripCmd**	*Signal: Trip Command blocked*
V[3] . **ExBlo TripCmd**	*Signal: External Blocking of the Trip Command*
V[3] . **Alarm L1**	*Signal: Alarm L1*
V[3] . **Alarm L2**	*Signal: Alarm L2*
V[3] . **Alarm L3**	*Signal: Alarm L3*
V[3] . **Alarm**	*Signal: Alarm voltage stage*
V[3] . **Trip L1**	*Signal: General Trip Phase L1*
V[3] . **Trip L2**	*Signal: General Trip Phase L2*
V[3] . **Trip L3**	*Signal: General Trip Phase L3*
V[3] . **Trip**	*Signal: Trip*
V[3] . **TripCmd**	*Signal: Trip Command*
V[3] . **ExBlo1-I**	*Module input state: External blocking1*
V[3] . **ExBlo2-I**	*Module input state: External blocking2*

1..n, Assignment List	Description
V[3] . **ExBlo TripCmd-I**	*Module input state: External Blocking of the Trip Command*
V[4] . **active**	*Signal: active*
V[4] . **ExBlo**	*Signal: External Blocking*
V[4] . **Blo TripCmd**	*Signal: Trip Command blocked*
V[4] . **ExBlo TripCmd**	*Signal: External Blocking of the Trip Command*
V[4] . **Alarm L1**	*Signal: Alarm L1*
V[4] . **Alarm L2**	*Signal: Alarm L2*
V[4] . **Alarm L3**	*Signal: Alarm L3*
V[4] . **Alarm**	*Signal: Alarm voltage stage*
V[4] . **Trip L1**	*Signal: General Trip Phase L1*
V[4] . **Trip L2**	*Signal: General Trip Phase L2*
V[4] . **Trip L3**	*Signal: General Trip Phase L3*
V[4] . **Trip**	*Signal: Trip*
V[4] . **TripCmd**	*Signal: Trip Command*
V[4] . **ExBlo1-I**	*Module input state: External blocking1*
V[4] . **ExBlo2-I**	*Module input state: External blocking2*
V[4] . **ExBlo TripCmd-I**	*Module input state: External Blocking of the Trip Command*
V[5] . **active**	*Signal: active*
V[5] . **ExBlo**	*Signal: External Blocking*
V[5] . **Blo TripCmd**	*Signal: Trip Command blocked*
V[5] . **ExBlo TripCmd**	*Signal: External Blocking of the Trip Command*
V[5] . **Alarm L1**	*Signal: Alarm L1*
V[5] . **Alarm L2**	*Signal: Alarm L2*
V[5] . **Alarm L3**	*Signal: Alarm L3*
V[5] . **Alarm**	*Signal: Alarm voltage stage*
V[5] . **Trip L1**	*Signal: General Trip Phase L1*
V[5] . **Trip L2**	*Signal: General Trip Phase L2*
V[5] . **Trip L3**	*Signal: General Trip Phase L3*
V[5] . **Trip**	*Signal: Trip*
V[5] . **TripCmd**	*Signal: Trip Command*
V[5] . **ExBlo1-I**	*Module input state: External blocking1*
V[5] . **ExBlo2-I**	*Module input state: External blocking2*

1..n, Assignment List	Description
V[5] . **ExBlo TripCmd-I**	*Module input state: External Blocking of the Trip Command*
V[6] . **active**	*Signal: active*
V[6] . **ExBlo**	*Signal: External Blocking*
V[6] . **Blo TripCmd**	*Signal: Trip Command blocked*
V[6] . **ExBlo TripCmd**	*Signal: External Blocking of the Trip Command*
V[6] . **Alarm L1**	*Signal: Alarm L1*
V[6] . **Alarm L2**	*Signal: Alarm L2*
V[6] . **Alarm L3**	*Signal: Alarm L3*
V[6] . **Alarm**	*Signal: Alarm voltage stage*
V[6] . **Trip L1**	*Signal: General Trip Phase L1*
V[6] . **Trip L2**	*Signal: General Trip Phase L2*
V[6] . **Trip L3**	*Signal: General Trip Phase L3*
V[6] . **Trip**	*Signal: Trip*
V[6] . **TripCmd**	*Signal: Trip Command*
V[6] . **ExBlo1-I**	*Module input state: External blocking1*
V[6] . **ExBlo2-I**	*Module input state: External blocking2*
V[6] . **ExBlo TripCmd-I**	*Module input state: External Blocking of the Trip Command*
df/dt . **active**	*Signal: active*
df/dt . **ExBlo**	*Signal: External Blocking*
df/dt . **Blo by V<**	*Signal: Module is blocked by undervoltage.*
df/dt . **Blo TripCmd**	*Signal: Trip Command blocked*
df/dt . **ExBlo TripCmd**	*Signal: External Blocking of the Trip Command*
df/dt . **Alarm**	*Signal: Alarm Frequency Protection (collective signal)*
df/dt . **Trip**	*Signal: Trip Frequency Protection (collective signal)*
df/dt . **TripCmd**	*Signal: Trip Command*
df/dt . **ExBlo1-I**	*Module input state: External blocking1*
df/dt . **ExBlo2-I**	*Module input state: External blocking2*
df/dt . **ExBlo TripCmd-I**	*Module input state: External Blocking of the Trip Command*
delta phi . **active**	*Signal: active*
delta phi . **ExBlo**	*Signal: External Blocking*
delta phi . **Blo by V<**	*Signal: Module is blocked by undervoltage.*
delta phi . **Blo TripCmd**	*Signal: Trip Command blocked*

1..n, Assignment List	Description
delta phi . **ExBlo TripCmd**	*Signal: External Blocking of the Trip Command*
delta phi . **Alarm**	*Signal: Alarm Frequency Protection (collective signal)*
delta phi . **Trip**	*Signal: Trip Frequency Protection (collective signal)*
delta phi . **TripCmd**	*Signal: Trip Command*
delta phi . **ExBlo1-I**	*Module input state: External blocking1*
delta phi . **ExBlo2-I**	*Module input state: External blocking2*
delta phi . **ExBlo TripCmd-I**	*Module input state: External Blocking of the Trip Command*
Intertripping . **active**	*Signal: active*
Intertripping . **ExBlo**	*Signal: External Blocking*
Intertripping . **Blo TripCmd**	*Signal: Trip Command blocked*
Intertripping . **ExBlo TripCmd**	*Signal: External Blocking of the Trip Command*
Intertripping . **Alarm**	*Signal: Alarm*
Intertripping . **Trip**	*Signal: Trip*
Intertripping . **TripCmd**	*Signal: Trip Command*
Intertripping . **ExBlo1-I**	*Module input state: External blocking1*
Intertripping . **ExBlo2-I**	*Module input state: External blocking2*
Intertripping . **ExBlo TripCmd-I**	*Module input state: External Blocking of the Trip Command*
Intertripping . **Alarm-I**	*Module input state: Alarm*
Intertripping . **Trip-I**	*Module input state: Trip*
LVRT[1] . **active**	*Signal: active*
LVRT[1] . **ExBlo**	*Signal: External Blocking*
LVRT[1] . **Blo TripCmd**	*Signal: Trip Command blocked*
LVRT[1] . **ExBlo TripCmd**	*Signal: External Blocking of the Trip Command*
LVRT[1] . **Alarm L1**	*Signal: Alarm L1*
LVRT[1] . **Alarm L2**	*Signal: Alarm L2*
LVRT[1] . **Alarm L3**	*Signal: Alarm L3*
LVRT[1] . **Alarm**	*Signal: Alarm voltage stage*
LVRT[1] . **Trip L1**	*Signal: General Trip Phase L1*
LVRT[1] . **Trip L2**	*Signal: General Trip Phase L2*

1..n, Assignment List	Description
LVRT[1] . **Trip L3**	*Signal: General Trip Phase L3*
LVRT[1] . **Trip**	*Signal: Trip*
LVRT[1] . **TripCmd**	*Signal: Trip Command*
LVRT[1] . **t-LVRT is running**	*Signal: t-LVRT is running*
LVRT[1] . **ExBlo1-I**	*Module input state: External blocking1*
LVRT[1] . **ExBlo2-I**	*Module input state: External blocking2*
LVRT[1] . **ExBlo TripCmd-I**	*Module input state: External Blocking of the Trip Command*
LVRT[2] . **active**	*Signal: active*
LVRT[2] . **ExBlo**	*Signal: External Blocking*
LVRT[2] . **Blo TripCmd**	*Signal: Trip Command blocked*
LVRT[2] . **ExBlo TripCmd**	*Signal: External Blocking of the Trip Command*
LVRT[2] . **Alarm L1**	*Signal: Alarm L1*
LVRT[2] . **Alarm L2**	*Signal: Alarm L2*
LVRT[2] . **Alarm L3**	*Signal: Alarm L3*
LVRT[2] . **Alarm**	*Signal: Alarm voltage stage*
LVRT[2] . **Trip L1**	*Signal: General Trip Phase L1*
LVRT[2] . **Trip L2**	*Signal: General Trip Phase L2*
LVRT[2] . **Trip L3**	*Signal: General Trip Phase L3*
LVRT[2] . **Trip**	*Signal: Trip*
LVRT[2] . **TripCmd**	*Signal: Trip Command*
LVRT[2] . **t-LVRT is running**	*Signal: t-LVRT is running*
LVRT[2] . **ExBlo1-I**	*Module input state: External blocking1*
LVRT[2] . **ExBlo2-I**	*Module input state: External blocking2*
LVRT[2] . **ExBlo TripCmd-I**	*Module input state: External Blocking of the Trip Command*
VG[1] . **active**	*Signal: active*
VG[1] . **ExBlo**	*Signal: External Blocking*
VG[1] . **Blo TripCmd**	*Signal: Trip Command blocked*
VG[1] . **ExBlo TripCmd**	*Signal: External Blocking of the Trip Command*
VG[1] . **Alarm**	*Signal: Alarm Residual Voltage Supervision-stage*

1..n, Assignment List	Description
VG[1] . **Trip**	*Signal: Trip*
VG[1] . **TripCmd**	*Signal: Trip Command*
VG[1] . **ExBlo1-I**	*Module input state: External blocking1*
VG[1] . **ExBlo2-I**	*Module input state: External blocking2*
VG[1] . **ExBlo TripCmd-I**	*Module input state: External Blocking of the Trip Command*
VG[2] . **active**	*Signal: active*
VG[2] . **ExBlo**	*Signal: External Blocking*
VG[2] . **Blo TripCmd**	*Signal: Trip Command blocked*
VG[2] . **ExBlo TripCmd**	*Signal: External Blocking of the Trip Command*
VG[2] . **Alarm**	*Signal: Alarm Residual Voltage Supervision-stage*
VG[2] . **Trip**	*Signal: Trip*
VG[2] . **TripCmd**	*Signal: Trip Command*
VG[2] . **ExBlo1-I**	*Module input state: External blocking1*
VG[2] . **ExBlo2-I**	*Module input state: External blocking2*
VG[2] . **ExBlo TripCmd-I**	*Module input state: External Blocking of the Trip Command*
V012[1] . **active**	*Signal: active*
V012[1] . **ExBlo**	*Signal: External Blocking*
V012[1] . **Blo TripCmd**	*Signal: Trip Command blocked*
V012[1] . **ExBlo TripCmd**	*Signal: External Blocking of the Trip Command*
V012[1] . **Alarm**	*Signal: Alarm voltage asymmetry*
V012[1] . **Trip**	*Signal: Trip*
V012[1] . **TripCmd**	*Signal: Trip Command*
V012[1] . **ExBlo1-I**	*Module input state: External blocking1*
V012[1] . **ExBlo2-I**	*Module input state: External blocking2*
V012[1] . **ExBlo TripCmd-I**	*Module input state: External Blocking of the Trip Command*
V012[2] . **active**	*Signal: active*
V012[2] . **ExBlo**	*Signal: External Blocking*
V012[2] . **Blo TripCmd**	*Signal: Trip Command blocked*
V012[2] . **ExBlo TripCmd**	*Signal: External Blocking of the Trip Command*
V012[2] . **Alarm**	*Signal: Alarm voltage asymmetry*
V012[2] . **Trip**	*Signal: Trip*

1..n, Assignment List	Description
V012[2] . **TripCmd**	*Signal: Trip Command*
V012[2] . **ExBlo1-I**	*Module input state: External blocking1*
V012[2] . **ExBlo2-I**	*Module input state: External blocking2*
V012[2] . **ExBlo TripCmd-I**	*Module input state: External Blocking of the Trip Command*
V012[3] . **active**	*Signal: active*
V012[3] . **ExBlo**	*Signal: External Blocking*
V012[3] . **Blo TripCmd**	*Signal: Trip Command blocked*
V012[3] . **ExBlo TripCmd**	*Signal: External Blocking of the Trip Command*
V012[3] . **Alarm**	*Signal: Alarm voltage asymmetry*
V012[3] . **Trip**	*Signal: Trip*
V012[3] . **TripCmd**	*Signal: Trip Command*
V012[3] . **ExBlo1-I**	*Module input state: External blocking1*
V012[3] . **ExBlo2-I**	*Module input state: External blocking2*
V012[3] . **ExBlo TripCmd-I**	*Module input state: External Blocking of the Trip Command*
V012[4] . **active**	*Signal: active*
V012[4] . **ExBlo**	*Signal: External Blocking*
V012[4] . **Blo TripCmd**	*Signal: Trip Command blocked*
V012[4] . **ExBlo TripCmd**	*Signal: External Blocking of the Trip Command*
V012[4] . **Alarm**	*Signal: Alarm voltage asymmetry*
V012[4] . **Trip**	*Signal: Trip*
V012[4] . **TripCmd**	*Signal: Trip Command*
V012[4] . **ExBlo1-I**	*Module input state: External blocking1*
V012[4] . **ExBlo2-I**	*Module input state: External blocking2*
V012[4] . **ExBlo TripCmd-I**	*Module input state: External Blocking of the Trip Command*
V012[5] . **active**	*Signal: active*
V012[5] . **ExBlo**	*Signal: External Blocking*
V012[5] . **Blo TripCmd**	*Signal: Trip Command blocked*
V012[5] . **ExBlo TripCmd**	*Signal: External Blocking of the Trip Command*
V012[5] . **Alarm**	*Signal: Alarm voltage asymmetry*
V012[5] . **Trip**	*Signal: Trip*

1..n, Assignment List	Description
V012[5] . **TripCmd**	*Signal: Trip Command*
V012[5] . **ExBlo1-I**	*Module input state: External blocking1*
V012[5] . **ExBlo2-I**	*Module input state: External blocking2*
V012[5] . **ExBlo TripCmd-I**	*Module input state: External Blocking of the Trip Command*
V012[6] . **active**	*Signal: active*
V012[6] . **ExBlo**	*Signal: External Blocking*
V012[6] . **Blo TripCmd**	*Signal: Trip Command blocked*
V012[6] . **ExBlo TripCmd**	*Signal: External Blocking of the Trip Command*
V012[6] . **Alarm**	*Signal: Alarm voltage asymmetry*
V012[6] . **Trip**	*Signal: Trip*
V012[6] . **TripCmd**	*Signal: Trip Command*
V012[6] . **ExBlo1-I**	*Module input state: External blocking1*
V012[6] . **ExBlo2-I**	*Module input state: External blocking2*
V012[6] . **ExBlo TripCmd-I**	*Module input state: External Blocking of the Trip Command*
f[1] . **active**	*Signal: active*
f[1] . **ExBlo**	*Signal: External Blocking*
f[1] . **Blo by V<**	*Signal: Module is blocked by undervoltage.*
f[1] . **Blo TripCmd**	*Signal: Trip Command blocked*
f[1] . **ExBlo TripCmd**	*Signal: External Blocking of the Trip Command*
f[1] . **Alarm f**	*Signal: Alarm Frequency Protection*
f[1] . **Alarm df/dt | DF/DT**	*Alarm instantaneous or average value of the rate-of-frequency-change*
f[1] . **Alarm delta phi**	*Signal: Alarm Vector Surge*
f[1] . **Alarm**	*Signal: Alarm Frequency Protection (collective signal)*
f[1] . **Trip f**	*Signal: Frequency has exceeded the limit.*
f[1] . **Trip df/dt | DF/DT**	*Signal: Trip df/dt or DF/DT*
f[1] . **Trip delta phi**	*Signal: Trip Vector Surge*
f[1] . **Trip**	*Signal: Trip Frequency Protection (collective signal)*
f[1] . **TripCmd**	*Signal: Trip Command*
f[1] . **ExBlo1-I**	*Module input state: External blocking1*
f[1] . **ExBlo2-I**	*Module input state: External blocking2*

1..n, Assignment List	Description
f[1] . **ExBlo TripCmd-I**	*Module input state: External Blocking of the Trip Command*
f[2] . **active**	*Signal: active*
f[2] . **ExBlo**	*Signal: External Blocking*
f[2] . **Blo by V<**	*Signal: Module is blocked by undervoltage.*
f[2] . **Blo TripCmd**	*Signal: Trip Command blocked*
f[2] . **ExBlo TripCmd**	*Signal: External Blocking of the Trip Command*
f[2] . **Alarm f**	*Signal: Alarm Frequency Protection*
f[2] . **Alarm df/dt | DF/DT**	*Alarm instantaneous or average value of the rate-of-frequency-change*
f[2] . **Alarm delta phi**	*Signal: Alarm Vector Surge*
f[2] . **Alarm**	*Signal: Alarm Frequency Protection (collective signal)*
f[2] . **Trip f**	*Signal: Frequency has exceeded the limit.*
f[2] . **Trip df/dt | DF/DT**	*Signal: Trip df/dt or DF/DT*
f[2] . **Trip delta phi**	*Signal: Trip Vector Surge*
f[2] . **Trip**	*Signal: Trip Frequency Protection (collective signal)*
f[2] . **TripCmd**	*Signal: Trip Command*
f[2] . **ExBlo1-I**	*Module input state: External blocking1*
f[2] . **ExBlo2-I**	*Module input state: External blocking2*
f[2] . **ExBlo TripCmd-I**	*Module input state: External Blocking of the Trip Command*
f[3] . **active**	*Signal: active*
f[3] . **ExBlo**	*Signal: External Blocking*
f[3] . **Blo by V<**	*Signal: Module is blocked by undervoltage.*
f[3] . **Blo TripCmd**	*Signal: Trip Command blocked*
f[3] . **ExBlo TripCmd**	*Signal: External Blocking of the Trip Command*
f[3] . **Alarm f**	*Signal: Alarm Frequency Protection*
f[3] . **Alarm df/dt | DF/DT**	*Alarm instantaneous or average value of the rate-of-frequency-change*
f[3] . **Alarm delta phi**	*Signal: Alarm Vector Surge*
f[3] . **Alarm**	*Signal: Alarm Frequency Protection (collective signal)*
f[3] . **Trip f**	*Signal: Frequency has exceeded the limit.*
f[3] . **Trip df/dt | DF/DT**	*Signal: Trip df/dt or DF/DT*
f[3] . **Trip delta phi**	*Signal: Trip Vector Surge*
f[3] . **Trip**	*Signal: Trip Frequency Protection (collective signal)*

1..n, Assignment List	Description
f[3] . **TripCmd**	*Signal: Trip Command*
f[3] . **ExBlo1-I**	*Module input state: External blocking1*
f[3] . **ExBlo2-I**	*Module input state: External blocking2*
f[3] . **ExBlo TripCmd-I**	*Module input state: External Blocking of the Trip Command*
f[4] . **active**	*Signal: active*
f[4] . **ExBlo**	*Signal: External Blocking*
f[4] . **Blo by V<**	*Signal: Module is blocked by undervoltage.*
f[4] . **Blo TripCmd**	*Signal: Trip Command blocked*
f[4] . **ExBlo TripCmd**	*Signal: External Blocking of the Trip Command*
f[4] . **Alarm f**	*Signal: Alarm Frequency Protection*
f[4] . **Alarm df/dt | DF/DT**	*Alarm instantaneous or average value of the rate-of-frequency-change*
f[4] . **Alarm delta phi**	*Signal: Alarm Vector Surge*
f[4] . **Alarm**	*Signal: Alarm Frequency Protection (collective signal)*
f[4] . **Trip f**	*Signal: Frequency has exceeded the limit.*
f[4] . **Trip df/dt | DF/DT**	*Signal: Trip df/dt or DF/DT*
f[4] . **Trip delta phi**	*Signal: Trip Vector Surge*
f[4] . **Trip**	*Signal: Trip Frequency Protection (collective signal)*
f[4] . **TripCmd**	*Signal: Trip Command*
f[4] . **ExBlo1-I**	*Module input state: External blocking1*
f[4] . **ExBlo2-I**	*Module input state: External blocking2*
f[4] . **ExBlo TripCmd-I**	*Module input state: External Blocking of the Trip Command*
f[5] . **active**	*Signal: active*
f[5] . **ExBlo**	*Signal: External Blocking*
f[5] . **Blo by V<**	*Signal: Module is blocked by undervoltage.*
f[5] . **Blo TripCmd**	*Signal: Trip Command blocked*
f[5] . **ExBlo TripCmd**	*Signal: External Blocking of the Trip Command*
f[5] . **Alarm f**	*Signal: Alarm Frequency Protection*
f[5] . **Alarm df/dt | DF/DT**	*Alarm instantaneous or average value of the rate-of-frequency-change*
f[5] . **Alarm delta phi**	*Signal: Alarm Vector Surge*
f[5] . **Alarm**	*Signal: Alarm Frequency Protection (collective signal)*
f[5] . **Trip f**	*Signal: Frequency has exceeded the limit.*

1..n, Assignment List	Description
f[5] . **Trip df/dt | DF/DT**	*Signal: Trip df/dt or DF/DT*
f[5] . **Trip delta phi**	*Signal: Trip Vector Surge*
f[5] . **Trip**	*Signal: Trip Frequency Protection (collective signal)*
f[5] . **TripCmd**	*Signal: Trip Command*
f[5] . **ExBlo1-I**	*Module input state: External blocking1*
f[5] . **ExBlo2-I**	*Module input state: External blocking2*
f[5] . **ExBlo TripCmd-I**	*Module input state: External Blocking of the Trip Command*
f[6] . **active**	*Signal: active*
f[6] . **ExBlo**	*Signal: External Blocking*
f[6] . **Blo by V<**	*Signal: Module is blocked by undervoltage.*
f[6] . **Blo TripCmd**	*Signal: Trip Command blocked*
f[6] . **ExBlo TripCmd**	*Signal: External Blocking of the Trip Command*
f[6] . **Alarm f**	*Signal: Alarm Frequency Protection*
f[6] . **Alarm df/dt | DF/DT**	*Alarm instantaneous or average value of the rate-of-frequency-change*
f[6] . **Alarm delta phi**	*Signal: Alarm Vector Surge*
f[6] . **Alarm**	*Signal: Alarm Frequency Protection (collective signal)*
f[6] . **Trip f**	*Signal: Frequency has exceeded the limit.*
f[6] . **Trip df/dt | DF/DT**	*Signal: Trip df/dt or DF/DT*
f[6] . **Trip delta phi**	*Signal: Trip Vector Surge*
f[6] . **Trip**	*Signal: Trip Frequency Protection (collective signal)*
f[6] . **TripCmd**	*Signal: Trip Command*
f[6] . **ExBlo1-I**	*Module input state: External blocking1*
f[6] . **ExBlo2-I**	*Module input state: External blocking2*
f[6] . **ExBlo TripCmd-I**	*Module input state: External Blocking of the Trip Command*
ReCon[1] . **active**	*Signal: active*
ReCon[1] . **ExBlo**	*Signal: External Blocking*
ReCon[1] . **Blo by Meas Ciruit Superv**	*Signal: Module blocked by measuring cirucuit supervision*
ReCon[1] . **Release Energy Resource**	*Signal: Release Energy Resource.*
ReCon[1] . **ExBlo1-I**	*Module input state: External blocking1*
ReCon[1] . **ExBlo2-I**	*Module input state: External blocking2*

1..n, Assignment List	Description
ReCon[1] . **V Ext Release PCC-I**	*Module input state: Release signal is being generated by the PCC (External Release)*
ReCon[1] . **PCC Fuse Fail VT-I**	*State of the module input: Blocking if the fuse of a voltage transformer has tripped at the PCC.*
ReCon[1] . **reconnected-I**	*This signal indicates the state "reconnected" (mains parallel).*
ReCon[1] . **Decoupling1-I**	*Decoupling function, that blocks the reconnection.*
ReCon[1] . **Decoupling2-I**	*Decoupling function, that blocks the reconnection.*
ReCon[1] . **Decoupling3-I**	*Decoupling function, that blocks the reconnection.*
ReCon[1] . **Decoupling4-I**	*Decoupling function, that blocks the reconnection.*
ReCon[1] . **Decoupling5-I**	*Decoupling function, that blocks the reconnection.*
ReCon[1] . **Decoupling6-I**	*Decoupling function, that blocks the reconnection.*
ReCon[2] . **active**	*Signal: active*
ReCon[2] . **ExBlo**	*Signal: External Blocking*
ReCon[2] . **Blo by Meas Ciruit Superv**	*Signal: Module blocked by measuring cirucuit supervision*
ReCon[2] . **Release Energy Resource**	*Signal: Release Energy Resource.*
ReCon[2] . **ExBlo1-I**	*Module input state: External blocking1*
ReCon[2] . **ExBlo2-I**	*Module input state: External blocking2*
ReCon[2] . **V Ext Release PCC-I**	*Module input state: Release signal is being generated by the PCC (External Release)*
ReCon[2] . **PCC Fuse Fail VT-I**	*State of the module input: Blocking if the fuse of a voltage transformer has tripped at the PCC.*
ReCon[2] . **reconnected-I**	*This signal indicates the state "reconnected" (mains parallel).*
ReCon[2] . **Decoupling1-I**	*Decoupling function, that blocks the reconnection.*
ReCon[2] . **Decoupling2-I**	*Decoupling function, that blocks the reconnection.*
ReCon[2] . **Decoupling3-I**	*Decoupling function, that blocks the reconnection.*
ReCon[2] . **Decoupling4-I**	*Decoupling function, that blocks the reconnection.*

1..n, Assignment List	Description
ReCon[2] . **Decoupling5-I**	*Decoupling function, that blocks the reconnection.*
ReCon[2] . **Decoupling6-I**	*Decoupling function, that blocks the reconnection.*
Sync . **active**	*Signal: active*
Sync . **ExBlo**	*Signal: External Blocking*
Sync . **LiveBus**	*Signal: Live-Bus flag: 1=Live-Bus, 0=Voltage is below the LiveBus threshold*
Sync . **LiveLine**	*Signal: Live Line flag: 1=Live-Line, 0=Voltage is below the LiveLine threshold*
Sync . **SynchronRunTiming**	*Signal: Synchron-Run-timer is timing (This timer starts when Close-Initiate is coming and stops if breaker is closed. Timeout means synchronizing failed.)*
Sync . **SynchronFailed**	*Signal: This signal indicates a failed synchronization. It is set for 5s when the circuit breaker is still open after the Synchron-Run-timer has timed out.*
Sync . **SyncOverridden**	*Signal:Synchronism Check is overridden because one of the Synchronism overriding conditions (DB/DL or ExtBypass) is met.*
Sync . **VDiffTooHigh**	*Signal: Voltage difference between bus and line too high.*
Sync . **SlipTooHigh**	*Signal: Frequency difference (slip frequency) between bus and line voltages too high.*
Sync . **AngleDiffTooHigh**	*Signal: Phase Angle difference between bus and line voltages too high.*
Sync . **Sys-in-Sync**	*Signal: Bus and line voltages are in synchronism according to the system synchronism criteria.*
Sync . **Ready to Close**	*Signal: Ready to Close*
Sync . **ExBlo1-I**	*Module input state: External blocking1*
Sync . **ExBlo2-I**	*Module input state: External blocking2*
Sync . **Bypass-I**	*State of the module input: The Synchrocheck will be bypassed if the state of the assigned signal (logic input) becomes true.*
Sync . **CBCloseInitiate-I**	*State of the module input: Breaker Close Initiate with synchronism check from any control sources (e.g. HMI / SCADA). If the state of the assigned signal becomes true, a Breaker Close will be initiated (Trigger Source).*
ExP[1] . **active**	*Signal: active*
ExP[1] . **ExBlo**	*Signal: External Blocking*
ExP[1] . **Blo TripCmd**	*Signal: Trip Command blocked*
ExP[1] . **ExBlo TripCmd**	*Signal: External Blocking of the Trip Command*
ExP[1] . **Alarm**	*Signal: Alarm*

1..n, Assignment List	Description
ExP[1] . **Trip**	*Signal: Trip*
ExP[1] . **TripCmd**	*Signal: Trip Command*
ExP[1] . **ExBlo1-I**	*Module input state: External blocking1*
ExP[1] . **ExBlo2-I**	*Module input state: External blocking2*
ExP[1] . **ExBlo TripCmd-I**	*Module input state: External Blocking of the Trip Command*
ExP[1] . **Alarm-I**	*Module input state: Alarm*
ExP[1] . **Trip-I**	*Module input state: Trip*
ExP[2] . **active**	*Signal: active*
ExP[2] . **ExBlo**	*Signal: External Blocking*
ExP[2] . **Blo TripCmd**	*Signal: Trip Command blocked*
ExP[2] . **ExBlo TripCmd**	*Signal: External Blocking of the Trip Command*
ExP[2] . **Alarm**	*Signal: Alarm*
ExP[2] . **Trip**	*Signal: Trip*
ExP[2] . **TripCmd**	*Signal: Trip Command*
ExP[2] . **ExBlo1-I**	*Module input state: External blocking1*
ExP[2] . **ExBlo2-I**	*Module input state: External blocking2*
ExP[2] . **ExBlo TripCmd-I**	*Module input state: External Blocking of the Trip Command*
ExP[2] . **Alarm-I**	*Module input state: Alarm*
ExP[2] . **Trip-I**	*Module input state: Trip*
ExP[3] . **active**	*Signal: active*
ExP[3] . **ExBlo**	*Signal: External Blocking*
ExP[3] . **Blo TripCmd**	*Signal: Trip Command blocked*
ExP[3] . **ExBlo TripCmd**	*Signal: External Blocking of the Trip Command*
ExP[3] . **Alarm**	*Signal: Alarm*
ExP[3] . **Trip**	*Signal: Trip*
ExP[3] . **TripCmd**	*Signal: Trip Command*
ExP[3] . **ExBlo1-I**	*Module input state: External blocking1*
ExP[3] . **ExBlo2-I**	*Module input state: External blocking2*
ExP[3] . **ExBlo TripCmd-I**	*Module input state: External Blocking of the Trip Command*
ExP[3] . **Alarm-I**	*Module input state: Alarm*
ExP[3] . **Trip-I**	*Module input state: Trip*
ExP[4] . **active**	*Signal: active*

1..n, Assignment List	Description
ExP[4] . **ExBlo**	*Signal: External Blocking*
ExP[4] . **Blo TripCmd**	*Signal: Trip Command blocked*
ExP[4] . **ExBlo TripCmd**	*Signal: External Blocking of the Trip Command*
ExP[4] . **Alarm**	*Signal: Alarm*
ExP[4] . **Trip**	*Signal: Trip*
ExP[4] . **TripCmd**	*Signal: Trip Command*
ExP[4] . **ExBlo1-I**	*Module input state: External blocking1*
ExP[4] . **ExBlo2-I**	*Module input state: External blocking2*
ExP[4] . **ExBlo TripCmd-I**	*Module input state: External Blocking of the Trip Command*
ExP[4] . **Alarm-I**	*Module input state: Alarm*
ExP[4] . **Trip-I**	*Module input state: Trip*
CBF . **active**	*Signal: active*
CBF . **ExBlo**	*Signal: External Blocking*
CBF . **Waiting for Trigger**	*Waiting for Trigger*
CBF . **running**	*Signal: CBF-Module started*
CBF . **Alarm**	*Signal: Circuit Breaker Failure*
CBF . **Lockout**	*Signal: Lockout*
CBF . **Res Lockout**	*Signal: Reset Lockout*
CBF . **ExBlo1-I**	*Module input state: External blocking1*
CBF . **ExBlo2-I**	*Module input state: External blocking2*
CBF . **Trigger1-I**	*Module Input: Trigger that will start the CBF*
CBF . **Trigger2-I**	*Module Input: Trigger that will start the CBF*
CBF . **Trigger3-I**	*Module Input: Trigger that will start the CBF*
TCS . **active**	*Signal: active*
TCS . **ExBlo**	*Signal: External Blocking*
TCS . **Alarm**	*Signal: Alarm Trip Circuit Supervision*
TCS . **Not Possible**	*Not possible because no state indicator assigned to the breaker.*
TCS . **Aux ON-I**	*Module Input State: Position indicator/check-back signal of the CB (52a)*
TCS . **Aux OFF-I**	*Module input state: Position indicator/check-back signal of the CB (52b)*
TCS . **ExBlo1-I**	*Module input state: External blocking1*
TCS . **ExBlo2-I**	*Module input state: External blocking2*

1..n, Assignment List	Description
VTS . **active**	*Signal: active*
VTS . **ExBlo**	*Signal: External Blocking*
VTS . **Alarm ΔV**	*Signal: Alarm ΔV Voltage Transformer Measuring Circuit Supervision*
VTS . **Alarm**	*Signal: Alarm Voltage Transformer Measuring Circuit Supervision*
VTS . **Ex FF VT**	*Signal: Ex FF VT*
VTS . **Ex FF EVT**	*Signal: Alarm Fuse Failure Earth Voltage Transformers*
VTS . **Ex Fuse Fail VT-I**	*Module input state: External fuse failure voltage transformers*
VTS . **Ex Fuse Fail EVT-I**	*Module input state: External fuse failure earth voltage transformer*
VTS . **ExBlo1-I**	*Module input state: External blocking1*
VTS . **ExBlo2-I**	*Module input state: External blocking2*
SysA . **active**	*Signal: active*
SysA . **ExBlo**	*Signal: External Blocking*
SysA . **Alarm V THD**	*Signal: Alarm Total Harmonic Distortion Voltage*
SysA . **Trip V THD**	*Signal: Trip Total Harmonic Distortion Voltage*
SysA . **ExBlo-I**	*Module input state: External blocking*
DI Slot X1 . **DI 1**	*Signal: Digital Input*
DI Slot X1 . **DI 2**	*Signal: Digital Input*
DI Slot X1 . **DI 3**	*Signal: Digital Input*
DI Slot X1 . **DI 4**	*Signal: Digital Input*
DI Slot X1 . **DI 5**	*Signal: Digital Input*
DI Slot X1 . **DI 6**	*Signal: Digital Input*
DI Slot X1 . **DI 7**	*Signal: Digital Input*
DI Slot X1 . **DI 8**	*Signal: Digital Input*
BO Slot X2 . **BO 1**	*Signal: Binary Output Relay*
BO Slot X2 . **BO 2**	*Signal: Binary Output Relay*
BO Slot X2 . **BO 3**	*Signal: Binary Output Relay*
BO Slot X2 . **BO 4**	*Signal: Binary Output Relay*
BO Slot X2 . **BO 5**	*Signal: Binary Output Relay*
BO Slot X2 . **DISARMED!**	*Signal: CAUTION! RELAYS DISARMED in order to safely perform maintenance while eliminating the risk of taking an entire process off-line. (Note: The Self Supervision Contact cannot be disarmed). YOU MUST ENSURE that the relays are ARMED AGAIN after maintenance*

1..n, Assignment List	Description
BO Slot X2 . **Outs forced**	*Signal: The State of at least one Relay Output has been set by force. That means that the state of at least one Relay is forced and hence does not show the state of the assigned signals.*
Event rec . **Res all records**	*Signal: All records are being deleted. (Remark: Immediately afterwards, this signal becomes inactive again.)*
Disturb rec . **recording**	*Signal: Recording*
Disturb rec . **memory full**	*Signal: Memory full*
Disturb rec . **Clear fail**	*Signal: Clear failure in memory*
Disturb rec . **Res all records**	*Signal: All records are being deleted. (Remark: Immediately afterwards, this signal becomes inactive again.)*
Disturb rec . **Res all records**	*Signal: All records are being deleted. (Remark: Immediately afterwards, this signal becomes inactive again.)*
Disturb rec . **Man Trigger**	*Signal: Manual Trigger*
Disturb rec . **Start1-I**	*State of the module input:: Trigger event / start recording*
Disturb rec . **Start2-I**	*State of the module input:: Trigger event / start recording*
Disturb rec . **Start3-I**	*State of the module input:: Trigger event / start recording*
Disturb rec . **Start4-I**	*State of the module input:: Trigger event / start recording*
Disturb rec . **Start5-I**	*State of the module input:: Trigger event / start recording*
Disturb rec . **Start6-I**	*State of the module input:: Trigger event / start recording*
Disturb rec . **Start7-I**	*State of the module input:: Trigger event / start recording*
Disturb rec . **Start8-I**	*State of the module input:: Trigger event / start recording*
Fault rec . **Res all records**	*Signal: All records are being deleted. (Remark: Immediately afterwards, this signal becomes inactive again.)*
Trend rec . **Res all records**	*Signal: All records are being deleted. (Remark: Immediately afterwards, this signal becomes inactive again.)*
SSV . **System Error**	*Signal: Device Failure*
SSV . **SelfSuperVision Contact**	*Signal: SelfSuperVision Contact*
SSV . **New error**	*Signal: A new error message has been issued.*
SSV . **New warning**	*Signal: A new warning message has been issued.*
Syslog . **active**	*Signal: active*
Sys . **Smart view via USB**	*Information whether or not the Smart view access via the USB interface is activated (allowed).*
Sys . **Smart view via Eth**	*Information whether or not the Smart view access via the Ethernet interface is activated (allowed).*

1..n, Assignment List	Description
Scada . **SCADA connected**	*At least one SCADA System is connected to the device.*
Scada . **SCADA not connected**	*No SCADA System is connected to the device*
DNP3 . **busy**	*This message is set if the protocol is started. It will be reset if the protocol is shut down.*
DNP3 . **ready**	*The message will be set if the protocol is successfully started and ready for data exchange.*
DNP3 . **active**	*The communication with the Master (SCADA) is active.* *Note that for TCP/UDP, this state is permanently “Low” unless »DataLink confirm« is set to “Always”.*
DNP3 . **BinaryOutput0**	*Virtual Digital Output (DNP). This corresponds to a virtual binary input of the protective device.*
DNP3 . **BinaryOutput1**	*Virtual Digital Output (DNP). This corresponds to a virtual binary input of the protective device.*
DNP3 . **BinaryOutput2**	*Virtual Digital Output (DNP). This corresponds to a virtual binary input of the protective device.*
DNP3 . **BinaryOutput3**	*Virtual Digital Output (DNP). This corresponds to a virtual binary input of the protective device.*
DNP3 . **BinaryOutput4**	*Virtual Digital Output (DNP). This corresponds to a virtual binary input of the protective device.*
DNP3 . **BinaryOutput5**	*Virtual Digital Output (DNP). This corresponds to a virtual binary input of the protective device.*
DNP3 . **BinaryOutput6**	*Virtual Digital Output (DNP). This corresponds to a virtual binary input of the protective device.*
DNP3 . **BinaryOutput7**	*Virtual Digital Output (DNP). This corresponds to a virtual binary input of the protective device.*
DNP3 . **BinaryOutput8**	*Virtual Digital Output (DNP). This corresponds to a virtual binary input of the protective device.*
DNP3 . **BinaryOutput9**	*Virtual Digital Output (DNP). This corresponds to a virtual binary input of the protective device.*
DNP3 . **BinaryOutput10**	*Virtual Digital Output (DNP). This corresponds to a virtual binary input of the protective device.*
DNP3 . **BinaryOutput11**	*Virtual Digital Output (DNP). This corresponds to a virtual binary input of the protective device.*
DNP3 . **BinaryOutput12**	*Virtual Digital Output (DNP). This corresponds to a virtual binary input of the protective device.*
DNP3 . **BinaryOutput13**	*Virtual Digital Output (DNP). This corresponds to a virtual binary input of the protective device.*

1..n, Assignment List	Description
DNP3 . **BinaryOutput14**	*Virtual Digital Output (DNP). This corresponds to a virtual binary input of the protective device.*
DNP3 . **BinaryOutput15**	*Virtual Digital Output (DNP). This corresponds to a virtual binary input of the protective device.*
DNP3 . **BinaryOutput16**	*Virtual Digital Output (DNP). This corresponds to a virtual binary input of the protective device.*
DNP3 . **BinaryOutput17**	*Virtual Digital Output (DNP). This corresponds to a virtual binary input of the protective device.*
DNP3 . **BinaryOutput18**	*Virtual Digital Output (DNP). This corresponds to a virtual binary input of the protective device.*
DNP3 . **BinaryOutput19**	*Virtual Digital Output (DNP). This corresponds to a virtual binary input of the protective device.*
DNP3 . **BinaryOutput20**	*Virtual Digital Output (DNP). This corresponds to a virtual binary input of the protective device.*
DNP3 . **BinaryOutput21**	*Virtual Digital Output (DNP). This corresponds to a virtual binary input of the protective device.*
DNP3 . **BinaryOutput22**	*Virtual Digital Output (DNP). This corresponds to a virtual binary input of the protective device.*
DNP3 . **BinaryOutput23**	*Virtual Digital Output (DNP). This corresponds to a virtual binary input of the protective device.*
DNP3 . **BinaryOutput24**	*Virtual Digital Output (DNP). This corresponds to a virtual binary input of the protective device.*
DNP3 . **BinaryOutput25**	*Virtual Digital Output (DNP). This corresponds to a virtual binary input of the protective device.*
DNP3 . **BinaryOutput26**	*Virtual Digital Output (DNP). This corresponds to a virtual binary input of the protective device.*
DNP3 . **BinaryOutput27**	*Virtual Digital Output (DNP). This corresponds to a virtual binary input of the protective device.*
DNP3 . **BinaryOutput28**	*Virtual Digital Output (DNP). This corresponds to a virtual binary input of the protective device.*
DNP3 . **BinaryOutput29**	*Virtual Digital Output (DNP). This corresponds to a virtual binary input of the protective device.*
DNP3 . **BinaryOutput30**	*Virtual Digital Output (DNP). This corresponds to a virtual binary input of the protective device.*
DNP3 . **BinaryOutput31**	*Virtual Digital Output (DNP). This corresponds to a virtual binary input of the protective device.*
DNP3 . **BinaryInput0-I**	*Virtual Digital Input (DNP). This corresponds to a virtual binary output of the protective device.*
DNP3 . **BinaryInput1-I**	*Virtual Digital Input (DNP). This corresponds to a virtual binary output of the protective device.*

1..n, Assignment List	Description
DNP3 . **BinaryInput2-I**	*Virtual Digital Input (DNP). This corresponds to a virtual binary output of the protective device.*
DNP3 . **BinaryInput3-I**	*Virtual Digital Input (DNP). This corresponds to a virtual binary output of the protective device.*
DNP3 . **BinaryInput4-I**	*Virtual Digital Input (DNP). This corresponds to a virtual binary output of the protective device.*
DNP3 . **BinaryInput5-I**	*Virtual Digital Input (DNP). This corresponds to a virtual binary output of the protective device.*
DNP3 . **BinaryInput6-I**	*Virtual Digital Input (DNP). This corresponds to a virtual binary output of the protective device.*
DNP3 . **BinaryInput7-I**	*Virtual Digital Input (DNP). This corresponds to a virtual binary output of the protective device.*
DNP3 . **BinaryInput8-I**	*Virtual Digital Input (DNP). This corresponds to a virtual binary output of the protective device.*
DNP3 . **BinaryInput9-I**	*Virtual Digital Input (DNP). This corresponds to a virtual binary output of the protective device.*
DNP3 . **BinaryInput10-I**	*Virtual Digital Input (DNP). This corresponds to a virtual binary output of the protective device.*
DNP3 . **BinaryInput11-I**	*Virtual Digital Input (DNP). This corresponds to a virtual binary output of the protective device.*
DNP3 . **BinaryInput12-I**	*Virtual Digital Input (DNP). This corresponds to a virtual binary output of the protective device.*
DNP3 . **BinaryInput13-I**	*Virtual Digital Input (DNP). This corresponds to a virtual binary output of the protective device.*
DNP3 . **BinaryInput14-I**	*Virtual Digital Input (DNP). This corresponds to a virtual binary output of the protective device.*
DNP3 . **BinaryInput15-I**	*Virtual Digital Input (DNP). This corresponds to a virtual binary output of the protective device.*
DNP3 . **BinaryInput16-I**	*Virtual Digital Input (DNP). This corresponds to a virtual binary output of the protective device.*
DNP3 . **BinaryInput17-I**	*Virtual Digital Input (DNP). This corresponds to a virtual binary output of the protective device.*
DNP3 . **BinaryInput18-I**	*Virtual Digital Input (DNP). This corresponds to a virtual binary output of the protective device.*
DNP3 . **BinaryInput19-I**	*Virtual Digital Input (DNP). This corresponds to a virtual binary output of the protective device.*
DNP3 . **BinaryInput20-I**	*Virtual Digital Input (DNP). This corresponds to a virtual binary output of the protective device.*
DNP3 . **BinaryInput21-I**	*Virtual Digital Input (DNP). This corresponds to a virtual binary output of the protective device.*

1..n, Assignment List	Description
DNP3 . **BinaryInput22-I**	*Virtual Digital Input (DNP). This corresponds to a virtual binary output of the protective device.*
DNP3 . **BinaryInput23-I**	*Virtual Digital Input (DNP). This corresponds to a virtual binary output of the protective device.*
DNP3 . **BinaryInput24-I**	*Virtual Digital Input (DNP). This corresponds to a virtual binary output of the protective device.*
DNP3 . **BinaryInput25-I**	*Virtual Digital Input (DNP). This corresponds to a virtual binary output of the protective device.*
DNP3 . **BinaryInput26-I**	*Virtual Digital Input (DNP). This corresponds to a virtual binary output of the protective device.*
DNP3 . **BinaryInput27-I**	*Virtual Digital Input (DNP). This corresponds to a virtual binary output of the protective device.*
DNP3 . **BinaryInput28-I**	*Virtual Digital Input (DNP). This corresponds to a virtual binary output of the protective device.*
DNP3 . **BinaryInput29-I**	*Virtual Digital Input (DNP). This corresponds to a virtual binary output of the protective device.*
DNP3 . **BinaryInput30-I**	*Virtual Digital Input (DNP). This corresponds to a virtual binary output of the protective device.*
DNP3 . **BinaryInput31-I**	*Virtual Digital Input (DNP). This corresponds to a virtual binary output of the protective device.*
DNP3 . **BinaryInput32-I**	*Virtual Digital Input (DNP). This corresponds to a virtual binary output of the protective device.*
DNP3 . **BinaryInput33-I**	*Virtual Digital Input (DNP). This corresponds to a virtual binary output of the protective device.*
DNP3 . **BinaryInput34-I**	*Virtual Digital Input (DNP). This corresponds to a virtual binary output of the protective device.*
DNP3 . **BinaryInput35-I**	*Virtual Digital Input (DNP). This corresponds to a virtual binary output of the protective device.*
DNP3 . **BinaryInput36-I**	*Virtual Digital Input (DNP). This corresponds to a virtual binary output of the protective device.*
DNP3 . **BinaryInput37-I**	*Virtual Digital Input (DNP). This corresponds to a virtual binary output of the protective device.*
DNP3 . **BinaryInput38-I**	*Virtual Digital Input (DNP). This corresponds to a virtual binary output of the protective device.*
DNP3 . **BinaryInput39-I**	*Virtual Digital Input (DNP). This corresponds to a virtual binary output of the protective device.*
DNP3 . **BinaryInput40-I**	*Virtual Digital Input (DNP). This corresponds to a virtual binary output of the protective device.*
DNP3 . **BinaryInput41-I**	*Virtual Digital Input (DNP). This corresponds to a virtual binary output of the protective device.*

1..n, Assignment List	Description
DNP3 . **BinaryInput42-I**	*Virtual Digital Input (DNP). This corresponds to a virtual binary output of the protective device.*
DNP3 . **BinaryInput43-I**	*Virtual Digital Input (DNP). This corresponds to a virtual binary output of the protective device.*
DNP3 . **BinaryInput44-I**	*Virtual Digital Input (DNP). This corresponds to a virtual binary output of the protective device.*
DNP3 . **BinaryInput45-I**	*Virtual Digital Input (DNP). This corresponds to a virtual binary output of the protective device.*
DNP3 . **BinaryInput46-I**	*Virtual Digital Input (DNP). This corresponds to a virtual binary output of the protective device.*
DNP3 . **BinaryInput47-I**	*Virtual Digital Input (DNP). This corresponds to a virtual binary output of the protective device.*
DNP3 . **BinaryInput48-I**	*Virtual Digital Input (DNP). This corresponds to a virtual binary output of the protective device.*
DNP3 . **BinaryInput49-I**	*Virtual Digital Input (DNP). This corresponds to a virtual binary output of the protective device.*
DNP3 . **BinaryInput50-I**	*Virtual Digital Input (DNP). This corresponds to a virtual binary output of the protective device.*
DNP3 . **BinaryInput51-I**	*Virtual Digital Input (DNP). This corresponds to a virtual binary output of the protective device.*
DNP3 . **BinaryInput52-I**	*Virtual Digital Input (DNP). This corresponds to a virtual binary output of the protective device.*
DNP3 . **BinaryInput53-I**	*Virtual Digital Input (DNP). This corresponds to a virtual binary output of the protective device.*
DNP3 . **BinaryInput54-I**	*Virtual Digital Input (DNP). This corresponds to a virtual binary output of the protective device.*
DNP3 . **BinaryInput55-I**	*Virtual Digital Input (DNP). This corresponds to a virtual binary output of the protective device.*
DNP3 . **BinaryInput56-I**	*Virtual Digital Input (DNP). This corresponds to a virtual binary output of the protective device.*
DNP3 . **BinaryInput57-I**	*Virtual Digital Input (DNP). This corresponds to a virtual binary output of the protective device.*
DNP3 . **BinaryInput58-I**	*Virtual Digital Input (DNP). This corresponds to a virtual binary output of the protective device.*
DNP3 . **BinaryInput59-I**	*Virtual Digital Input (DNP). This corresponds to a virtual binary output of the protective device.*
DNP3 . **BinaryInput60-I**	*Virtual Digital Input (DNP). This corresponds to a virtual binary output of the protective device.*
DNP3 . **BinaryInput61-I**	*Virtual Digital Input (DNP). This corresponds to a virtual binary output of the protective device.*

1..n, Assignment List	Description
DNP3 . **BinaryInput62-I**	*Virtual Digital Input (DNP). This corresponds to a virtual binary output of the protective device.*
DNP3 . **BinaryInput63-I**	*Virtual Digital Input (DNP). This corresponds to a virtual binary output of the protective device.*
Modbus . **Transmission RTU**	*Signal: SCADA active*
Modbus . **Transmission TCP**	*Signal: SCADA active*
Modbus . **Scada Cmd 1**	*Scada Command*
Modbus . **Scada Cmd 2**	*Scada Command*
Modbus . **Scada Cmd 3**	*Scada Command*
Modbus . **Scada Cmd 4**	*Scada Command*
Modbus . **Scada Cmd 5**	*Scada Command*
Modbus . **Scada Cmd 6**	*Scada Command*
Modbus . **Scada Cmd 7**	*Scada Command*
Modbus . **Scada Cmd 8**	*Scada Command*
Modbus . **Scada Cmd 9**	*Scada Command*
Modbus . **Scada Cmd 10**	*Scada Command*
Modbus . **Scada Cmd 11**	*Scada Command*
Modbus . **Scada Cmd 12**	*Scada Command*
Modbus . **Scada Cmd 13**	*Scada Command*
Modbus . **Scada Cmd 14**	*Scada Command*
Modbus . **Scada Cmd 15**	*Scada Command*
Modbus . **Scada Cmd 16**	*Scada Command*
Modbus . **Config Bin Inp1-I**	*State of the module input: Config Bin Inp*
Modbus . **Config Bin Inp2-I**	*State of the module input: Config Bin Inp*
Modbus . **Config Bin Inp3-I**	*State of the module input: Config Bin Inp*
Modbus . **Config Bin Inp4-I**	*State of the module input: Config Bin Inp*
Modbus . **Config Bin Inp5-I**	*State of the module input: Config Bin Inp*
Modbus . **Config Bin Inp6-I**	*State of the module input: Config Bin Inp*

1..n, Assignment List	Description
Modbus . **Config Bin Inp7-I**	*State of the module input: Config Bin Inp*
Modbus . **Config Bin Inp8-I**	*State of the module input: Config Bin Inp*
Modbus . **Config Bin Inp9-I**	*State of the module input: Config Bin Inp*
Modbus . **Config Bin Inp10-I**	*State of the module input: Config Bin Inp*
Modbus . **Config Bin Inp11-I**	*State of the module input: Config Bin Inp*
Modbus . **Config Bin Inp12-I**	*State of the module input: Config Bin Inp*
Modbus . **Config Bin Inp13-I**	*State of the module input: Config Bin Inp*
Modbus . **Config Bin Inp14-I**	*State of the module input: Config Bin Inp*
Modbus . **Config Bin Inp15-I**	*State of the module input: Config Bin Inp*
Modbus . **Config Bin Inp16-I**	*State of the module input: Config Bin Inp*
Modbus . **Config Bin Inp17-I**	*State of the module input: Config Bin Inp*
Modbus . **Config Bin Inp18-I**	*State of the module input: Config Bin Inp*
Modbus . **Config Bin Inp19-I**	*State of the module input: Config Bin Inp*
Modbus . **Config Bin Inp20-I**	*State of the module input: Config Bin Inp*
Modbus . **Config Bin Inp21-I**	*State of the module input: Config Bin Inp*
Modbus . **Config Bin Inp22-I**	*State of the module input: Config Bin Inp*
Modbus . **Config Bin Inp23-I**	*State of the module input: Config Bin Inp*
Modbus . **Config Bin Inp24-I**	*State of the module input: Config Bin Inp*
Modbus . **Config Bin Inp25-I**	*State of the module input: Config Bin Inp*
Modbus . **Config Bin Inp26-I**	*State of the module input: Config Bin Inp*

1..n, Assignment List	Description
Modbus . **Config Bin Inp27-I**	*State of the module input: Config Bin Inp*
Modbus . **Config Bin Inp28-I**	*State of the module input: Config Bin Inp*
Modbus . **Config Bin Inp29-I**	*State of the module input: Config Bin Inp*
Modbus . **Config Bin Inp30-I**	*State of the module input: Config Bin Inp*
Modbus . **Config Bin Inp31-I**	*State of the module input: Config Bin Inp*
Modbus . **Config Bin Inp32-I**	*State of the module input: Config Bin Inp*
IEC 61850 . **MMS Client connected**	*At least one MMS client is connected to the device*
IEC 61850 . **All Goose Subscriber active**	*All Goose subscriber in the device are working*
IEC 61850 . **GOSINGGIO1.Ind1.stVal**	*Signal: Virtual Input (IEC61850 GGIO Ind): State*
IEC 61850 . **GOSINGGIO1.Ind2.stVal**	*Signal: Virtual Input (IEC61850 GGIO Ind): State*
IEC 61850 . **GOSINGGIO1.Ind3.stVal**	*Signal: Virtual Input (IEC61850 GGIO Ind): State*
IEC 61850 . **GOSINGGIO1.Ind4.stVal**	*Signal: Virtual Input (IEC61850 GGIO Ind): State*
IEC 61850 . **GOSINGGIO1.Ind5.stVal**	*Signal: Virtual Input (IEC61850 GGIO Ind): State*
IEC 61850 . **GOSINGGIO1.Ind6.stVal**	*Signal: Virtual Input (IEC61850 GGIO Ind): State*
IEC 61850 . **GOSINGGIO1.Ind7.stVal**	*Signal: Virtual Input (IEC61850 GGIO Ind): State*
IEC 61850 . **GOSINGGIO1.Ind8.stVal**	*Signal: Virtual Input (IEC61850 GGIO Ind): State*
IEC 61850 . **GOSINGGIO1.Ind9.stVal**	*Signal: Virtual Input (IEC61850 GGIO Ind): State*
IEC 61850 . **GOSINGGIO1.Ind10.stVal**	*Signal: Virtual Input (IEC61850 GGIO Ind): State*
IEC 61850 . **GOSINGGIO1.Ind11.stVal**	*Signal: Virtual Input (IEC61850 GGIO Ind): State*
IEC 61850 . **GOSINGGIO1.Ind12.stVal**	*Signal: Virtual Input (IEC61850 GGIO Ind): State*

1..n, Assignment List	Description
IEC 61850 . **GOSINGGIO1.Ind13.stVal**	*Signal: Virtual Input (IEC61850 GGIO Ind): State*
IEC 61850 . **GOSINGGIO1.Ind14.stVal**	*Signal: Virtual Input (IEC61850 GGIO Ind): State*
IEC 61850 . **GOSINGGIO1.Ind15.stVal**	*Signal: Virtual Input (IEC61850 GGIO Ind): State*
IEC 61850 . **GOSINGGIO1.Ind16.stVal**	*Signal: Virtual Input (IEC61850 GGIO Ind): State*
IEC 61850 . **GOSINGGIO1.Ind17.stVal**	*Signal: Virtual Input (IEC61850 GGIO Ind): State*
IEC 61850 . **GOSINGGIO1.Ind18.stVal**	*Signal: Virtual Input (IEC61850 GGIO Ind): State*
IEC 61850 . **GOSINGGIO1.Ind19.stVal**	*Signal: Virtual Input (IEC61850 GGIO Ind): State*
IEC 61850 . **GOSINGGIO1.Ind20.stVal**	*Signal: Virtual Input (IEC61850 GGIO Ind): State*
IEC 61850 . **GOSINGGIO1.Ind21.stVal**	*Signal: Virtual Input (IEC61850 GGIO Ind): State*
IEC 61850 . **GOSINGGIO1.Ind22.stVal**	*Signal: Virtual Input (IEC61850 GGIO Ind): State*
IEC 61850 . **GOSINGGIO1.Ind23.stVal**	*Signal: Virtual Input (IEC61850 GGIO Ind): State*
IEC 61850 . **GOSINGGIO1.Ind24.stVal**	*Signal: Virtual Input (IEC61850 GGIO Ind): State*
IEC 61850 . **GOSINGGIO1.Ind25.stVal**	*Signal: Virtual Input (IEC61850 GGIO Ind): State*
IEC 61850 . **GOSINGGIO1.Ind26.stVal**	*Signal: Virtual Input (IEC61850 GGIO Ind): State*
IEC 61850 . **GOSINGGIO1.Ind27.stVal**	*Signal: Virtual Input (IEC61850 GGIO Ind): State*
IEC 61850 . **GOSINGGIO1.Ind28.stVal**	*Signal: Virtual Input (IEC61850 GGIO Ind): State*
IEC 61850 . **GOSINGGIO1.Ind29.stVal**	*Signal: Virtual Input (IEC61850 GGIO Ind): State*
IEC 61850 . **GOSINGGIO1.Ind30.stVal**	*Signal: Virtual Input (IEC61850 GGIO Ind): State*
IEC 61850 . **GOSINGGIO1.Ind31.stVal**	*Signal: Virtual Input (IEC61850 GGIO Ind): State*
IEC 61850 . **GOSINGGIO1.Ind32.stVal**	*Signal: Virtual Input (IEC61850 GGIO Ind): State*

1..n, Assignment List	Description
IEC 61850 . **GOSINGGIO2.Ind1.stVal**	*Signal: Virtual Input (IEC61850 GGIO Ind): State*
IEC 61850 . **GOSINGGIO2.Ind2.stVal**	*Signal: Virtual Input (IEC61850 GGIO Ind): State*
IEC 61850 . **GOSINGGIO2.Ind3.stVal**	*Signal: Virtual Input (IEC61850 GGIO Ind): State*
IEC 61850 . **GOSINGGIO2.Ind4.stVal**	*Signal: Virtual Input (IEC61850 GGIO Ind): State*
IEC 61850 . **GOSINGGIO2.Ind5.stVal**	*Signal: Virtual Input (IEC61850 GGIO Ind): State*
IEC 61850 . **GOSINGGIO2.Ind6.stVal**	*Signal: Virtual Input (IEC61850 GGIO Ind): State*
IEC 61850 . **GOSINGGIO2.Ind7.stVal**	*Signal: Virtual Input (IEC61850 GGIO Ind): State*
IEC 61850 . **GOSINGGIO2.Ind8.stVal**	*Signal: Virtual Input (IEC61850 GGIO Ind): State*
IEC 61850 . **GOSINGGIO2.Ind9.stVal**	*Signal: Virtual Input (IEC61850 GGIO Ind): State*
IEC 61850 . **GOSINGGIO2.Ind10.stVal**	*Signal: Virtual Input (IEC61850 GGIO Ind): State*
IEC 61850 . **GOSINGGIO2.Ind11.stVal**	*Signal: Virtual Input (IEC61850 GGIO Ind): State*
IEC 61850 . **GOSINGGIO2.Ind12.stVal**	*Signal: Virtual Input (IEC61850 GGIO Ind): State*
IEC 61850 . **GOSINGGIO2.Ind13.stVal**	*Signal: Virtual Input (IEC61850 GGIO Ind): State*
IEC 61850 . **GOSINGGIO2.Ind14.stVal**	*Signal: Virtual Input (IEC61850 GGIO Ind): State*
IEC 61850 . **GOSINGGIO2.Ind15.stVal**	*Signal: Virtual Input (IEC61850 GGIO Ind): State*
IEC 61850 . **GOSINGGIO2.Ind16.stVal**	*Signal: Virtual Input (IEC61850 GGIO Ind): State*
IEC 61850 . **GOSINGGIO2.Ind17.stVal**	*Signal: Virtual Input (IEC61850 GGIO Ind): State*
IEC 61850 . **GOSINGGIO2.Ind18.stVal**	*Signal: Virtual Input (IEC61850 GGIO Ind): State*
IEC 61850 . **GOSINGGIO2.Ind19.stVal**	*Signal: Virtual Input (IEC61850 GGIO Ind): State*
IEC 61850 . **GOSINGGIO2.Ind20.stVal**	*Signal: Virtual Input (IEC61850 GGIO Ind): State*

1..n, Assignment List	Description
IEC 61850 . **GOSINGGIO2.Ind21.stVal**	*Signal: Virtual Input (IEC61850 GGIO Ind): State*
IEC 61850 . **GOSINGGIO2.Ind22.stVal**	*Signal: Virtual Input (IEC61850 GGIO Ind): State*
IEC 61850 . **GOSINGGIO2.Ind23.stVal**	*Signal: Virtual Input (IEC61850 GGIO Ind): State*
IEC 61850 . **GOSINGGIO2.Ind24.stVal**	*Signal: Virtual Input (IEC61850 GGIO Ind): State*
IEC 61850 . **GOSINGGIO2.Ind25.stVal**	*Signal: Virtual Input (IEC61850 GGIO Ind): State*
IEC 61850 . **GOSINGGIO2.Ind26.stVal**	*Signal: Virtual Input (IEC61850 GGIO Ind): State*
IEC 61850 . **GOSINGGIO2.Ind27.stVal**	*Signal: Virtual Input (IEC61850 GGIO Ind): State*
IEC 61850 . **GOSINGGIO2.Ind28.stVal**	*Signal: Virtual Input (IEC61850 GGIO Ind): State*
IEC 61850 . **GOSINGGIO2.Ind29.stVal**	*Signal: Virtual Input (IEC61850 GGIO Ind): State*
IEC 61850 . **GOSINGGIO2.Ind30.stVal**	*Signal: Virtual Input (IEC61850 GGIO Ind): State*
IEC 61850 . **GOSINGGIO2.Ind31.stVal**	*Signal: Virtual Input (IEC61850 GGIO Ind): State*
IEC 61850 . **GOSINGGIO2.Ind32.stVal**	*Signal: Virtual Input (IEC61850 GGIO Ind): State*
IEC 61850 . **GOSINGGIO1.Ind1.q**	*Signal: Virtual Input (IEC61850 GGIO Ind): Self-Supervision of the GGIO Input*
IEC 61850 . **GOSINGGIO1.Ind2.q**	*Signal: Virtual Input (IEC61850 GGIO Ind): Self-Supervision of the GGIO Input*
IEC 61850 . **GOSINGGIO1.Ind3.q**	*Signal: Virtual Input (IEC61850 GGIO Ind): Self-Supervision of the GGIO Input*
IEC 61850 . **GOSINGGIO1.Ind4.q**	*Signal: Virtual Input (IEC61850 GGIO Ind): Self-Supervision of the GGIO Input*
IEC 61850 . **GOSINGGIO1.Ind5.q**	*Signal: Virtual Input (IEC61850 GGIO Ind): Self-Supervision of the GGIO Input*
IEC 61850 . **GOSINGGIO1.Ind6.q**	*Signal: Virtual Input (IEC61850 GGIO Ind): Self-Supervision of the GGIO Input*
IEC 61850 . **GOSINGGIO1.Ind7.q**	*Signal: Virtual Input (IEC61850 GGIO Ind): Self-Supervision of the GGIO Input*
IEC 61850 . **GOSINGGIO1.Ind8.q**	*Signal: Virtual Input (IEC61850 GGIO Ind): Self-Supervision of the GGIO Input*

1..n, Assignment List	Description
IEC 61850 . **GOSINGGIO1.Ind9.q**	*Signal: Virtual Input (IEC61850 GGIO Ind): Self-Supervision of the GGIO Input*
IEC 61850 . **GOSINGGIO1.Ind10.q**	*Signal: Virtual Input (IEC61850 GGIO Ind): Self-Supervision of the GGIO Input*
IEC 61850 . **GOSINGGIO1.Ind11.q**	*Signal: Virtual Input (IEC61850 GGIO Ind): Self-Supervision of the GGIO Input*
IEC 61850 . **GOSINGGIO1.Ind12.q**	*Signal: Virtual Input (IEC61850 GGIO Ind): Self-Supervision of the GGIO Input*
IEC 61850 . **GOSINGGIO1.Ind13.q**	*Signal: Virtual Input (IEC61850 GGIO Ind): Self-Supervision of the GGIO Input*
IEC 61850 . **GOSINGGIO1.Ind14.q**	*Signal: Virtual Input (IEC61850 GGIO Ind): Self-Supervision of the GGIO Input*
IEC 61850 . **GOSINGGIO1.Ind15.q**	*Signal: Virtual Input (IEC61850 GGIO Ind): Self-Supervision of the GGIO Input*
IEC 61850 . **GOSINGGIO1.Ind16.q**	*Signal: Virtual Input (IEC61850 GGIO Ind): Self-Supervision of the GGIO Input*
IEC 61850 . **GOSINGGIO1.Ind17.q**	*Signal: Virtual Input (IEC61850 GGIO Ind): Self-Supervision of the GGIO Input*
IEC 61850 . **GOSINGGIO1.Ind18.q**	*Signal: Virtual Input (IEC61850 GGIO Ind): Self-Supervision of the GGIO Input*
IEC 61850 . **GOSINGGIO1.Ind19.q**	*Signal: Virtual Input (IEC61850 GGIO Ind): Self-Supervision of the GGIO Input*
IEC 61850 . **GOSINGGIO1.Ind20.q**	*Signal: Virtual Input (IEC61850 GGIO Ind): Self-Supervision of the GGIO Input*
IEC 61850 . **GOSINGGIO1.Ind21.q**	*Signal: Virtual Input (IEC61850 GGIO Ind): Self-Supervision of the GGIO Input*
IEC 61850 . **GOSINGGIO1.Ind22.q**	*Signal: Virtual Input (IEC61850 GGIO Ind): Self-Supervision of the GGIO Input*
IEC 61850 . **GOSINGGIO1.Ind23.q**	*Signal: Virtual Input (IEC61850 GGIO Ind): Self-Supervision of the GGIO Input*
IEC 61850 . **GOSINGGIO1.Ind24.q**	*Signal: Virtual Input (IEC61850 GGIO Ind): Self-Supervision of the GGIO Input*
IEC 61850 . **GOSINGGIO1.Ind25.q**	*Signal: Virtual Input (IEC61850 GGIO Ind): Self-Supervision of the GGIO Input*
IEC 61850 . **GOSINGGIO1.Ind26.q**	*Signal: Virtual Input (IEC61850 GGIO Ind): Self-Supervision of the GGIO Input*
IEC 61850 . **GOSINGGIO1.Ind27.q**	*Signal: Virtual Input (IEC61850 GGIO Ind): Self-Supervision of the GGIO Input*
IEC 61850 . **GOSINGGIO1.Ind28.q**	*Signal: Virtual Input (IEC61850 GGIO Ind): Self-Supervision of the GGIO Input*

1..n, Assignment List	Description
IEC 61850 . **GOSINGGIO1.Ind29.q**	*Signal: Virtual Input (IEC61850 GGIO Ind): Self-Supervision of the GGIO Input*
IEC 61850 . **GOSINGGIO1.Ind30.q**	*Signal: Virtual Input (IEC61850 GGIO Ind): Self-Supervision of the GGIO Input*
IEC 61850 . **GOSINGGIO1.Ind31.q**	*Signal: Virtual Input (IEC61850 GGIO Ind): Self-Supervision of the GGIO Input*
IEC 61850 . **GOSINGGIO1.Ind32.q**	*Signal: Virtual Input (IEC61850 GGIO Ind): Self-Supervision of the GGIO Input*
IEC 61850 . **GOSINGGIO2.Ind1.q**	*Signal: Virtual Input (IEC61850 GGIO Ind): Self-Supervision of the GGIO Input*
IEC 61850 . **GOSINGGIO2.Ind2.q**	*Signal: Virtual Input (IEC61850 GGIO Ind): Self-Supervision of the GGIO Input*
IEC 61850 . **GOSINGGIO2.Ind3.q**	*Signal: Virtual Input (IEC61850 GGIO Ind): Self-Supervision of the GGIO Input*
IEC 61850 . **GOSINGGIO2.Ind4.q**	*Signal: Virtual Input (IEC61850 GGIO Ind): Self-Supervision of the GGIO Input*
IEC 61850 . **GOSINGGIO2.Ind5.q**	*Signal: Virtual Input (IEC61850 GGIO Ind): Self-Supervision of the GGIO Input*
IEC 61850 . **GOSINGGIO2.Ind6.q**	*Signal: Virtual Input (IEC61850 GGIO Ind): Self-Supervision of the GGIO Input*
IEC 61850 . **GOSINGGIO2.Ind7.q**	*Signal: Virtual Input (IEC61850 GGIO Ind): Self-Supervision of the GGIO Input*
IEC 61850 . **GOSINGGIO2.Ind8.q**	*Signal: Virtual Input (IEC61850 GGIO Ind): Self-Supervision of the GGIO Input*
IEC 61850 . **GOSINGGIO2.Ind9.q**	*Signal: Virtual Input (IEC61850 GGIO Ind): Self-Supervision of the GGIO Input*
IEC 61850 . **GOSINGGIO2.Ind10.q**	*Signal: Virtual Input (IEC61850 GGIO Ind): Self-Supervision of the GGIO Input*
IEC 61850 . **GOSINGGIO2.Ind11.q**	*Signal: Virtual Input (IEC61850 GGIO Ind): Self-Supervision of the GGIO Input*
IEC 61850 . **GOSINGGIO2.Ind12.q**	*Signal: Virtual Input (IEC61850 GGIO Ind): Self-Supervision of the GGIO Input*
IEC 61850 . **GOSINGGIO2.Ind13.q**	*Signal: Virtual Input (IEC61850 GGIO Ind): Self-Supervision of the GGIO Input*
IEC 61850 . **GOSINGGIO2.Ind14.q**	*Signal: Virtual Input (IEC61850 GGIO Ind): Self-Supervision of the GGIO Input*
IEC 61850 . **GOSINGGIO2.Ind15.q**	*Signal: Virtual Input (IEC61850 GGIO Ind): Self-Supervision of the GGIO Input*
IEC 61850 . **GOSINGGIO2.Ind16.q**	*Signal: Virtual Input (IEC61850 GGIO Ind): Self-Supervision of the GGIO Input*

1..n, Assignment List	Description
IEC 61850 . **GOSINGGIO2.Ind17.q**	*Signal: Virtual Input (IEC61850 GGIO Ind): Self-Supervision of the GGIO Input*
IEC 61850 . **GOSINGGIO2.Ind18.q**	*Signal: Virtual Input (IEC61850 GGIO Ind): Self-Supervision of the GGIO Input*
IEC 61850 . **GOSINGGIO2.Ind19.q**	*Signal: Virtual Input (IEC61850 GGIO Ind): Self-Supervision of the GGIO Input*
IEC 61850 . **GOSINGGIO2.Ind20.q**	*Signal: Virtual Input (IEC61850 GGIO Ind): Self-Supervision of the GGIO Input*
IEC 61850 . **GOSINGGIO2.Ind21.q**	*Signal: Virtual Input (IEC61850 GGIO Ind): Self-Supervision of the GGIO Input*
IEC 61850 . **GOSINGGIO2.Ind22.q**	*Signal: Virtual Input (IEC61850 GGIO Ind): Self-Supervision of the GGIO Input*
IEC 61850 . **GOSINGGIO2.Ind23.q**	*Signal: Virtual Input (IEC61850 GGIO Ind): Self-Supervision of the GGIO Input*
IEC 61850 . **GOSINGGIO2.Ind24.q**	*Signal: Virtual Input (IEC61850 GGIO Ind): Self-Supervision of the GGIO Input*
IEC 61850 . **GOSINGGIO2.Ind25.q**	*Signal: Virtual Input (IEC61850 GGIO Ind): Self-Supervision of the GGIO Input*
IEC 61850 . **GOSINGGIO2.Ind26.q**	*Signal: Virtual Input (IEC61850 GGIO Ind): Self-Supervision of the GGIO Input*
IEC 61850 . **GOSINGGIO2.Ind27.q**	*Signal: Virtual Input (IEC61850 GGIO Ind): Self-Supervision of the GGIO Input*
IEC 61850 . **GOSINGGIO2.Ind28.q**	*Signal: Virtual Input (IEC61850 GGIO Ind): Self-Supervision of the GGIO Input*
IEC 61850 . **GOSINGGIO2.Ind29.q**	*Signal: Virtual Input (IEC61850 GGIO Ind): Self-Supervision of the GGIO Input*
IEC 61850 . **GOSINGGIO2.Ind30.q**	*Signal: Virtual Input (IEC61850 GGIO Ind): Self-Supervision of the GGIO Input*
IEC 61850 . **GOSINGGIO2.Ind31.q**	*Signal: Virtual Input (IEC61850 GGIO Ind): Self-Supervision of the GGIO Input*
IEC 61850 . **GOSINGGIO2.Ind32.q**	*Signal: Virtual Input (IEC61850 GGIO Ind): Self-Supervision of the GGIO Input*
IEC 61850 . **SPCSO1**	*Status bit that can be set by clients like e.g. SCADA (Single Point Controllable Status Output).*
IEC 61850 . **SPCSO2**	*Status bit that can be set by clients like e.g. SCADA (Single Point Controllable Status Output).*
IEC 61850 . **SPCSO3**	*Status bit that can be set by clients like e.g. SCADA (Single Point Controllable Status Output).*
IEC 61850 . **SPCSO4**	*Status bit that can be set by clients like e.g. SCADA (Single Point Controllable Status Output).*

1..n, Assignment List	Description
IEC 61850 . **SPCSO5**	*Status bit that can be set by clients like e.g. SCADA (Single Point Controllable Status Output).*
IEC 61850 . **SPCSO6**	*Status bit that can be set by clients like e.g. SCADA (Single Point Controllable Status Output).*
IEC 61850 . **SPCSO7**	*Status bit that can be set by clients like e.g. SCADA (Single Point Controllable Status Output).*
IEC 61850 . **SPCSO8**	*Status bit that can be set by clients like e.g. SCADA (Single Point Controllable Status Output).*
IEC 61850 . **SPCSO9**	*Status bit that can be set by clients like e.g. SCADA (Single Point Controllable Status Output).*
IEC 61850 . **SPCSO10**	*Status bit that can be set by clients like e.g. SCADA (Single Point Controllable Status Output).*
IEC 61850 . **SPCSO11**	*Status bit that can be set by clients like e.g. SCADA (Single Point Controllable Status Output).*
IEC 61850 . **SPCSO12**	*Status bit that can be set by clients like e.g. SCADA (Single Point Controllable Status Output).*
IEC 61850 . **SPCSO13**	*Status bit that can be set by clients like e.g. SCADA (Single Point Controllable Status Output).*
IEC 61850 . **SPCSO14**	*Status bit that can be set by clients like e.g. SCADA (Single Point Controllable Status Output).*
IEC 61850 . **SPCSO15**	*Status bit that can be set by clients like e.g. SCADA (Single Point Controllable Status Output).*
IEC 61850 . **SPCSO16**	*Status bit that can be set by clients like e.g. SCADA (Single Point Controllable Status Output).*
IEC 61850 . **SPCSO17**	*Status bit that can be set by clients like e.g. SCADA (Single Point Controllable Status Output).*
IEC 61850 . **SPCSO18**	*Status bit that can be set by clients like e.g. SCADA (Single Point Controllable Status Output).*
IEC 61850 . **SPCSO19**	*Status bit that can be set by clients like e.g. SCADA (Single Point Controllable Status Output).*
IEC 61850 . **SPCSO20**	*Status bit that can be set by clients like e.g. SCADA (Single Point Controllable Status Output).*
IEC 61850 . **SPCSO21**	*Status bit that can be set by clients like e.g. SCADA (Single Point Controllable Status Output).*
IEC 61850 . **SPCSO22**	*Status bit that can be set by clients like e.g. SCADA (Single Point Controllable Status Output).*
IEC 61850 . **SPCSO23**	*Status bit that can be set by clients like e.g. SCADA (Single Point Controllable Status Output).*
IEC 61850 . **SPCSO24**	*Status bit that can be set by clients like e.g. SCADA (Single Point Controllable Status Output).*

1..n, Assignment List	Description
IEC 61850 . **SPCSO25**	*Status bit that can be set by clients like e.g. SCADA (Single Point Controllable Status Output).*
IEC 61850 . **SPCSO26**	*Status bit that can be set by clients like e.g. SCADA (Single Point Controllable Status Output).*
IEC 61850 . **SPCSO27**	*Status bit that can be set by clients like e.g. SCADA (Single Point Controllable Status Output).*
IEC 61850 . **SPCSO28**	*Status bit that can be set by clients like e.g. SCADA (Single Point Controllable Status Output).*
IEC 61850 . **SPCSO29**	*Status bit that can be set by clients like e.g. SCADA (Single Point Controllable Status Output).*
IEC 61850 . **SPCSO30**	*Status bit that can be set by clients like e.g. SCADA (Single Point Controllable Status Output).*
IEC 61850 . **SPCSO31**	*Status bit that can be set by clients like e.g. SCADA (Single Point Controllable Status Output).*
IEC 61850 . **SPCSO32**	*Status bit that can be set by clients like e.g. SCADA (Single Point Controllable Status Output).*
IEC103 . **Scada Cmd 1**	*Scada Command*
IEC103 . **Scada Cmd 2**	*Scada Command*
IEC103 . **Scada Cmd 3**	*Scada Command*
IEC103 . **Scada Cmd 4**	*Scada Command*
IEC103 . **Scada Cmd 5**	*Scada Command*
IEC103 . **Scada Cmd 6**	*Scada Command*
IEC103 . **Scada Cmd 7**	*Scada Command*
IEC103 . **Scada Cmd 8**	*Scada Command*
IEC103 . **Scada Cmd 9**	*Scada Command*
IEC103 . **Scada Cmd 10**	*Scada Command*
IEC103 . **Transmission**	*Signal: SCADA active*
IEC103 . **Failure Event lost**	*Failure event lost*
IEC103 . **Test mode active**	*Signal: IEC103 communication has been switched over into Test Mode.*
IEC103 . **Block MD active**	*Signal: The blocking of IEC103 transmission in monitor direction has been activated.*
IEC103 . **Ex activate test mode-I**	*Module input state: Test Mode of the IEC103 communication.*
IEC103 . **Ex activate Block MD-I**	*Module input state: Activation of the blocking of IEC103 transmission in monitor direction.*

1..n, Assignment List	Description
IEC104 . **busy**	*This message is set if the protocol is started. It will be reset if the protocol is shut down.*
IEC104 . **ready**	*The message will be set if the protocol is successfully started and ready for data exchange.*
IEC104 . **Transmission**	*Signal: SCADA active*
IEC104 . **Failure Event lost**	*Failure event lost*
IEC104 . **Scada Cmd 1**	*Scada Command*
IEC104 . **Scada Cmd 2**	*Scada Command*
IEC104 . **Scada Cmd 3**	*Scada Command*
IEC104 . **Scada Cmd 4**	*Scada Command*
IEC104 . **Scada Cmd 5**	*Scada Command*
IEC104 . **Scada Cmd 6**	*Scada Command*
IEC104 . **Scada Cmd 7**	*Scada Command*
IEC104 . **Scada Cmd 8**	*Scada Command*
IEC104 . **Scada Cmd 9**	*Scada Command*
IEC104 . **Scada Cmd 10**	*Scada Command*
IEC104 . **Scada Cmd 11**	*Scada Command*
IEC104 . **Scada Cmd 12**	*Scada Command*
IEC104 . **Scada Cmd 13**	*Scada Command*
IEC104 . **Scada Cmd 14**	*Scada Command*
IEC104 . **Scada Cmd 15**	*Scada Command*
IEC104 . **Scada Cmd 16**	*Scada Command*
Profibus . **Data OK**	*Data within the Input field are OK (Yes=1)*
Profibus . **SubModul Err**	*Assignable Signal, Failure in Sub-Module, Communication Failure.*
Profibus . **Connection active**	*Connection active*
Profibus . **Scada Cmd 1**	*Scada Command*
Profibus . **Scada Cmd 2**	*Scada Command*
Profibus . **Scada Cmd 3**	*Scada Command*
Profibus . **Scada Cmd 4**	*Scada Command*
Profibus . **Scada Cmd 5**	*Scada Command*
Profibus . **Scada Cmd 6**	*Scada Command*

1..n, Assignment List	Description
Profibus . **Scada Cmd 7**	*Scada Command*
Profibus . **Scada Cmd 8**	*Scada Command*
Profibus . **Scada Cmd 9**	*Scada Command*
Profibus . **Scada Cmd 10**	*Scada Command*
Profibus . **Scada Cmd 11**	*Scada Command*
Profibus . **Scada Cmd 12**	*Scada Command*
Profibus . **Scada Cmd 13**	*Scada Command*
Profibus . **Scada Cmd 14**	*Scada Command*
Profibus . **Scada Cmd 15**	*Scada Command*
Profibus . **Scada Cmd 16**	*Scada Command*
IRIG-B . **IRIG-B active**	*Signal: If there is no valid IRIG-B signal for 60 sec, IRIG-B is regarded as inactive.*
IRIG-B . **High-Low Invert**	*Signal: The High and Low signals of the IRIG-B are inverted. This does NOT mean that the wiring is faulty. If the wiring is faulty no IRIG-B signal will be detected.*
IRIG-B . **Control Signal1**	*Signal: IRIG-B Control Signal. The external IRIG-B generator can set these signals. They can be used for further control procedures inside the device (e.g. logic funtions).*
IRIG-B . **Control Signal2**	*Signal: IRIG-B Control Signal. The external IRIG-B generator can set these signals. They can be used for further control procedures inside the device (e.g. logic funtions).*
IRIG-B . **Control Signal3**	*Signal: IRIG-B Control Signal. The external IRIG-B generator can set these signals. They can be used for further control procedures inside the device (e.g. logic funtions).*
IRIG-B . **Control Signal4**	*Signal: IRIG-B Control Signal. The external IRIG-B generator can set these signals. They can be used for further control procedures inside the device (e.g. logic funtions).*
IRIG-B . **Control Signal5**	*Signal: IRIG-B Control Signal. The external IRIG-B generator can set these signals. They can be used for further control procedures inside the device (e.g. logic funtions).*
IRIG-B . **Control Signal6**	*Signal: IRIG-B Control Signal. The external IRIG-B generator can set these signals. They can be used for further control procedures inside the device (e.g. logic funtions).*
IRIG-B . **Control Signal7**	*Signal: IRIG-B Control Signal. The external IRIG-B generator can set these signals. They can be used for further control procedures inside the device (e.g. logic funtions).*
IRIG-B . **Control Signal8**	*Signal: IRIG-B Control Signal. The external IRIG-B generator can set these signals. They can be used for further control procedures inside the device (e.g. logic funtions).*

1..n, Assignment List	Description
IRIG-B . **Control Signal9**	*Signal: IRIG-B Control Signal. The external IRIG-B generator can set these signals. They can be used for further control procedures inside the device (e.g. logic funtions).*
IRIG-B . **Control Signal10**	*Signal: IRIG-B Control Signal. The external IRIG-B generator can set these signals. They can be used for further control procedures inside the device (e.g. logic funtions).*
IRIG-B . **Control Signal11**	*Signal: IRIG-B Control Signal. The external IRIG-B generator can set these signals. They can be used for further control procedures inside the device (e.g. logic funtions).*
IRIG-B . **Control Signal12**	*Signal: IRIG-B Control Signal. The external IRIG-B generator can set these signals. They can be used for further control procedures inside the device (e.g. logic funtions).*
IRIG-B . **Control Signal13**	*Signal: IRIG-B Control Signal. The external IRIG-B generator can set these signals. They can be used for further control procedures inside the device (e.g. logic funtions).*
IRIG-B . **Control Signal14**	*Signal: IRIG-B Control Signal. The external IRIG-B generator can set these signals. They can be used for further control procedures inside the device (e.g. logic funtions).*
IRIG-B . **Control Signal15**	*Signal: IRIG-B Control Signal. The external IRIG-B generator can set these signals. They can be used for further control procedures inside the device (e.g. logic funtions).*
IRIG-B . **Control Signal16**	*Signal: IRIG-B Control Signal. The external IRIG-B generator can set these signals. They can be used for further control procedures inside the device (e.g. logic funtions).*
IRIG-B . **Control Signal17**	*Signal: IRIG-B Control Signal. The external IRIG-B generator can set these signals. They can be used for further control procedures inside the device (e.g. logic funtions).*
IRIG-B . **Control Signal18**	*Signal: IRIG-B Control Signal. The external IRIG-B generator can set these signals. They can be used for further control procedures inside the device (e.g. logic funtions).*
SNTP . **SNTP active**	*Signal: If there is no valid SNTP signal for 120 sec, SNTP is regarded as inactive.*
TimeSync . **synchronized**	*Clock is synchronized.*
Statistics . **ResFc all**	*Signal: Resetting of all Statistic values (Current Demand, Power Demand, Min, Max)*
Statistics . **ResFc Vavg**	*Signal: Resetting of the sliding average calculation.*
Statistics . **ResFc Max**	*Signal: Resetting of all Maximum values*
Statistics . **ResFc Min**	*Signal: Resetting of all Minimum values*
Statistics . **StartFc Vavg-I**	*State of the module input: Start of Statistics Average Voltage*
Logics . **LE1.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE1.Timer Out**	*Signal: Timer Output*

1..n, Assignment List	Description
Logics . **LE1.Out**	*Signal: Latched Output (Q)*
Logics . **LE1.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE1.Gate In1-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE1.Gate In2-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE1.Gate In3-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE1.Gate In4-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE1.Reset Latch-I**	*State of the module input: Reset Signal for the Latching*
Logics . **LE2.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE2.Timer Out**	*Signal: Timer Output*
Logics . **LE2.Out**	*Signal: Latched Output (Q)*
Logics . **LE2.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE2.Gate In1-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE2.Gate In2-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE2.Gate In3-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE2.Gate In4-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE2.Reset Latch-I**	*State of the module input: Reset Signal for the Latching*
Logics . **LE3.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE3.Timer Out**	*Signal: Timer Output*
Logics . **LE3.Out**	*Signal: Latched Output (Q)*
Logics . **LE3.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE3.Gate In1-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE3.Gate In2-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE3.Gate In3-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE3.Gate In4-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE3.Reset Latch-I**	*State of the module input: Reset Signal for the Latching*
Logics . **LE4.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE4.Timer Out**	*Signal: Timer Output*
Logics . **LE4.Out**	*Signal: Latched Output (Q)*

1..n, Assignment List	Description
Logics . **LE4.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE4.Gate In1-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE4.Gate In2-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE4.Gate In3-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE4.Gate In4-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE4.Reset Latch-I**	*State of the module input: Reset Signal for the Latching*
Logics . **LE5.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE5.Timer Out**	*Signal: Timer Output*
Logics . **LE5.Out**	*Signal: Latched Output (Q)*
Logics . **LE5.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE5.Gate In1-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE5.Gate In2-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE5.Gate In3-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE5.Gate In4-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE5.Reset Latch-I**	*State of the module input: Reset Signal for the Latching*
Logics . **LE6.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE6.Timer Out**	*Signal: Timer Output*
Logics . **LE6.Out**	*Signal: Latched Output (Q)*
Logics . **LE6.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE6.Gate In1-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE6.Gate In2-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE6.Gate In3-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE6.Gate In4-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE6.Reset Latch-I**	*State of the module input: Reset Signal for the Latching*
Logics . **LE7.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE7.Timer Out**	*Signal: Timer Output*
Logics . **LE7.Out**	*Signal: Latched Output (Q)*
Logics . **LE7.Out inverted**	*Signal: Negated Latched Output (Q NOT)*

1..n, Assignment List	Description
Logics . **LE7.Gate In1-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE7.Gate In2-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE7.Gate In3-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE7.Gate In4-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE7.Reset Latch-I**	*State of the module input: Reset Signal for the Latching*
Logics . **LE8.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE8.Timer Out**	*Signal: Timer Output*
Logics . **LE8.Out**	*Signal: Latched Output (Q)*
Logics . **LE8.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE8.Gate In1-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE8.Gate In2-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE8.Gate In3-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE8.Gate In4-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE8.Reset Latch-I**	*State of the module input: Reset Signal for the Latching*
Logics . **LE9.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE9.Timer Out**	*Signal: Timer Output*
Logics . **LE9.Out**	*Signal: Latched Output (Q)*
Logics . **LE9.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE9.Gate In1-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE9.Gate In2-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE9.Gate In3-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE9.Gate In4-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE9.Reset Latch-I**	*State of the module input: Reset Signal for the Latching*
Logics . **LE10.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE10.Timer Out**	*Signal: Timer Output*
Logics . **LE10.Out**	*Signal: Latched Output (Q)*
Logics . **LE10.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE10.Gate In1-I**	*State of the module input: Assignment of the Input Signal*

1..n, Assignment List	Description
Logics . **LE10.Gate In2-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE10.Gate In3-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE10.Gate In4-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE10.Reset Latch-I**	*State of the module input: Reset Signal for the Latching*
Logics . **LE11.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE11.Timer Out**	*Signal: Timer Output*
Logics . **LE11.Out**	*Signal: Latched Output (Q)*
Logics . **LE11.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE11.Gate In1-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE11.Gate In2-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE11.Gate In3-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE11.Gate In4-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE11.Reset Latch-I**	*State of the module input: Reset Signal for the Latching*
Logics . **LE12.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE12.Timer Out**	*Signal: Timer Output*
Logics . **LE12.Out**	*Signal: Latched Output (Q)*
Logics . **LE12.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE12.Gate In1-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE12.Gate In2-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE12.Gate In3-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE12.Gate In4-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE12.Reset Latch-I**	*State of the module input: Reset Signal for the Latching*
Logics . **LE13.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE13.Timer Out**	*Signal: Timer Output*
Logics . **LE13.Out**	*Signal: Latched Output (Q)*
Logics . **LE13.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE13.Gate In1-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE13.Gate In2-I**	*State of the module input: Assignment of the Input Signal*

1..n, Assignment List	Description
Logics . **LE13.Gate In3-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE13.Gate In4-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE13.Reset Latch-I**	*State of the module input: Reset Signal for the Latching*
Logics . **LE14.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE14.Timer Out**	*Signal: Timer Output*
Logics . **LE14.Out**	*Signal: Latched Output (Q)*
Logics . **LE14.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE14.Gate In1-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE14.Gate In2-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE14.Gate In3-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE14.Gate In4-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE14.Reset Latch-I**	*State of the module input: Reset Signal for the Latching*
Logics . **LE15.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE15.Timer Out**	*Signal: Timer Output*
Logics . **LE15.Out**	*Signal: Latched Output (Q)*
Logics . **LE15.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE15.Gate In1-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE15.Gate In2-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE15.Gate In3-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE15.Gate In4-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE15.Reset Latch-I**	*State of the module input: Reset Signal for the Latching*
Logics . **LE16.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE16.Timer Out**	*Signal: Timer Output*
Logics . **LE16.Out**	*Signal: Latched Output (Q)*
Logics . **LE16.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE16.Gate In1-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE16.Gate In2-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE16.Gate In3-I**	*State of the module input: Assignment of the Input Signal*

1..n, Assignment List	Description
Logics . **LE16.Gate In4-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE16.Reset Latch-I**	*State of the module input: Reset Signal for the Latching*
Logics . **LE17.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE17.Timer Out**	*Signal: Timer Output*
Logics . **LE17.Out**	*Signal: Latched Output (Q)*
Logics . **LE17.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE17.Gate In1-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE17.Gate In2-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE17.Gate In3-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE17.Gate In4-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE17.Reset Latch-I**	*State of the module input: Reset Signal for the Latching*
Logics . **LE18.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE18.Timer Out**	*Signal: Timer Output*
Logics . **LE18.Out**	*Signal: Latched Output (Q)*
Logics . **LE18.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE18.Gate In1-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE18.Gate In2-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE18.Gate In3-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE18.Gate In4-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE18.Reset Latch-I**	*State of the module input: Reset Signal for the Latching*
Logics . **LE19.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE19.Timer Out**	*Signal: Timer Output*
Logics . **LE19.Out**	*Signal: Latched Output (Q)*
Logics . **LE19.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE19.Gate In1-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE19.Gate In2-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE19.Gate In3-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE19.Gate In4-I**	*State of the module input: Assignment of the Input Signal*

1..n, Assignment List	Description
Logics . **LE19.Reset Latch-I**	*State of the module input: Reset Signal for the Latching*
Logics . **LE20.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE20.Timer Out**	*Signal: Timer Output*
Logics . **LE20.Out**	*Signal: Latched Output (Q)*
Logics . **LE20.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE20.Gate In1-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE20.Gate In2-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE20.Gate In3-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE20.Gate In4-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE20.Reset Latch-I**	*State of the module input: Reset Signal for the Latching*
Logics . **LE21.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE21.Timer Out**	*Signal: Timer Output*
Logics . **LE21.Out**	*Signal: Latched Output (Q)*
Logics . **LE21.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE21.Gate In1-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE21.Gate In2-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE21.Gate In3-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE21.Gate In4-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE21.Reset Latch-I**	*State of the module input: Reset Signal for the Latching*
Logics . **LE22.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE22.Timer Out**	*Signal: Timer Output*
Logics . **LE22.Out**	*Signal: Latched Output (Q)*
Logics . **LE22.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE22.Gate In1-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE22.Gate In2-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE22.Gate In3-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE22.Gate In4-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE22.Reset Latch-I**	*State of the module input: Reset Signal for the Latching*

1..n, Assignment List	Description
Logics . **LE23.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE23.Timer Out**	*Signal: Timer Output*
Logics . **LE23.Out**	*Signal: Latched Output (Q)*
Logics . **LE23.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE23.Gate In1-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE23.Gate In2-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE23.Gate In3-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE23.Gate In4-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE23.Reset Latch-I**	*State of the module input: Reset Signal for the Latching*
Logics . **LE24.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE24.Timer Out**	*Signal: Timer Output*
Logics . **LE24.Out**	*Signal: Latched Output (Q)*
Logics . **LE24.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE24.Gate In1-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE24.Gate In2-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE24.Gate In3-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE24.Gate In4-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE24.Reset Latch-I**	*State of the module input: Reset Signal for the Latching*
Logics . **LE25.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE25.Timer Out**	*Signal: Timer Output*
Logics . **LE25.Out**	*Signal: Latched Output (Q)*
Logics . **LE25.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE25.Gate In1-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE25.Gate In2-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE25.Gate In3-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE25.Gate In4-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE25.Reset Latch-I**	*State of the module input: Reset Signal for the Latching*
Logics . **LE26.Gate Out**	*Signal: Output of the logic gate*

1..n, Assignment List	Description
Logics . **LE26.Timer Out**	*Signal: Timer Output*
Logics . **LE26.Out**	*Signal: Latched Output (Q)*
Logics . **LE26.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE26.Gate In1-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE26.Gate In2-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE26.Gate In3-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE26.Gate In4-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE26.Reset Latch-I**	*State of the module input: Reset Signal for the Latching*
Logics . **LE27.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE27.Timer Out**	*Signal: Timer Output*
Logics . **LE27.Out**	*Signal: Latched Output (Q)*
Logics . **LE27.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE27.Gate In1-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE27.Gate In2-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE27.Gate In3-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE27.Gate In4-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE27.Reset Latch-I**	*State of the module input: Reset Signal for the Latching*
Logics . **LE28.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE28.Timer Out**	*Signal: Timer Output*
Logics . **LE28.Out**	*Signal: Latched Output (Q)*
Logics . **LE28.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE28.Gate In1-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE28.Gate In2-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE28.Gate In3-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE28.Gate In4-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE28.Reset Latch-I**	*State of the module input: Reset Signal for the Latching*
Logics . **LE29.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE29.Timer Out**	*Signal: Timer Output*

1..n, Assignment List	Description
Logics . **LE29.Out**	*Signal: Latched Output (Q)*
Logics . **LE29.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE29.Gate In1-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE29.Gate In2-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE29.Gate In3-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE29.Gate In4-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE29.Reset Latch-I**	*State of the module input: Reset Signal for the Latching*
Logics . **LE30.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE30.Timer Out**	*Signal: Timer Output*
Logics . **LE30.Out**	*Signal: Latched Output (Q)*
Logics . **LE30.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE30.Gate In1-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE30.Gate In2-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE30.Gate In3-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE30.Gate In4-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE30.Reset Latch-I**	*State of the module input: Reset Signal for the Latching*
Logics . **LE31.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE31.Timer Out**	*Signal: Timer Output*
Logics . **LE31.Out**	*Signal: Latched Output (Q)*
Logics . **LE31.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE31.Gate In1-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE31.Gate In2-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE31.Gate In3-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE31.Gate In4-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE31.Reset Latch-I**	*State of the module input: Reset Signal for the Latching*
Logics . **LE32.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE32.Timer Out**	*Signal: Timer Output*
Logics . **LE32.Out**	*Signal: Latched Output (Q)*

1..n, Assignment List	Description
Logics . **LE32.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE32.Gate In1-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE32.Gate In2-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE32.Gate In3-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE32.Gate In4-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE32.Reset Latch-I**	*State of the module input: Reset Signal for the Latching*
Logics . **LE33.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE33.Timer Out**	*Signal: Timer Output*
Logics . **LE33.Out**	*Signal: Latched Output (Q)*
Logics . **LE33.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE33.Gate In1-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE33.Gate In2-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE33.Gate In3-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE33.Gate In4-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE33.Reset Latch-I**	*State of the module input: Reset Signal for the Latching*
Logics . **LE34.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE34.Timer Out**	*Signal: Timer Output*
Logics . **LE34.Out**	*Signal: Latched Output (Q)*
Logics . **LE34.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE34.Gate In1-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE34.Gate In2-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE34.Gate In3-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE34.Gate In4-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE34.Reset Latch-I**	*State of the module input: Reset Signal for the Latching*
Logics . **LE35.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE35.Timer Out**	*Signal: Timer Output*
Logics . **LE35.Out**	*Signal: Latched Output (Q)*
Logics . **LE35.Out inverted**	*Signal: Negated Latched Output (Q NOT)*

1..n, Assignment List	Description
Logics . **LE35.Gate In1-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE35.Gate In2-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE35.Gate In3-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE35.Gate In4-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE35.Reset Latch-I**	*State of the module input: Reset Signal for the Latching*
Logics . **LE36.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE36.Timer Out**	*Signal: Timer Output*
Logics . **LE36.Out**	*Signal: Latched Output (Q)*
Logics . **LE36.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE36.Gate In1-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE36.Gate In2-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE36.Gate In3-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE36.Gate In4-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE36.Reset Latch-I**	*State of the module input: Reset Signal for the Latching*
Logics . **LE37.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE37.Timer Out**	*Signal: Timer Output*
Logics . **LE37.Out**	*Signal: Latched Output (Q)*
Logics . **LE37.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE37.Gate In1-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE37.Gate In2-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE37.Gate In3-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE37.Gate In4-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE37.Reset Latch-I**	*State of the module input: Reset Signal for the Latching*
Logics . **LE38.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE38.Timer Out**	*Signal: Timer Output*
Logics . **LE38.Out**	*Signal: Latched Output (Q)*
Logics . **LE38.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE38.Gate In1-I**	*State of the module input: Assignment of the Input Signal*

1..n, Assignment List	Description
Logics . **LE38.Gate In2-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE38.Gate In3-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE38.Gate In4-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE38.Reset Latch-I**	*State of the module input: Reset Signal for the Latching*
Logics . **LE39.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE39.Timer Out**	*Signal: Timer Output*
Logics . **LE39.Out**	*Signal: Latched Output (Q)*
Logics . **LE39.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE39.Gate In1-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE39.Gate In2-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE39.Gate In3-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE39.Gate In4-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE39.Reset Latch-I**	*State of the module input: Reset Signal for the Latching*
Logics . **LE40.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE40.Timer Out**	*Signal: Timer Output*
Logics . **LE40.Out**	*Signal: Latched Output (Q)*
Logics . **LE40.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE40.Gate In1-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE40.Gate In2-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE40.Gate In3-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE40.Gate In4-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE40.Reset Latch-I**	*State of the module input: Reset Signal for the Latching*
Logics . **LE41.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE41.Timer Out**	*Signal: Timer Output*
Logics . **LE41.Out**	*Signal: Latched Output (Q)*
Logics . **LE41.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE41.Gate In1-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE41.Gate In2-I**	*State of the module input: Assignment of the Input Signal*

1..n, Assignment List	Description
Logics . **LE41.Gate In3-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE41.Gate In4-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE41.Reset Latch-I**	*State of the module input: Reset Signal for the Latching*
Logics . **LE42.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE42.Timer Out**	*Signal: Timer Output*
Logics . **LE42.Out**	*Signal: Latched Output (Q)*
Logics . **LE42.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE42.Gate In1-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE42.Gate In2-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE42.Gate In3-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE42.Gate In4-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE42.Reset Latch-I**	*State of the module input: Reset Signal for the Latching*
Logics . **LE43.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE43.Timer Out**	*Signal: Timer Output*
Logics . **LE43.Out**	*Signal: Latched Output (Q)*
Logics . **LE43.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE43.Gate In1-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE43.Gate In2-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE43.Gate In3-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE43.Gate In4-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE43.Reset Latch-I**	*State of the module input: Reset Signal for the Latching*
Logics . **LE44.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE44.Timer Out**	*Signal: Timer Output*
Logics . **LE44.Out**	*Signal: Latched Output (Q)*
Logics . **LE44.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE44.Gate In1-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE44.Gate In2-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE44.Gate In3-I**	*State of the module input: Assignment of the Input Signal*

1..n, Assignment List	Description
Logics . **LE44.Gate In4-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE44.Reset Latch-I**	*State of the module input: Reset Signal for the Latching*
Logics . **LE45.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE45.Timer Out**	*Signal: Timer Output*
Logics . **LE45.Out**	*Signal: Latched Output (Q)*
Logics . **LE45.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE45.Gate In1-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE45.Gate In2-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE45.Gate In3-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE45.Gate In4-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE45.Reset Latch-I**	*State of the module input: Reset Signal for the Latching*
Logics . **LE46.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE46.Timer Out**	*Signal: Timer Output*
Logics . **LE46.Out**	*Signal: Latched Output (Q)*
Logics . **LE46.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE46.Gate In1-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE46.Gate In2-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE46.Gate In3-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE46.Gate In4-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE46.Reset Latch-I**	*State of the module input: Reset Signal for the Latching*
Logics . **LE47.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE47.Timer Out**	*Signal: Timer Output*
Logics . **LE47.Out**	*Signal: Latched Output (Q)*
Logics . **LE47.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE47.Gate In1-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE47.Gate In2-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE47.Gate In3-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE47.Gate In4-I**	*State of the module input: Assignment of the Input Signal*

1..n, Assignment List	Description
Logics . **LE47.Reset Latch-I**	*State of the module input: Reset Signal for the Latching*
Logics . **LE48.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE48.Timer Out**	*Signal: Timer Output*
Logics . **LE48.Out**	*Signal: Latched Output (Q)*
Logics . **LE48.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE48.Gate In1-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE48.Gate In2-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE48.Gate In3-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE48.Gate In4-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE48.Reset Latch-I**	*State of the module input: Reset Signal for the Latching*
Logics . **LE49.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE49.Timer Out**	*Signal: Timer Output*
Logics . **LE49.Out**	*Signal: Latched Output (Q)*
Logics . **LE49.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE49.Gate In1-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE49.Gate In2-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE49.Gate In3-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE49.Gate In4-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE49.Reset Latch-I**	*State of the module input: Reset Signal for the Latching*
Logics . **LE50.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE50.Timer Out**	*Signal: Timer Output*
Logics . **LE50.Out**	*Signal: Latched Output (Q)*
Logics . **LE50.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE50.Gate In1-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE50.Gate In2-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE50.Gate In3-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE50.Gate In4-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE50.Reset Latch-I**	*State of the module input: Reset Signal for the Latching*

1..n, Assignment List	Description
Logics . **LE51.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE51.Timer Out**	*Signal: Timer Output*
Logics . **LE51.Out**	*Signal: Latched Output (Q)*
Logics . **LE51.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE51.Gate In1-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE51.Gate In2-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE51.Gate In3-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE51.Gate In4-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE51.Reset Latch-I**	*State of the module input: Reset Signal for the Latching*
Logics . **LE52.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE52.Timer Out**	*Signal: Timer Output*
Logics . **LE52.Out**	*Signal: Latched Output (Q)*
Logics . **LE52.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE52.Gate In1-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE52.Gate In2-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE52.Gate In3-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE52.Gate In4-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE52.Reset Latch-I**	*State of the module input: Reset Signal for the Latching*
Logics . **LE53.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE53.Timer Out**	*Signal: Timer Output*
Logics . **LE53.Out**	*Signal: Latched Output (Q)*
Logics . **LE53.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE53.Gate In1-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE53.Gate In2-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE53.Gate In3-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE53.Gate In4-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE53.Reset Latch-I**	*State of the module input: Reset Signal for the Latching*
Logics . **LE54.Gate Out**	*Signal: Output of the logic gate*

1..n, Assignment List	Description
Logics . **LE54.Timer Out**	*Signal: Timer Output*
Logics . **LE54.Out**	*Signal: Latched Output (Q)*
Logics . **LE54.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE54.Gate In1-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE54.Gate In2-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE54.Gate In3-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE54.Gate In4-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE54.Reset Latch-I**	*State of the module input: Reset Signal for the Latching*
Logics . **LE55.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE55.Timer Out**	*Signal: Timer Output*
Logics . **LE55.Out**	*Signal: Latched Output (Q)*
Logics . **LE55.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE55.Gate In1-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE55.Gate In2-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE55.Gate In3-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE55.Gate In4-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE55.Reset Latch-I**	*State of the module input: Reset Signal for the Latching*
Logics . **LE56.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE56.Timer Out**	*Signal: Timer Output*
Logics . **LE56.Out**	*Signal: Latched Output (Q)*
Logics . **LE56.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE56.Gate In1-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE56.Gate In2-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE56.Gate In3-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE56.Gate In4-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE56.Reset Latch-I**	*State of the module input: Reset Signal for the Latching*
Logics . **LE57.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE57.Timer Out**	*Signal: Timer Output*

1..n, Assignment List	Description
Logics . **LE57.Out**	*Signal: Latched Output (Q)*
Logics . **LE57.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE57.Gate In1-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE57.Gate In2-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE57.Gate In3-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE57.Gate In4-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE57.Reset Latch-I**	*State of the module input: Reset Signal for the Latching*
Logics . **LE58.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE58.Timer Out**	*Signal: Timer Output*
Logics . **LE58.Out**	*Signal: Latched Output (Q)*
Logics . **LE58.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE58.Gate In1-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE58.Gate In2-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE58.Gate In3-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE58.Gate In4-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE58.Reset Latch-I**	*State of the module input: Reset Signal for the Latching*
Logics . **LE59.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE59.Timer Out**	*Signal: Timer Output*
Logics . **LE59.Out**	*Signal: Latched Output (Q)*
Logics . **LE59.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE59.Gate In1-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE59.Gate In2-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE59.Gate In3-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE59.Gate In4-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE59.Reset Latch-I**	*State of the module input: Reset Signal for the Latching*
Logics . **LE60.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE60.Timer Out**	*Signal: Timer Output*
Logics . **LE60.Out**	*Signal: Latched Output (Q)*

1..n, Assignment List	Description
Logics . **LE60.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE60.Gate In1-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE60.Gate In2-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE60.Gate In3-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE60.Gate In4-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE60.Reset Latch-I**	*State of the module input: Reset Signal for the Latching*
Logics . **LE61.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE61.Timer Out**	*Signal: Timer Output*
Logics . **LE61.Out**	*Signal: Latched Output (Q)*
Logics . **LE61.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE61.Gate In1-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE61.Gate In2-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE61.Gate In3-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE61.Gate In4-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE61.Reset Latch-I**	*State of the module input: Reset Signal for the Latching*
Logics . **LE62.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE62.Timer Out**	*Signal: Timer Output*
Logics . **LE62.Out**	*Signal: Latched Output (Q)*
Logics . **LE62.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE62.Gate In1-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE62.Gate In2-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE62.Gate In3-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE62.Gate In4-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE62.Reset Latch-I**	*State of the module input: Reset Signal for the Latching*
Logics . **LE63.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE63.Timer Out**	*Signal: Timer Output*
Logics . **LE63.Out**	*Signal: Latched Output (Q)*
Logics . **LE63.Out inverted**	*Signal: Negated Latched Output (Q NOT)*

1..n, Assignment List	Description
Logics . **LE63.Gate In1-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE63.Gate In2-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE63.Gate In3-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE63.Gate In4-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE63.Reset Latch-I**	*State of the module input: Reset Signal for the Latching*
Logics . **LE64.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE64.Timer Out**	*Signal: Timer Output*
Logics . **LE64.Out**	*Signal: Latched Output (Q)*
Logics . **LE64.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE64.Gate In1-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE64.Gate In2-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE64.Gate In3-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE64.Gate In4-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE64.Reset Latch-I**	*State of the module input: Reset Signal for the Latching*
Logics . **LE65.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE65.Timer Out**	*Signal: Timer Output*
Logics . **LE65.Out**	*Signal: Latched Output (Q)*
Logics . **LE65.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE65.Gate In1-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE65.Gate In2-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE65.Gate In3-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE65.Gate In4-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE65.Reset Latch-I**	*State of the module input: Reset Signal for the Latching*
Logics . **LE66.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE66.Timer Out**	*Signal: Timer Output*
Logics . **LE66.Out**	*Signal: Latched Output (Q)*
Logics . **LE66.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE66.Gate In1-I**	*State of the module input: Assignment of the Input Signal*

1..n, Assignment List	Description
Logics . **LE66.Gate In2-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE66.Gate In3-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE66.Gate In4-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE66.Reset Latch-I**	*State of the module input: Reset Signal for the Latching*
Logics . **LE67.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE67.Timer Out**	*Signal: Timer Output*
Logics . **LE67.Out**	*Signal: Latched Output (Q)*
Logics . **LE67.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE67.Gate In1-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE67.Gate In2-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE67.Gate In3-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE67.Gate In4-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE67.Reset Latch-I**	*State of the module input: Reset Signal for the Latching*
Logics . **LE68.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE68.Timer Out**	*Signal: Timer Output*
Logics . **LE68.Out**	*Signal: Latched Output (Q)*
Logics . **LE68.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE68.Gate In1-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE68.Gate In2-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE68.Gate In3-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE68.Gate In4-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE68.Reset Latch-I**	*State of the module input: Reset Signal for the Latching*
Logics . **LE69.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE69.Timer Out**	*Signal: Timer Output*
Logics . **LE69.Out**	*Signal: Latched Output (Q)*
Logics . **LE69.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE69.Gate In1-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE69.Gate In2-I**	*State of the module input: Assignment of the Input Signal*

1..n, Assignment List	Description
Logics . **LE69.Gate In3-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE69.Gate In4-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE69.Reset Latch-I**	*State of the module input: Reset Signal for the Latching*
Logics . **LE70.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE70.Timer Out**	*Signal: Timer Output*
Logics . **LE70.Out**	*Signal: Latched Output (Q)*
Logics . **LE70.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE70.Gate In1-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE70.Gate In2-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE70.Gate In3-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE70.Gate In4-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE70.Reset Latch-I**	*State of the module input: Reset Signal for the Latching*
Logics . **LE71.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE71.Timer Out**	*Signal: Timer Output*
Logics . **LE71.Out**	*Signal: Latched Output (Q)*
Logics . **LE71.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE71.Gate In1-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE71.Gate In2-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE71.Gate In3-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE71.Gate In4-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE71.Reset Latch-I**	*State of the module input: Reset Signal for the Latching*
Logics . **LE72.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE72.Timer Out**	*Signal: Timer Output*
Logics . **LE72.Out**	*Signal: Latched Output (Q)*
Logics . **LE72.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE72.Gate In1-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE72.Gate In2-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE72.Gate In3-I**	*State of the module input: Assignment of the Input Signal*

1..n, Assignment List	Description
Logics . **LE72.Gate In4-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE72.Reset Latch-I**	*State of the module input: Reset Signal for the Latching*
Logics . **LE73.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE73.Timer Out**	*Signal: Timer Output*
Logics . **LE73.Out**	*Signal: Latched Output (Q)*
Logics . **LE73.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE73.Gate In1-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE73.Gate In2-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE73.Gate In3-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE73.Gate In4-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE73.Reset Latch-I**	*State of the module input: Reset Signal for the Latching*
Logics . **LE74.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE74.Timer Out**	*Signal: Timer Output*
Logics . **LE74.Out**	*Signal: Latched Output (Q)*
Logics . **LE74.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE74.Gate In1-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE74.Gate In2-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE74.Gate In3-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE74.Gate In4-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE74.Reset Latch-I**	*State of the module input: Reset Signal for the Latching*
Logics . **LE75.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE75.Timer Out**	*Signal: Timer Output*
Logics . **LE75.Out**	*Signal: Latched Output (Q)*
Logics . **LE75.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE75.Gate In1-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE75.Gate In2-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE75.Gate In3-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE75.Gate In4-I**	*State of the module input: Assignment of the Input Signal*

1..n, Assignment List	Description
Logics . **LE75.Reset Latch-I**	*State of the module input: Reset Signal for the Latching*
Logics . **LE76.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE76.Timer Out**	*Signal: Timer Output*
Logics . **LE76.Out**	*Signal: Latched Output (Q)*
Logics . **LE76.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE76.Gate In1-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE76.Gate In2-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE76.Gate In3-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE76.Gate In4-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE76.Reset Latch-I**	*State of the module input: Reset Signal for the Latching*
Logics . **LE77.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE77.Timer Out**	*Signal: Timer Output*
Logics . **LE77.Out**	*Signal: Latched Output (Q)*
Logics . **LE77.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE77.Gate In1-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE77.Gate In2-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE77.Gate In3-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE77.Gate In4-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE77.Reset Latch-I**	*State of the module input: Reset Signal for the Latching*
Logics . **LE78.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE78.Timer Out**	*Signal: Timer Output*
Logics . **LE78.Out**	*Signal: Latched Output (Q)*
Logics . **LE78.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE78.Gate In1-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE78.Gate In2-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE78.Gate In3-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE78.Gate In4-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE78.Reset Latch-I**	*State of the module input: Reset Signal for the Latching*

1..n, Assignment List	Description
Logics . **LE79.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE79.Timer Out**	*Signal: Timer Output*
Logics . **LE79.Out**	*Signal: Latched Output (Q)*
Logics . **LE79.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE79.Gate In1-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE79.Gate In2-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE79.Gate In3-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE79.Gate In4-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE79.Reset Latch-I**	*State of the module input: Reset Signal for the Latching*
Logics . **LE80.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE80.Timer Out**	*Signal: Timer Output*
Logics . **LE80.Out**	*Signal: Latched Output (Q)*
Logics . **LE80.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE80.Gate In1-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE80.Gate In2-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE80.Gate In3-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE80.Gate In4-I**	*State of the module input: Assignment of the Input Signal*
Logics . **LE80.Reset Latch-I**	*State of the module input: Reset Signal for the Latching*
Sgen . **Manual Start**	*Fault Simulation has been started manually.*
Sgen . **Manual Stop**	*Fault Simulation has been stopped manually.*
Sgen . **Running**	*Signal; Measuring value simulation is running*
Sgen . **Started**	*Fault Simulation has been started*
Sgen . **Stopped**	*Fault Simulation has been stopped*
Sgen . **Ex Start Simulation-I**	*State of the module input:External Start of Fault Simulation (Using the test parameters)*
Sgen . **ExBlo1-I**	*Module input state: External blocking1*
Sgen . **ExBlo2-I**	*Module input state: External blocking2*
Sgen . **Ex ForcePost-I**	*State of the module input:Force Post state. Abort simulation.*
Sys . **PS 1**	*Signal: The currently active Parameter Set is PS 1*
Sys . **PS 2**	*Signal: The currently active Parameter Set is PS 2*

1..n, Assignment List	Description
Sys . **PS 3**	*Signal: The currently active Parameter Set is PS 3*
Sys . **PS 4**	*Signal: The currently active Parameter Set is PS 4*
Sys . **PSS manual**	*Signal: Manual Switch over of a Parameter Set*
Sys . **PSS via Scada**	*Signal: Parameter Set Switch via Scada. Write into this output byte the integer of the parameter set that should become active (e.g. 4 => Switch onto parameter set 4).*
Sys . **PSS via Inp fct**	*Signal: Parameter Set Switch via input function*
Sys . **min 1 param changed**	*Signal: At least one parameter has been changed*
Sys . **Setting Lock Bypass**	*Signal: Short-period unlock of the Setting Lock*
Sys . **Ack LED**	*Signal: LEDs acknowledgement*
Sys . **Ack BO**	*Signal: Acknowledgement of the Binary Outputs*
Sys . **Ack Scada**	*Signal: Acknowledge latched SCADA signals*
Sys . **Ack TripCmd**	*Signal: Reset Trip Command*
Sys . **Ack LED-HMI**	*Signal: LEDs acknowledgement :HMI*
Sys . **Ack BO-HMI**	*Signal: Acknowledgement of the Binary Outputs :HMI*
Sys . **Ack Scada-HMI**	*Signal: Acknowledge latched SCADA signals :HMI*
Sys . **Ack TripCmd-HMI**	*Signal: Reset Trip Command :HMI*
Sys . **Ack LED-Sca**	*Signal: LEDs acknowledgement :SCADA*
Sys . **Ack BO-Sca**	*Signal: Acknowledgement of the Binary Outputs :SCADA*
Sys . **Ack Counter-Sca**	*Signal: Reset of all Counters :SCADA*
Sys . **Ack Scada-Sca**	*Signal: Acknowledge latched SCADA signals :SCADA*
Sys . **Ack TripCmd-Sca**	*Signal: Reset Trip Command :SCADA*
Sys . **Res OperationsCr**	*Signal:: Res OperationsCr*
Sys . **Res AlarmCr**	*Signal:: Res AlarmCr*
Sys . **Res TripCmdCr**	*Signal:: Res TripCmdCr*
Sys . **Res TotalCr**	*Signal:: Res TotalCr*
Sys . **Ack LED-I**	*Module input state: LEDs acknowledgement by digital input*
Sys . **Ack BO-I**	*Module input state: Acknowledgement of the binary Output Relays*
Sys . **Ack Scada-I**	*Module input state: Acknowledge latched SCADA signals.*
Sys . **PS1-I**	*State of the module input respectively of the signal, that should activate this Parameter Setting Group.*

1..n, Assignment List	Description
Sys . **PS2-I**	*State of the module input respectively of the signal, that should activate this Parameter Setting Group.*
Sys . **PS3-I**	*State of the module input respectively of the signal, that should activate this Parameter Setting Group.*
Sys . **PS4-I**	*State of the module input respectively of the signal, that should activate this Parameter Setting Group.*
Sys . **Setting Lock-I**	*State of the module input: No parameters can be changed as long as this input is true. The parameter settings are locked.*
Sys . **Internal test state**	*Auxiliary state for testing purposes.*

Mode

general operation mode

Selection list referenced by the following parameters:

- ⮡ LEDs group A . Latched
- ⮡ LEDs group A . Latched
- ⮡ LEDs group A . Latched
- ⮡ LEDs group A . Latched
- ⮡ LEDs group A . Latched
- ⮡ LEDs group A . Latched
- *[. . .]*

Mode	Description
inactive	*inactive*
active	*active*
active, ack. by alarm	*Latching of LEDs is active, but will be acknowledged (reset) automatically (by a protection function) in case of a new alarm.*

LED active color

Selection list referenced by the following parameters:

- ⮡ LEDs group A . LED active color
- ⮡ LEDs group A . LED inactive color

- ⮡ LEDs group A . LED active color
- ⮡ LEDs group A . LED inactive color
- ⮡ LEDs group A . LED active color
- ⮡ LEDs group A . LED inactive color
- *[...]*

LED active color	Description
green	*green*
red	*red*
red flash	*red flashing*
green flash	*green blinking*
“-”	*No assignment*

Ack via »C« key

Select which acknowledgeable elements can be reset via pressing the »C« key.

Selection list referenced by the following parameters:

- ⮡ Sys . Ack via »C« key

Ack via »C« key	Description
Nothing	*No elements can be simply reset via pressing the »C« key for a long time (ca. 1 second). This has the consequence that pressing the »C« key is only a shortcut to the Acknowledge menu, from which the user has to select the elements to be reset.*
Ack LEDs w/o passw.	*All LEDs are acknowledged (reset) via pressing the »C« key for ca. 1 second. No password has to be entered for this. The reset activity can be recognized from the fact that it always includes an LED test, i.e. all LEDs flash in red color for a second, then flash in green color for a second.*
Ack LEDs	*All LEDs are reset via pressing the »C« key (for ca. 1 second). The reset activity can be recognized from the fact that it always includes an LED test, i.e. all LEDs flash in red color for a second, then flash in green color for a second.*
Ack LEDs and relays	*All LEDs and all acknowledgeable binary output relays are reset via pressing the »C« key (for ca. 1 second). The reset activity can be recognized from the fact that it always includes an LED test, i.e. all LEDs flash in red color for a second, then flash in green color for a second.*
Ack Everything	*All acknowledgeable elements are reset via pressing the »C« key (for ca. 1 second):*

Ack via »C« key	Description
	- All LEDs, and *- all binary output relays, and* *- all latched SCADA signals, and* *- the Trip command.* *The reset activity can be recognized from the fact that it always includes an LED test, i.e. all LEDs flash in red color for a second, then flash in green color for a second.*

Duration

Recording time

Selection list referenced by the following parameters:

- ⮡ Statistics . Start Vavg via:

Duration	Description
Duration	*Recording time*
StartFct	*Start function*

Duration

Recording time

Selection list referenced by the following parameters:

- ⮡ Statistics . Duration Vavg

Duration	Description
2 s	*s*
5 s	*s*
10 s	*s*
15 s	*seconds*
30 s	*seconds*
1 min	*minute*
5 min	*minute*

Duration	Description
10 min	*minute*
15 min	*minute*
30 min	*minute*
1 h	*Hours*
2 h	*Hours*
6 h	*Hours*
12 h	*Hours*
1 d	*days*
2 d	*days*
5 d	*days*
7 d	*days*
10 d	*days*
30 d	*days*

Window configuration

Selection list referenced by the following parameters:

- ⮡ Statistics . Window Vavg

Window configuration	Description
sliding	*Moving mean: Continuously the newest measuring value is added and the oldest measuring value is removed from the moving mean (average value).*
fixed	*The average value is calculated for a fixed window.*

Selection

Selection list referenced by the following parameters:

- ⮡ HMI . Menu language

Selection	Description
English	*English*

Selection	Description
German	*German*
Russian	*Russian*
Polish	*Polish*
French	*French*
Portuguese	*Portuguese*
Spanish	*Spanish*
Romanian	*Romanian*

Record-Mode

Recorder Mode (Set the behaviour of the recorder)

Selection list referenced by the following parameters:

- ⮡ Fault rec . Record-Mode

Record-Mode	Description
Alarms and Trips	*A recording is started in case of an alarm or a trip.*
Trips only	*A recording is started only in case of a trip.*

Resolution

Resolution (recording frequency)

Selection list referenced by the following parameters:

- ⮡ Trend rec . Resolution

Resolution	Description
60 min	*Add next entry: 60 min*
30 min	*Add next entry: 30 min*
15 min	*Add next entry: 15 min*
10 min	*Add next entry: 10 min*
5 min	*Add next entry: 5 min*

1..n, TrendRecList

Selection list referenced by the following parameters:

- ⮡ DNP3 . Analog value 0
- ⮡ Modbus . Mapped Meas 1
- ⮡ Trend rec . Trend1
- ⮡ Trend rec . Trend2
- ⮡ Trend rec . Trend3
- ⮡ Trend rec . Trend4
- *[. . .]*

1..n, TrendRecList	Description
“-”	*No assignment*
VT . **VL1**	*Measured value: Phase-to-neutral voltage (fundamental)*
VT . **VL2**	*Measured value: Phase-to-neutral voltage (fundamental)*
VT . **VL3**	*Measured value: Phase-to-neutral voltage (fundamental)*
VT . **VX meas**	*Measured value (measured): VX measured (fundamental)*
VT . **VG calc**	*Measured value (calculated): VG (fundamental)*
VT . **VL12**	*Measured value: Phase-to-phase voltage (fundamental)*
VT . **VL23**	*Measured value: Phase-to-phase voltage (fundamental)*
VT . **VL31**	*Measured value: Phase-to-phase voltage (fundamental)*
VT . **VL1 RMS**	*Measured value: Phase-to-neutral voltage (RMS)*
VT . **VL2 RMS**	*Measured value: Phase-to-neutral voltage (RMS)*
VT . **VL3 RMS**	*Measured value: Phase-to-neutral voltage (RMS)*
VT . **VX meas RMS**	*Measured value (measured): VX measured (RMS)*
VT . **VG calc RMS**	*Measured value (calculated): VG (RMS)*
VT . **VL12 RMS**	*Measured value: Phase-to-phase voltage (RMS)*
VT . **VL23 RMS**	*Measured value: Phase-to-phase voltage (RMS)*
VT . **VL31 RMS**	*Measured value: Phase-to-phase voltage (RMS)*
VT . **V0**	*Measured value (calculated): Symmetrical components Zero voltage(fundamental)*
VT . **V1**	*Measured value (calculated): Symmetrical components positive phase sequence voltage(fundamental)*

1..n, TrendRecList	Description
VT . **V2**	*Measured value (calculated): Symmetrical components negative phase sequence voltage(fundamental)*
VT . **%(V2/V1)**	*Measured value (calculated): V2/V1, phase sequence will be taken into account automatically.*
VT . **VL1 avg RMS**	*VL1 average value (RMS)*
VT . **VL2 avg RMS**	*VL2 average value (RMS)*
VT . **VL3 avg RMS**	*VL3 average value (RMS)*
VT . **VL12 avg RMS**	*VL12 average value (RMS)*
VT . **VL23 avg RMS**	*VL23 average value (RMS)*
VT . **VL31 avg RMS**	*VL31 average value (RMS)*
VT . **f**	*Measured value: Frequency*
VT . **VL1 THD**	*Measured value (calculated): VL1 Total Harmonic Distortion*
VT . **VL2 THD**	*Measured value (calculated): VL2 Total Harmonic Distortion*
VT . **VL3 THD**	*Measured value (calculated): VL3 Total Harmonic Distortion*
VT . **VL12 THD**	*Measured value (calculated): V12 Total Harmonic Distortion*
VT . **VL23 THD**	*Measured value (calculated): V23 Total Harmonic Distortion*
VT . **VL31 THD**	*Measured value (calculated): V31 Total Harmonic Distortion*

1..n, OnOffList

Selection list referenced by the following parameters:

- ⮡ IEC 61850 . Function

1..n, OnOffList	Description
inactive	*inactive*
active	*active*

Baud rate

Selection list referenced by the following parameters:

- ⮡ DNP3 . Baud rate

Baud rate	Description
1200	*1200*
2400	*2400*
4800	*4800*
9600	*9600*
19200	*19200*
38400	*38400*
57600	*57600*
115200	*115200*

Byte Frame

Selection list referenced by the following parameters:

- ⮡ DNP3 . Frame Layout

Byte Frame	Description
8E1	*8 data bits, even parity, 1 stopbit.*
8O1	*8 data bits, odd, 1 stopbit.*
8N1	*8 data bits, no parity, 1 stopbit.*
8N2	*8 data bits, no parity, 2 stopbits.*

Optical rest position

Selection list referenced by the following parameters:

- ⮡ DNP3 . Optical rest position

Optical rest position	Description
Light off	*Light off*
Light on	*Light on*

Communication Start Variants

Selection list referenced by the following parameters:

- ⮡ DNP3 . DataLink confirm

Communication Start Variants	Description
Never	*Option Never is recommended*
Always	*If this variable is set to Always then LinkLayer needs to establish a connection before sending any Frame.*
On_Large	*If set to On_Large then a connection needs to be established before sending the first Frame of a multi Term Message*

_AL_ResponseType_k

_AL_ResponseType_h

Selection list referenced by the following parameters:

- ⮡ DNP3 . AppLink confirm

_AL_ResponseType_k	Description
Never	*Never*
Always	*Always*
Event	*Event*

1..n, Assignment List

Assignment List

Selection list referenced by the following parameters:

- ⮡ DNP3 . DoubleBitInput 0

1..n, Assignment List	Description
“-”	*No assignment*
SG[1] . **Pos**	*Signal: Circuit Breaker Position (0 = Indeterminate, 1 = OFF, 2 = ON, 3 = Disturbed)*

1..n, Assignment List

Assignment List

Selection list referenced by the following parameters:

- ⮡ DNP3 . BinaryCounter 0

1..n, Assignment List	Description
“-”	*No assignment*
Prot . **FaultNo**	*Fault number*
Prot . **No. of Grid Fault**	*Number of grid fault: A grid fault, e.g. a short circuit, might cause several faults with trip and autoreclosing; in this case, the fault number counts each fault, but the grid fault number remains the same.*
SG[1] . **TripCmd Cr**	*Counter: Total number of trips of the switchgear.*
LVRT[1] . **NumOf Vdips in t-LVRT**	*Number of Voltage dips during t-LVRT*
LVRT[1] . **Cr Tot Numb of Vdips**	*Counter Total number of voltage dips.*
LVRT[1] . **Cr Tot Numb of Vdips to Trip**	*Counter Total number of voltage dips that caused a Trip.*
LVRT[2] . **NumOf Vdips in t-LVRT**	*Number of Voltage dips during t-LVRT*
LVRT[2] . **Cr Tot Numb of Vdips**	*Counter Total number of voltage dips.*
LVRT[2] . **Cr Tot Numb of Vdips to Trip**	*Counter Total number of voltage dips that caused a Trip.*
Sys . **Operating hours Cr**	*Operating hours counter of the protective device*

Scale Factor

Multiplier in order to convert float values into integer.

Selection list referenced by the following parameters:

- ⮡ DNP3 . Scale Factor 0

Scale Factor	Description
0.001	*0.001*
0.01	*0.01*
0.1	*0.1*

Scale Factor	Description
1	*1*
10	*10*
100	*100*
1000	*1000*
10000	*10000*
100000	*100000*
1000000	*1000000*

Optical rest position

Selection list referenced by the following parameters:

- ⮡ Modbus . Optical rest position

Optical rest position	Description
Light off	*Light off*
Light on	*Light on*

Port selection

Selection list referenced by the following parameters:

- ⮡ Modbus . TCP Port Config

Port selection	Description
Default	*Default Port*
Private	*Private Port*

Baud rate

Selection list referenced by the following parameters:

- ⮡ Modbus . Baud rate

Baud rate	Description
1200	*1200*
2400	*2400*
4800	*4800*
9600	*9600*
19200	*19200*
38400	*38400*

Byte Frame

Selection list referenced by the following parameters:

- ⮡ Modbus . Physical Settings

Byte Frame	Description
8E1	*8 data bits, even parity, 1 stopbit.*
8O1	*8 data bits, odd, 1 stopbit.*
8N1	*8 data bits, no parity, 1 stopbit.*
8N2	*8 data bits, no parity, 2 stopbits.*

Type of SCADA mapping

This setting decides whether the communication protocol shall use the default mapping of data objects, or some user-defined mapping that has been loaded from a *.HptSMap file.

Selection list referenced by the following parameters:

- ⮡ Modbus . Type of SCADA mapping

Type of SCADA mapping	Description
Standard	*Default mapping of data objects*
User-defined	*User-defined mapping of data objects*

Config status

Status of the user-defined SCADA configuration.\nPossible values:

Selection list referenced by the following parameters:

- ⮡ Modbus . Config status

Config status	Description
Changing	*New SCADA configuration is being loaded, but not active yet.*
OK	*The SCADA configuration is active.*
Config. not avail.	*The user-defined SCADA configuration is not available (e.g. has not been loaded into the device).*
Error	*Unexpected error. Please contact our service-team.*

Baud rate

Selection list referenced by the following parameters:

- ⮡ IEC103 . Baud rate

Baud rate	Description
1200	*1200*
2400	*2400*
4800	*4800*
9600	*9600*
19200	*19200*
38400	*38400*
57600	*57600*

Byte Frame

Selection list referenced by the following parameters:

- ⮡ IEC103 . Physical Settings

Byte Frame	Description
8E1	*8 data bits, even parity, 1 stopbit.*
8O1	*8 data bits, odd, 1 stopbit.*

Byte Frame	Description
8N1	*8 data bits, no parity, 1 stopbit.*
8N2	*8 data bits, no parity, 2 stopbits.*

Timezone

Selection whether the timestamps in IEC103 messages shall be given as UTC or local time. (“Local time” always includes the actual daylight saving settings.)

Selection list referenced by the following parameters:

- ⮡ IEC103 . Timezone

Timezone	Description
UTC	*UTC*
Local Time	*Local time according to the »Time Zones« setting (in Device Parameters) (incl. daylight saving settings).*

Optical rest position

Selection list referenced by the following parameters:

- ⮡ IEC103 . Optical rest position

Optical rest position	Description
Light off	*Light off*
Light on	*Light on*

Port selection

Selection list referenced by the following parameters:

- ⮡ IEC104 . TCP Port Config

Port selection	Description
Default	*Default Port*
Private	*Private Port*

Timezone

Selection whether the timestamps in the transmitted communication telegrams shall be given as UTC or local time. (“Local time” always includes the actual daylight saving settings.)

Selection list referenced by the following parameters:

- ⮡ IEC104 . Timezone

Timezone	Description
UTC	*UTC*
Local Time	*Local time according to the »Time Zones« setting (in Device Parameters) (incl. daylight saving settings).*

Type of SCADA mapping

This setting decides whether the communication protocol shall use the default mapping of data objects, or some user-defined mapping that has been loaded from a *.HptSMap file.

Selection list referenced by the following parameters:

- ⮡ IEC104 . Type of SCADA mapping

Type of SCADA mapping	Description
Standard	*Default mapping of data objects*
User-defined	*User-defined mapping of data objects*

Config status

Status of the user-defined SCADA configuration.\nPossible values:

Selection list referenced by the following parameters:

- ⮡ IEC104 . Config status

Config status	Description
Changing	*New SCADA configuration is being loaded, but not active yet.*
OK	*The SCADA configuration is active.*

Config status	Description
Config. not avail.	*The user-defined SCADA configuration is not available (e.g. has not been loaded into the device).*
Error	*Unexpected error. Please contact our service-team.*

Type of SCADA mapping

This setting decides whether the communication protocol shall use the default mapping of data objects, or some user-defined mapping that has been loaded from a *.HptSMap file.

Selection list referenced by the following parameters:

- ⮡ Profibus . Type of SCADA mapping

Type of SCADA mapping	Description
Standard	*Default mapping of data objects*
User-defined	*User-defined mapping of data objects*

Time Zones

Selection list referenced by the following parameters:

- ⮡ TimeSync . Time Zones

Time Zones	Description
UTC+14 Kiritimati	*UTC+14 Kiritimati*
UTC+13 Rawaki	*UTC+13 Rawaki*
UTC+12.75 Chatham Island	*UTC+12.75 Chatham Island*
UTC+12 Wellington	*UTC+12 Wellington*
UTC+11.5 Kingston	*UTC+11.5 Kingston*
UTC+11 Port Vila	*UTC+11 Port Vila*
UTC+10.5 Lord Howe Island	*UTC+10.5 Lord Howe Island*
UTC+10 Sydney	*UTC+10 Sydney*
UTC+9.5 Adelaide	*UTC+9.5 Adelaide*

Time Zones	Description
UTC+9 Tokyo	*UTC+9 Tokyo*
UTC+8 Hong Kong	*UTC+8 Hong Kong*
UTC+7 Bangkok	*UTC+7 Bangkok*
UTC+6.5 Rangoon	*UTC+6.5 Rangoon*
UTC+6 Colombo	*UTC+6 Colombo*
UTC+5.75 Kathmandu	*UTC+5.75 Kathmandu*
UTC+5.5 New Delhi	*UTC+5.5 New Delhi*
UTC+5 Islamabad	*UTC+5 Islamabad*
UTC+4.5 Kabul	*UTC+4.5 Kabul*
UTC+4 Abu Dhabi	*UTC+4 Abu Dhabi*
UTC+3.5 Tehran	*UTC+3.5 Tehran*
UTC+3 Moscow	*UTC+3 Moscow*
UTC+2 Athens	*UTC+2 Athens*
UTC+1 Berlin	*UTC+1 Berlin*
UTC+0 London	*UTC+0 London*
UTC-1 Azores	*UTC-1 Azores*
UTC-2 Fern. d. Noronha	*UTC-2 Fern. d. Noronha*
UTC-3 Buenos Aires	*UTC-3 Buenos Aires*
UTC-3.5 St. John’s	*UTC-3.5 St. John’s*
UTC-4 Santiago	*UTC-4 Santiago*
UTC-5 New York	*UTC-5 New York*
UTC-6 Chicago	*UTC-6 Chicago*
UTC-7 Salt Lake City	*UTC-7 Salt Lake City*
UTC-8 Los Angeles	*UTC-8 Los Angeles*
UTC-9 Anchorage	*UTC-9 Anchorage*
UTC-9.5 Taiohae	*UTC-9.5 Taiohae*
UTC-10 Honolulu	*UTC-10 Honolulu*
UTC-11 Midway Islands	*UTC-11 Midway Islands*

Month of clock change

Selection list referenced by the following parameters:

- ⮡ TimeSync . Summertime m
- ⮡ TimeSync . Wintertime m

Month of clock change	Description
January	*January*
February	*February*
March	*March*
April	*April*
May	*May*
June	*June*
July	*July*
August	*August*
September	*September*
October	*October*
November	*November*
December	*December*

Date

Selection list referenced by the following parameters:

- ⮡ TimeSync . Summertime d
- ⮡ TimeSync . Wintertime d

Date	Description
Sunday	*Sunday*
Monday	*Monday*
Tuesday	*Tuesday*
Wednesday	*Wednesday*
Thursday	*Thursday*
Friday	*Friday*
Saturday	*Saturday*

Date	Description
General day	*General day: Examples: first day of month, last day of month*

Day of clock change

Day of Time Saving change

Selection list referenced by the following parameters:

- ⮡ TimeSync . Summertime w
- ⮡ TimeSync . Wintertime w

Day of clock change	Description
First	*First week of the month*
Second	*Second week of the month*
Third	*Third week of the month*
Fourth	*Fourth week of the month*
Last	*Last week of the month*

Used Protocol

Selection list referenced by the following parameters:

- ⮡ TimeSync . TimeSync

Used Protocol	Description
“-”	**-**
IRIG-B . **IRIG-B**	*IRIG-B-Module*
SNTP . **SNTP**	*SNTP-Module*
Modbus . **Modbus**	*Modbus Protocol*
IEC103 . **IEC 60870-5-103**	*IEC 60870-5-103 Protocol*
IEC104 . **IEC104**	*IEC 60870-5-104 communication*
DNP3 . **DNP3**	*Distributed Network Protocol*

IRIG-B00X

Determination of the Type: IRIG-B00X. IRIG-B types differ in types of included “Coded Expressions” (year, control-functions, straight-binary-seconds).

Selection list referenced by the following parameters:

- ⮡ IRIG-B . IRIG-B00X

IRIG-B00X	Description
IRIGB-000	*Please refer to: IRIG STANDARD 200-04*
IRIGB-001	*Please refer to: IRIG STANDARD 200-04*
IRIGB-002	*Please refer to: IRIG STANDARD 200-04*
IRIGB-003	*Please refer to: IRIG STANDARD 200-04*
IRIGB-004	*Please refer to: IRIG STANDARD 200-04*
IRIGB-005	*Please refer to: IRIG STANDARD 200-04*
IRIGB-006	*Please refer to: IRIG STANDARD 200-04*
IRIGB-007	*Please refer to: IRIG STANDARD 200-04*

Selection list referenced by the following parameters:

- ⮡ Sys . DM version

	Description
3.6.b	*Version*

Phase Sequence

Phase Sequence direction

Selection list referenced by the following parameters:

- ⮡ Field Para . Phase Sequence

Phase Sequence	Description
ABC	*rotating clockwise*
ACB	*Counter-clockwise phase sequence. Positive and negative phase sequence are exchanged and MTA is turned for 180°.*

fN

Selection list referenced by the following parameters:

- ⮡ Field Para . f

fN	Description
50	*Rated frequency*
60	*Rated frequency*

VT con

This parameter has to be set in order to ensure the correct assignment of the voltage measurement channels in the device.

Selection list referenced by the following parameters:

- ⮡ VT . VT con

VT con	Description
Phase to Phase	*The phase voltage measuring inputs are feed with "Phase-to-Phase" voltages (Delta-Connection)*
Phase to Ground	*The phase voltage measuring inputs are feed with "Phase-to-Ground" voltages (Star-Connection)*

Voltages to be synchronized

Selection list referenced by the following parameters:

- ⮡ VT . V Sync

Voltages to be synchronized	Description
L1	*Phase L1*
L2	*Phase L2*
L3	*Phase L3*
L12	*L12*
L23	*L23*

Voltages to be synchronized	Description
L31	*L31*

delta phi - Mode

The delta phi element (vector surge) trips, if the permissable voltage angle shift (delta phi) of the three measured voltages (phase-ground or phase-phase) in: one phase, two phases or within all phases is exceeded.

Selection list referenced by the following parameters:

- ⮡ VT . delta phi - Mode

delta phi - Mode	Description
one phase	*one phase*
two phases	*two phases*
three phases	*three phases*

active/inactive

Selection list referenced by the following parameters:

- ⮡ BO Slot X2 . DISARMED Ctrl
- ⮡ Prot . ExBlo Fc
- ⮡ Prot . ExBlo TripCmd Fc
- ⮡ V[1] . ExBlo Fc
- ⮡ V[1] . ExBlo TripCmd Fc
- ⮡ df/dt . ExBlo Fc
- *[. . .]*

active/inactive	Description
inactive	*inactive*
active	*active*

1..n, Dig Inputs

List of Digital Inputs that are available for the detection of the Circuit Breaker Position.

Selection list referenced by the following parameters:

- ReCon[1] . PCC Fuse Fail VT
- TCS . Input 1
- TCS . Input 2

1..n, Dig Inputs	Description
“-”	*No assignment*
DI Slot X1 . **DI 1**	*Signal: Digital Input*
DI Slot X1 . **DI 2**	*Signal: Digital Input*
DI Slot X1 . **DI 3**	*Signal: Digital Input*
DI Slot X1 . **DI 4**	*Signal: Digital Input*
DI Slot X1 . **DI 5**	*Signal: Digital Input*
DI Slot X1 . **DI 6**	*Signal: Digital Input*
DI Slot X1 . **DI 7**	*Signal: Digital Input*
DI Slot X1 . **DI 8**	*Signal: Digital Input*

Decoupling Functions

Selection list referenced by the following parameters:

- ReCon[1] . Decoupling1

Decoupling Functions	Description
“-”	*No assignment*
V[1] . **TripCmd**	*Signal: Trip Command*
V[2] . **TripCmd**	*Signal: Trip Command*
V[3] . **TripCmd**	*Signal: Trip Command*
V[4] . **TripCmd**	*Signal: Trip Command*
V[5] . **TripCmd**	*Signal: Trip Command*
V[6] . **TripCmd**	*Signal: Trip Command*
df/dt . **TripCmd**	*Signal: Trip Command*
delta phi . **TripCmd**	*Signal: Trip Command*

Decoupling Functions	Description
Intertripping . **TripCmd**	*Signal: Trip Command*
LVRT[1] . **TripCmd**	*Signal: Trip Command*
LVRT[2] . **TripCmd**	*Signal: Trip Command*
VG[1] . **TripCmd**	*Signal: Trip Command*
VG[2] . **TripCmd**	*Signal: Trip Command*
V012[1] . **TripCmd**	*Signal: Trip Command*
V012[2] . **TripCmd**	*Signal: Trip Command*
V012[3] . **TripCmd**	*Signal: Trip Command*
V012[4] . **TripCmd**	*Signal: Trip Command*
V012[5] . **TripCmd**	*Signal: Trip Command*
V012[6] . **TripCmd**	*Signal: Trip Command*
f[1] . **TripCmd**	*Signal: Trip Command*
f[2] . **TripCmd**	*Signal: Trip Command*
f[3] . **TripCmd**	*Signal: Trip Command*
f[4] . **TripCmd**	*Signal: Trip Command*
f[5] . **TripCmd**	*Signal: Trip Command*
f[6] . **TripCmd**	*Signal: Trip Command*
ExP[1] . **TripCmd**	*Signal: Trip Command*
ExP[2] . **TripCmd**	*Signal: Trip Command*
ExP[3] . **TripCmd**	*Signal: Trip Command*
ExP[4] . **TripCmd**	*Signal: Trip Command*
DI Slot X1 . **DI 1**	*Signal: Digital Input*
DI Slot X1 . **DI 2**	*Signal: Digital Input*
DI Slot X1 . **DI 3**	*Signal: Digital Input*
DI Slot X1 . **DI 4**	*Signal: Digital Input*
DI Slot X1 . **DI 5**	*Signal: Digital Input*
DI Slot X1 . **DI 6**	*Signal: Digital Input*
DI Slot X1 . **DI 7**	*Signal: Digital Input*
DI Slot X1 . **DI 8**	*Signal: Digital Input*
DNP3 . **BinaryOutput0**	*Virtual Digital Output (DNP). This corresponds to a virtual binary input of the protective device.*
DNP3 . **BinaryOutput1**	*Virtual Digital Output (DNP). This corresponds to a virtual binary input of the protective device.*

Decoupling Functions	Description
DNP3 . **BinaryOutput2**	*Virtual Digital Output (DNP). This corresponds to a virtual binary input of the protective device.*
DNP3 . **BinaryOutput3**	*Virtual Digital Output (DNP). This corresponds to a virtual binary input of the protective device.*
DNP3 . **BinaryOutput4**	*Virtual Digital Output (DNP). This corresponds to a virtual binary input of the protective device.*
DNP3 . **BinaryOutput5**	*Virtual Digital Output (DNP). This corresponds to a virtual binary input of the protective device.*
DNP3 . **BinaryOutput6**	*Virtual Digital Output (DNP). This corresponds to a virtual binary input of the protective device.*
DNP3 . **BinaryOutput7**	*Virtual Digital Output (DNP). This corresponds to a virtual binary input of the protective device.*
DNP3 . **BinaryOutput8**	*Virtual Digital Output (DNP). This corresponds to a virtual binary input of the protective device.*
DNP3 . **BinaryOutput9**	*Virtual Digital Output (DNP). This corresponds to a virtual binary input of the protective device.*
DNP3 . **BinaryOutput10**	*Virtual Digital Output (DNP). This corresponds to a virtual binary input of the protective device.*
DNP3 . **BinaryOutput11**	*Virtual Digital Output (DNP). This corresponds to a virtual binary input of the protective device.*
DNP3 . **BinaryOutput12**	*Virtual Digital Output (DNP). This corresponds to a virtual binary input of the protective device.*
DNP3 . **BinaryOutput13**	*Virtual Digital Output (DNP). This corresponds to a virtual binary input of the protective device.*
DNP3 . **BinaryOutput14**	*Virtual Digital Output (DNP). This corresponds to a virtual binary input of the protective device.*
DNP3 . **BinaryOutput15**	*Virtual Digital Output (DNP). This corresponds to a virtual binary input of the protective device.*
DNP3 . **BinaryOutput16**	*Virtual Digital Output (DNP). This corresponds to a virtual binary input of the protective device.*
DNP3 . **BinaryOutput17**	*Virtual Digital Output (DNP). This corresponds to a virtual binary input of the protective device.*
DNP3 . **BinaryOutput18**	*Virtual Digital Output (DNP). This corresponds to a virtual binary input of the protective device.*
DNP3 . **BinaryOutput19**	*Virtual Digital Output (DNP). This corresponds to a virtual binary input of the protective device.*
DNP3 . **BinaryOutput20**	*Virtual Digital Output (DNP). This corresponds to a virtual binary input of the protective device.*
DNP3 . **BinaryOutput21**	*Virtual Digital Output (DNP). This corresponds to a virtual binary input of the protective device.*

Decoupling Functions	Description
DNP3 . **BinaryOutput22**	*Virtual Digital Output (DNP). This corresponds to a virtual binary input of the protective device.*
DNP3 . **BinaryOutput23**	*Virtual Digital Output (DNP). This corresponds to a virtual binary input of the protective device.*
DNP3 . **BinaryOutput24**	*Virtual Digital Output (DNP). This corresponds to a virtual binary input of the protective device.*
DNP3 . **BinaryOutput25**	*Virtual Digital Output (DNP). This corresponds to a virtual binary input of the protective device.*
DNP3 . **BinaryOutput26**	*Virtual Digital Output (DNP). This corresponds to a virtual binary input of the protective device.*
DNP3 . **BinaryOutput27**	*Virtual Digital Output (DNP). This corresponds to a virtual binary input of the protective device.*
DNP3 . **BinaryOutput28**	*Virtual Digital Output (DNP). This corresponds to a virtual binary input of the protective device.*
DNP3 . **BinaryOutput29**	*Virtual Digital Output (DNP). This corresponds to a virtual binary input of the protective device.*
DNP3 . **BinaryOutput30**	*Virtual Digital Output (DNP). This corresponds to a virtual binary input of the protective device.*
DNP3 . **BinaryOutput31**	*Virtual Digital Output (DNP). This corresponds to a virtual binary input of the protective device.*
Modbus . **Scada Cmd 1**	*Scada Command*
Modbus . **Scada Cmd 2**	*Scada Command*
Modbus . **Scada Cmd 3**	*Scada Command*
Modbus . **Scada Cmd 4**	*Scada Command*
Modbus . **Scada Cmd 5**	*Scada Command*
Modbus . **Scada Cmd 6**	*Scada Command*
Modbus . **Scada Cmd 7**	*Scada Command*
Modbus . **Scada Cmd 8**	*Scada Command*
Modbus . **Scada Cmd 9**	*Scada Command*
Modbus . **Scada Cmd 10**	*Scada Command*
Modbus . **Scada Cmd 11**	*Scada Command*
Modbus . **Scada Cmd 12**	*Scada Command*
Modbus . **Scada Cmd 13**	*Scada Command*
Modbus . **Scada Cmd 14**	*Scada Command*
Modbus . **Scada Cmd 15**	*Scada Command*
Modbus . **Scada Cmd 16**	*Scada Command*

Decoupling Functions	Description
IEC 61850 . **GOSINGGIO1.Ind1.stVal**	*Signal: Virtual Input (IEC61850 GGIO Ind): State*
IEC 61850 . **GOSINGGIO1.Ind2.stVal**	*Signal: Virtual Input (IEC61850 GGIO Ind): State*
IEC 61850 . **GOSINGGIO1.Ind3.stVal**	*Signal: Virtual Input (IEC61850 GGIO Ind): State*
IEC 61850 . **GOSINGGIO1.Ind4.stVal**	*Signal: Virtual Input (IEC61850 GGIO Ind): State*
IEC 61850 . **GOSINGGIO1.Ind5.stVal**	*Signal: Virtual Input (IEC61850 GGIO Ind): State*
IEC 61850 . **GOSINGGIO1.Ind6.stVal**	*Signal: Virtual Input (IEC61850 GGIO Ind): State*
IEC 61850 . **GOSINGGIO1.Ind7.stVal**	*Signal: Virtual Input (IEC61850 GGIO Ind): State*
IEC 61850 . **GOSINGGIO1.Ind8.stVal**	*Signal: Virtual Input (IEC61850 GGIO Ind): State*
IEC 61850 . **GOSINGGIO1.Ind9.stVal**	*Signal: Virtual Input (IEC61850 GGIO Ind): State*
IEC 61850 . **GOSINGGIO1.Ind10.stVal**	*Signal: Virtual Input (IEC61850 GGIO Ind): State*
IEC 61850 . **GOSINGGIO1.Ind11.stVal**	*Signal: Virtual Input (IEC61850 GGIO Ind): State*
IEC 61850 . **GOSINGGIO1.Ind12.stVal**	*Signal: Virtual Input (IEC61850 GGIO Ind): State*
IEC 61850 . **GOSINGGIO1.Ind13.stVal**	*Signal: Virtual Input (IEC61850 GGIO Ind): State*
IEC 61850 . **GOSINGGIO1.Ind14.stVal**	*Signal: Virtual Input (IEC61850 GGIO Ind): State*
IEC 61850 . **GOSINGGIO1.Ind15.stVal**	*Signal: Virtual Input (IEC61850 GGIO Ind): State*
IEC 61850 . **GOSINGGIO1.Ind16.stVal**	*Signal: Virtual Input (IEC61850 GGIO Ind): State*
IEC 61850 . **GOSINGGIO1.Ind17.stVal**	*Signal: Virtual Input (IEC61850 GGIO Ind): State*
IEC 61850 . **GOSINGGIO1.Ind18.stVal**	*Signal: Virtual Input (IEC61850 GGIO Ind): State*
IEC 61850 . **GOSINGGIO1.Ind19.stVal**	*Signal: Virtual Input (IEC61850 GGIO Ind): State*
IEC 61850 . **GOSINGGIO1.Ind20.stVal**	*Signal: Virtual Input (IEC61850 GGIO Ind): State*

Decoupling Functions	Description
IEC 61850 . **GOSINGGIO1.Ind21.stVal**	*Signal: Virtual Input (IEC61850 GGIO Ind): State*
IEC 61850 . **GOSINGGIO1.Ind22.stVal**	*Signal: Virtual Input (IEC61850 GGIO Ind): State*
IEC 61850 . **GOSINGGIO1.Ind23.stVal**	*Signal: Virtual Input (IEC61850 GGIO Ind): State*
IEC 61850 . **GOSINGGIO1.Ind24.stVal**	*Signal: Virtual Input (IEC61850 GGIO Ind): State*
IEC 61850 . **GOSINGGIO1.Ind25.stVal**	*Signal: Virtual Input (IEC61850 GGIO Ind): State*
IEC 61850 . **GOSINGGIO1.Ind26.stVal**	*Signal: Virtual Input (IEC61850 GGIO Ind): State*
IEC 61850 . **GOSINGGIO1.Ind27.stVal**	*Signal: Virtual Input (IEC61850 GGIO Ind): State*
IEC 61850 . **GOSINGGIO1.Ind28.stVal**	*Signal: Virtual Input (IEC61850 GGIO Ind): State*
IEC 61850 . **GOSINGGIO1.Ind29.stVal**	*Signal: Virtual Input (IEC61850 GGIO Ind): State*
IEC 61850 . **GOSINGGIO1.Ind30.stVal**	*Signal: Virtual Input (IEC61850 GGIO Ind): State*
IEC 61850 . **GOSINGGIO1.Ind31.stVal**	*Signal: Virtual Input (IEC61850 GGIO Ind): State*
IEC 61850 . **GOSINGGIO1.Ind32.stVal**	*Signal: Virtual Input (IEC61850 GGIO Ind): State*
IEC 61850 . **SPCSO1**	*Status bit that can be set by clients like e.g. SCADA (Single Point Controllable Status Output).*
IEC 61850 . **SPCSO2**	*Status bit that can be set by clients like e.g. SCADA (Single Point Controllable Status Output).*
IEC 61850 . **SPCSO3**	*Status bit that can be set by clients like e.g. SCADA (Single Point Controllable Status Output).*
IEC 61850 . **SPCSO4**	*Status bit that can be set by clients like e.g. SCADA (Single Point Controllable Status Output).*
IEC 61850 . **SPCSO5**	*Status bit that can be set by clients like e.g. SCADA (Single Point Controllable Status Output).*
IEC 61850 . **SPCSO6**	*Status bit that can be set by clients like e.g. SCADA (Single Point Controllable Status Output).*
IEC 61850 . **SPCSO7**	*Status bit that can be set by clients like e.g. SCADA (Single Point Controllable Status Output).*
IEC 61850 . **SPCSO8**	*Status bit that can be set by clients like e.g. SCADA (Single Point Controllable Status Output).*

Decoupling Functions	Description
IEC 61850 . **SPCSO9**	*Status bit that can be set by clients like e.g. SCADA (Single Point Controllable Status Output).*
IEC 61850 . **SPCSO10**	*Status bit that can be set by clients like e.g. SCADA (Single Point Controllable Status Output).*
IEC 61850 . **SPCSO11**	*Status bit that can be set by clients like e.g. SCADA (Single Point Controllable Status Output).*
IEC 61850 . **SPCSO12**	*Status bit that can be set by clients like e.g. SCADA (Single Point Controllable Status Output).*
IEC 61850 . **SPCSO13**	*Status bit that can be set by clients like e.g. SCADA (Single Point Controllable Status Output).*
IEC 61850 . **SPCSO14**	*Status bit that can be set by clients like e.g. SCADA (Single Point Controllable Status Output).*
IEC 61850 . **SPCSO15**	*Status bit that can be set by clients like e.g. SCADA (Single Point Controllable Status Output).*
IEC 61850 . **SPCSO16**	*Status bit that can be set by clients like e.g. SCADA (Single Point Controllable Status Output).*
IEC103 . **Scada Cmd 1**	*Scada Command*
IEC103 . **Scada Cmd 2**	*Scada Command*
IEC103 . **Scada Cmd 3**	*Scada Command*
IEC103 . **Scada Cmd 4**	*Scada Command*
IEC103 . **Scada Cmd 5**	*Scada Command*
IEC103 . **Scada Cmd 6**	*Scada Command*
IEC103 . **Scada Cmd 7**	*Scada Command*
IEC103 . **Scada Cmd 8**	*Scada Command*
IEC103 . **Scada Cmd 9**	*Scada Command*
IEC103 . **Scada Cmd 10**	*Scada Command*
IEC104 . **Scada Cmd 1**	*Scada Command*
IEC104 . **Scada Cmd 2**	*Scada Command*
IEC104 . **Scada Cmd 3**	*Scada Command*
IEC104 . **Scada Cmd 4**	*Scada Command*
IEC104 . **Scada Cmd 5**	*Scada Command*
IEC104 . **Scada Cmd 6**	*Scada Command*
IEC104 . **Scada Cmd 7**	*Scada Command*
IEC104 . **Scada Cmd 8**	*Scada Command*
IEC104 . **Scada Cmd 9**	*Scada Command*

Decoupling Functions	Description
IEC104 . **Scada Cmd 10**	*Scada Command*
IEC104 . **Scada Cmd 11**	*Scada Command*
IEC104 . **Scada Cmd 12**	*Scada Command*
IEC104 . **Scada Cmd 13**	*Scada Command*
IEC104 . **Scada Cmd 14**	*Scada Command*
IEC104 . **Scada Cmd 15**	*Scada Command*
IEC104 . **Scada Cmd 16**	*Scada Command*
Profibus . **Scada Cmd 1**	*Scada Command*
Profibus . **Scada Cmd 2**	*Scada Command*
Profibus . **Scada Cmd 3**	*Scada Command*
Profibus . **Scada Cmd 4**	*Scada Command*
Profibus . **Scada Cmd 5**	*Scada Command*
Profibus . **Scada Cmd 6**	*Scada Command*
Profibus . **Scada Cmd 7**	*Scada Command*
Profibus . **Scada Cmd 8**	*Scada Command*
Profibus . **Scada Cmd 9**	*Scada Command*
Profibus . **Scada Cmd 10**	*Scada Command*
Profibus . **Scada Cmd 11**	*Scada Command*
Profibus . **Scada Cmd 12**	*Scada Command*
Profibus . **Scada Cmd 13**	*Scada Command*
Profibus . **Scada Cmd 14**	*Scada Command*
Profibus . **Scada Cmd 15**	*Scada Command*
Profibus . **Scada Cmd 16**	*Scada Command*
Logics . **LE1.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE1.Timer Out**	*Signal: Timer Output*
Logics . **LE1.Out**	*Signal: Latched Output (Q)*
Logics . **LE1.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE2.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE2.Timer Out**	*Signal: Timer Output*
Logics . **LE2.Out**	*Signal: Latched Output (Q)*
Logics . **LE2.Out inverted**	*Signal: Negated Latched Output (Q NOT)*

Decoupling Functions	Description
Logics . **LE3.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE3.Timer Out**	*Signal: Timer Output*
Logics . **LE3.Out**	*Signal: Latched Output (Q)*
Logics . **LE3.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE4.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE4.Timer Out**	*Signal: Timer Output*
Logics . **LE4.Out**	*Signal: Latched Output (Q)*
Logics . **LE4.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE5.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE5.Timer Out**	*Signal: Timer Output*
Logics . **LE5.Out**	*Signal: Latched Output (Q)*
Logics . **LE5.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE6.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE6.Timer Out**	*Signal: Timer Output*
Logics . **LE6.Out**	*Signal: Latched Output (Q)*
Logics . **LE6.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE7.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE7.Timer Out**	*Signal: Timer Output*
Logics . **LE7.Out**	*Signal: Latched Output (Q)*
Logics . **LE7.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE8.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE8.Timer Out**	*Signal: Timer Output*
Logics . **LE8.Out**	*Signal: Latched Output (Q)*
Logics . **LE8.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE9.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE9.Timer Out**	*Signal: Timer Output*
Logics . **LE9.Out**	*Signal: Latched Output (Q)*
Logics . **LE9.Out inverted**	*Signal: Negated Latched Output (Q NOT)*

Decoupling Functions	Description
Logics . **LE10.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE10.Timer Out**	*Signal: Timer Output*
Logics . **LE10.Out**	*Signal: Latched Output (Q)*
Logics . **LE10.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE11.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE11.Timer Out**	*Signal: Timer Output*
Logics . **LE11.Out**	*Signal: Latched Output (Q)*
Logics . **LE11.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE12.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE12.Timer Out**	*Signal: Timer Output*
Logics . **LE12.Out**	*Signal: Latched Output (Q)*
Logics . **LE12.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE13.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE13.Timer Out**	*Signal: Timer Output*
Logics . **LE13.Out**	*Signal: Latched Output (Q)*
Logics . **LE13.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE14.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE14.Timer Out**	*Signal: Timer Output*
Logics . **LE14.Out**	*Signal: Latched Output (Q)*
Logics . **LE14.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE15.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE15.Timer Out**	*Signal: Timer Output*
Logics . **LE15.Out**	*Signal: Latched Output (Q)*
Logics . **LE15.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE16.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE16.Timer Out**	*Signal: Timer Output*
Logics . **LE16.Out**	*Signal: Latched Output (Q)*
Logics . **LE16.Out inverted**	*Signal: Negated Latched Output (Q NOT)*

Decoupling Functions	Description
Logics . **LE17.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE17.Timer Out**	*Signal: Timer Output*
Logics . **LE17.Out**	*Signal: Latched Output (Q)*
Logics . **LE17.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE18.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE18.Timer Out**	*Signal: Timer Output*
Logics . **LE18.Out**	*Signal: Latched Output (Q)*
Logics . **LE18.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE19.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE19.Timer Out**	*Signal: Timer Output*
Logics . **LE19.Out**	*Signal: Latched Output (Q)*
Logics . **LE19.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE20.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE20.Timer Out**	*Signal: Timer Output*
Logics . **LE20.Out**	*Signal: Latched Output (Q)*
Logics . **LE20.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE21.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE21.Timer Out**	*Signal: Timer Output*
Logics . **LE21.Out**	*Signal: Latched Output (Q)*
Logics . **LE21.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE22.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE22.Timer Out**	*Signal: Timer Output*
Logics . **LE22.Out**	*Signal: Latched Output (Q)*
Logics . **LE22.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE23.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE23.Timer Out**	*Signal: Timer Output*
Logics . **LE23.Out**	*Signal: Latched Output (Q)*
Logics . **LE23.Out inverted**	*Signal: Negated Latched Output (Q NOT)*

Decoupling Functions	Description
Logics . **LE24.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE24.Timer Out**	*Signal: Timer Output*
Logics . **LE24.Out**	*Signal: Latched Output (Q)*
Logics . **LE24.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE25.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE25.Timer Out**	*Signal: Timer Output*
Logics . **LE25.Out**	*Signal: Latched Output (Q)*
Logics . **LE25.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE26.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE26.Timer Out**	*Signal: Timer Output*
Logics . **LE26.Out**	*Signal: Latched Output (Q)*
Logics . **LE26.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE27.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE27.Timer Out**	*Signal: Timer Output*
Logics . **LE27.Out**	*Signal: Latched Output (Q)*
Logics . **LE27.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE28.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE28.Timer Out**	*Signal: Timer Output*
Logics . **LE28.Out**	*Signal: Latched Output (Q)*
Logics . **LE28.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE29.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE29.Timer Out**	*Signal: Timer Output*
Logics . **LE29.Out**	*Signal: Latched Output (Q)*
Logics . **LE29.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE30.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE30.Timer Out**	*Signal: Timer Output*
Logics . **LE30.Out**	*Signal: Latched Output (Q)*
Logics . **LE30.Out inverted**	*Signal: Negated Latched Output (Q NOT)*

Decoupling Functions	Description
Logics . **LE31.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE31.Timer Out**	*Signal: Timer Output*
Logics . **LE31.Out**	*Signal: Latched Output (Q)*
Logics . **LE31.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE32.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE32.Timer Out**	*Signal: Timer Output*
Logics . **LE32.Out**	*Signal: Latched Output (Q)*
Logics . **LE32.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE33.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE33.Timer Out**	*Signal: Timer Output*
Logics . **LE33.Out**	*Signal: Latched Output (Q)*
Logics . **LE33.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE34.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE34.Timer Out**	*Signal: Timer Output*
Logics . **LE34.Out**	*Signal: Latched Output (Q)*
Logics . **LE34.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE35.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE35.Timer Out**	*Signal: Timer Output*
Logics . **LE35.Out**	*Signal: Latched Output (Q)*
Logics . **LE35.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE36.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE36.Timer Out**	*Signal: Timer Output*
Logics . **LE36.Out**	*Signal: Latched Output (Q)*
Logics . **LE36.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE37.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE37.Timer Out**	*Signal: Timer Output*
Logics . **LE37.Out**	*Signal: Latched Output (Q)*
Logics . **LE37.Out inverted**	*Signal: Negated Latched Output (Q NOT)*

Decoupling Functions	Description
Logics . **LE38.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE38.Timer Out**	*Signal: Timer Output*
Logics . **LE38.Out**	*Signal: Latched Output (Q)*
Logics . **LE38.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE39.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE39.Timer Out**	*Signal: Timer Output*
Logics . **LE39.Out**	*Signal: Latched Output (Q)*
Logics . **LE39.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE40.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE40.Timer Out**	*Signal: Timer Output*
Logics . **LE40.Out**	*Signal: Latched Output (Q)*
Logics . **LE40.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE41.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE41.Timer Out**	*Signal: Timer Output*
Logics . **LE41.Out**	*Signal: Latched Output (Q)*
Logics . **LE41.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE42.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE42.Timer Out**	*Signal: Timer Output*
Logics . **LE42.Out**	*Signal: Latched Output (Q)*
Logics . **LE42.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE43.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE43.Timer Out**	*Signal: Timer Output*
Logics . **LE43.Out**	*Signal: Latched Output (Q)*
Logics . **LE43.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE44.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE44.Timer Out**	*Signal: Timer Output*
Logics . **LE44.Out**	*Signal: Latched Output (Q)*
Logics . **LE44.Out inverted**	*Signal: Negated Latched Output (Q NOT)*

Decoupling Functions	Description
Logics . **LE45.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE45.Timer Out**	*Signal: Timer Output*
Logics . **LE45.Out**	*Signal: Latched Output (Q)*
Logics . **LE45.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE46.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE46.Timer Out**	*Signal: Timer Output*
Logics . **LE46.Out**	*Signal: Latched Output (Q)*
Logics . **LE46.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE47.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE47.Timer Out**	*Signal: Timer Output*
Logics . **LE47.Out**	*Signal: Latched Output (Q)*
Logics . **LE47.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE48.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE48.Timer Out**	*Signal: Timer Output*
Logics . **LE48.Out**	*Signal: Latched Output (Q)*
Logics . **LE48.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE49.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE49.Timer Out**	*Signal: Timer Output*
Logics . **LE49.Out**	*Signal: Latched Output (Q)*
Logics . **LE49.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE50.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE50.Timer Out**	*Signal: Timer Output*
Logics . **LE50.Out**	*Signal: Latched Output (Q)*
Logics . **LE50.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE51.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE51.Timer Out**	*Signal: Timer Output*
Logics . **LE51.Out**	*Signal: Latched Output (Q)*
Logics . **LE51.Out inverted**	*Signal: Negated Latched Output (Q NOT)*

Decoupling Functions	Description
Logics . **LE52.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE52.Timer Out**	*Signal: Timer Output*
Logics . **LE52.Out**	*Signal: Latched Output (Q)*
Logics . **LE52.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE53.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE53.Timer Out**	*Signal: Timer Output*
Logics . **LE53.Out**	*Signal: Latched Output (Q)*
Logics . **LE53.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE54.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE54.Timer Out**	*Signal: Timer Output*
Logics . **LE54.Out**	*Signal: Latched Output (Q)*
Logics . **LE54.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE55.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE55.Timer Out**	*Signal: Timer Output*
Logics . **LE55.Out**	*Signal: Latched Output (Q)*
Logics . **LE55.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE56.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE56.Timer Out**	*Signal: Timer Output*
Logics . **LE56.Out**	*Signal: Latched Output (Q)*
Logics . **LE56.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE57.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE57.Timer Out**	*Signal: Timer Output*
Logics . **LE57.Out**	*Signal: Latched Output (Q)*
Logics . **LE57.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE58.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE58.Timer Out**	*Signal: Timer Output*
Logics . **LE58.Out**	*Signal: Latched Output (Q)*
Logics . **LE58.Out inverted**	*Signal: Negated Latched Output (Q NOT)*

Decoupling Functions	Description
Logics . **LE59.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE59.Timer Out**	*Signal: Timer Output*
Logics . **LE59.Out**	*Signal: Latched Output (Q)*
Logics . **LE59.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE60.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE60.Timer Out**	*Signal: Timer Output*
Logics . **LE60.Out**	*Signal: Latched Output (Q)*
Logics . **LE60.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE61.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE61.Timer Out**	*Signal: Timer Output*
Logics . **LE61.Out**	*Signal: Latched Output (Q)*
Logics . **LE61.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE62.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE62.Timer Out**	*Signal: Timer Output*
Logics . **LE62.Out**	*Signal: Latched Output (Q)*
Logics . **LE62.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE63.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE63.Timer Out**	*Signal: Timer Output*
Logics . **LE63.Out**	*Signal: Latched Output (Q)*
Logics . **LE63.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE64.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE64.Timer Out**	*Signal: Timer Output*
Logics . **LE64.Out**	*Signal: Latched Output (Q)*
Logics . **LE64.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE65.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE65.Timer Out**	*Signal: Timer Output*
Logics . **LE65.Out**	*Signal: Latched Output (Q)*
Logics . **LE65.Out inverted**	*Signal: Negated Latched Output (Q NOT)*

Decoupling Functions	Description
Logics . **LE66.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE66.Timer Out**	*Signal: Timer Output*
Logics . **LE66.Out**	*Signal: Latched Output (Q)*
Logics . **LE66.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE67.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE67.Timer Out**	*Signal: Timer Output*
Logics . **LE67.Out**	*Signal: Latched Output (Q)*
Logics . **LE67.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE68.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE68.Timer Out**	*Signal: Timer Output*
Logics . **LE68.Out**	*Signal: Latched Output (Q)*
Logics . **LE68.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE69.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE69.Timer Out**	*Signal: Timer Output*
Logics . **LE69.Out**	*Signal: Latched Output (Q)*
Logics . **LE69.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE70.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE70.Timer Out**	*Signal: Timer Output*
Logics . **LE70.Out**	*Signal: Latched Output (Q)*
Logics . **LE70.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE71.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE71.Timer Out**	*Signal: Timer Output*
Logics . **LE71.Out**	*Signal: Latched Output (Q)*
Logics . **LE71.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE72.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE72.Timer Out**	*Signal: Timer Output*
Logics . **LE72.Out**	*Signal: Latched Output (Q)*
Logics . **LE72.Out inverted**	*Signal: Negated Latched Output (Q NOT)*

Decoupling Functions	Description
Logics . **LE73.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE73.Timer Out**	*Signal: Timer Output*
Logics . **LE73.Out**	*Signal: Latched Output (Q)*
Logics . **LE73.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE74.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE74.Timer Out**	*Signal: Timer Output*
Logics . **LE74.Out**	*Signal: Latched Output (Q)*
Logics . **LE74.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE75.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE75.Timer Out**	*Signal: Timer Output*
Logics . **LE75.Out**	*Signal: Latched Output (Q)*
Logics . **LE75.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE76.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE76.Timer Out**	*Signal: Timer Output*
Logics . **LE76.Out**	*Signal: Latched Output (Q)*
Logics . **LE76.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE77.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE77.Timer Out**	*Signal: Timer Output*
Logics . **LE77.Out**	*Signal: Latched Output (Q)*
Logics . **LE77.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE78.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE78.Timer Out**	*Signal: Timer Output*
Logics . **LE78.Out**	*Signal: Latched Output (Q)*
Logics . **LE78.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE79.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE79.Timer Out**	*Signal: Timer Output*
Logics . **LE79.Out**	*Signal: Latched Output (Q)*
Logics . **LE79.Out inverted**	*Signal: Negated Latched Output (Q NOT)*

Decoupling Functions	Description
Logics . **LE80.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE80.Timer Out**	*Signal: Timer Output*
Logics . **LE80.Out**	*Signal: Latched Output (Q)*
Logics . **LE80.Out inverted**	*Signal: Negated Latched Output (Q NOT)*

1..n, DI-LogicList

Selection list referenced by the following parameters:

- ⮡ Sync . Bypass
- ⮡ SG[1] . Aux ON
- ⮡ SG[1] . Aux OFF
- ⮡ SG[1] . Ready
- ⮡ SG[1] . Removed
- ⮡ SG[1] . SCmd ON
- *[. . .]*

1..n, DI-LogicList	Description
“-”	*No assignment*
DI Slot X1 . **DI 1**	*Signal: Digital Input*
DI Slot X1 . **DI 2**	*Signal: Digital Input*
DI Slot X1 . **DI 3**	*Signal: Digital Input*
DI Slot X1 . **DI 4**	*Signal: Digital Input*
DI Slot X1 . **DI 5**	*Signal: Digital Input*
DI Slot X1 . **DI 6**	*Signal: Digital Input*
DI Slot X1 . **DI 7**	*Signal: Digital Input*
DI Slot X1 . **DI 8**	*Signal: Digital Input*
DNP3 . **BinaryOutput0**	*Virtual Digital Output (DNP). This corresponds to a virtual binary input of the protective device.*
DNP3 . **BinaryOutput1**	*Virtual Digital Output (DNP). This corresponds to a virtual binary input of the protective device.*
DNP3 . **BinaryOutput2**	*Virtual Digital Output (DNP). This corresponds to a virtual binary input of the protective device.*

1..n, DI-LogicList	Description
DNP3 . **BinaryOutput3**	*Virtual Digital Output (DNP). This corresponds to a virtual binary input of the protective device.*
DNP3 . **BinaryOutput4**	*Virtual Digital Output (DNP). This corresponds to a virtual binary input of the protective device.*
DNP3 . **BinaryOutput5**	*Virtual Digital Output (DNP). This corresponds to a virtual binary input of the protective device.*
DNP3 . **BinaryOutput6**	*Virtual Digital Output (DNP). This corresponds to a virtual binary input of the protective device.*
DNP3 . **BinaryOutput7**	*Virtual Digital Output (DNP). This corresponds to a virtual binary input of the protective device.*
DNP3 . **BinaryOutput8**	*Virtual Digital Output (DNP). This corresponds to a virtual binary input of the protective device.*
DNP3 . **BinaryOutput9**	*Virtual Digital Output (DNP). This corresponds to a virtual binary input of the protective device.*
DNP3 . **BinaryOutput10**	*Virtual Digital Output (DNP). This corresponds to a virtual binary input of the protective device.*
DNP3 . **BinaryOutput11**	*Virtual Digital Output (DNP). This corresponds to a virtual binary input of the protective device.*
DNP3 . **BinaryOutput12**	*Virtual Digital Output (DNP). This corresponds to a virtual binary input of the protective device.*
DNP3 . **BinaryOutput13**	*Virtual Digital Output (DNP). This corresponds to a virtual binary input of the protective device.*
DNP3 . **BinaryOutput14**	*Virtual Digital Output (DNP). This corresponds to a virtual binary input of the protective device.*
DNP3 . **BinaryOutput15**	*Virtual Digital Output (DNP). This corresponds to a virtual binary input of the protective device.*
DNP3 . **BinaryOutput16**	*Virtual Digital Output (DNP). This corresponds to a virtual binary input of the protective device.*
DNP3 . **BinaryOutput17**	*Virtual Digital Output (DNP). This corresponds to a virtual binary input of the protective device.*
DNP3 . **BinaryOutput18**	*Virtual Digital Output (DNP). This corresponds to a virtual binary input of the protective device.*
DNP3 . **BinaryOutput19**	*Virtual Digital Output (DNP). This corresponds to a virtual binary input of the protective device.*
DNP3 . **BinaryOutput20**	*Virtual Digital Output (DNP). This corresponds to a virtual binary input of the protective device.*
DNP3 . **BinaryOutput21**	*Virtual Digital Output (DNP). This corresponds to a virtual binary input of the protective device.*
DNP3 . **BinaryOutput22**	*Virtual Digital Output (DNP). This corresponds to a virtual binary input of the protective device.*

1..n, DI-LogicList	Description
DNP3 . **BinaryOutput23**	*Virtual Digital Output (DNP). This corresponds to a virtual binary input of the protective device.*
DNP3 . **BinaryOutput24**	*Virtual Digital Output (DNP). This corresponds to a virtual binary input of the protective device.*
DNP3 . **BinaryOutput25**	*Virtual Digital Output (DNP). This corresponds to a virtual binary input of the protective device.*
DNP3 . **BinaryOutput26**	*Virtual Digital Output (DNP). This corresponds to a virtual binary input of the protective device.*
DNP3 . **BinaryOutput27**	*Virtual Digital Output (DNP). This corresponds to a virtual binary input of the protective device.*
DNP3 . **BinaryOutput28**	*Virtual Digital Output (DNP). This corresponds to a virtual binary input of the protective device.*
DNP3 . **BinaryOutput29**	*Virtual Digital Output (DNP). This corresponds to a virtual binary input of the protective device.*
DNP3 . **BinaryOutput30**	*Virtual Digital Output (DNP). This corresponds to a virtual binary input of the protective device.*
DNP3 . **BinaryOutput31**	*Virtual Digital Output (DNP). This corresponds to a virtual binary input of the protective device.*
IEC104 . **Scada Cmd 1**	*Scada Command*
IEC104 . **Scada Cmd 2**	*Scada Command*
IEC104 . **Scada Cmd 3**	*Scada Command*
IEC104 . **Scada Cmd 4**	*Scada Command*
IEC104 . **Scada Cmd 5**	*Scada Command*
IEC104 . **Scada Cmd 6**	*Scada Command*
IEC104 . **Scada Cmd 7**	*Scada Command*
IEC104 . **Scada Cmd 8**	*Scada Command*
IEC104 . **Scada Cmd 9**	*Scada Command*
IEC104 . **Scada Cmd 10**	*Scada Command*
IEC104 . **Scada Cmd 11**	*Scada Command*
IEC104 . **Scada Cmd 12**	*Scada Command*
IEC104 . **Scada Cmd 13**	*Scada Command*
IEC104 . **Scada Cmd 14**	*Scada Command*
IEC104 . **Scada Cmd 15**	*Scada Command*
IEC104 . **Scada Cmd 16**	*Scada Command*
Logics . **LE1.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE1.Timer Out**	*Signal: Timer Output*

1..n, DI-LogicList	Description
Logics . **LE1.Out**	*Signal: Latched Output (Q)*
Logics . **LE1.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE2.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE2.Timer Out**	*Signal: Timer Output*
Logics . **LE2.Out**	*Signal: Latched Output (Q)*
Logics . **LE2.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE3.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE3.Timer Out**	*Signal: Timer Output*
Logics . **LE3.Out**	*Signal: Latched Output (Q)*
Logics . **LE3.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE4.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE4.Timer Out**	*Signal: Timer Output*
Logics . **LE4.Out**	*Signal: Latched Output (Q)*
Logics . **LE4.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE5.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE5.Timer Out**	*Signal: Timer Output*
Logics . **LE5.Out**	*Signal: Latched Output (Q)*
Logics . **LE5.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE6.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE6.Timer Out**	*Signal: Timer Output*
Logics . **LE6.Out**	*Signal: Latched Output (Q)*
Logics . **LE6.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE7.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE7.Timer Out**	*Signal: Timer Output*
Logics . **LE7.Out**	*Signal: Latched Output (Q)*
Logics . **LE7.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE8.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE8.Timer Out**	*Signal: Timer Output*

1..n, DI-LogicList	Description
Logics . **LE8.Out**	*Signal: Latched Output (Q)*
Logics . **LE8.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE9.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE9.Timer Out**	*Signal: Timer Output*
Logics . **LE9.Out**	*Signal: Latched Output (Q)*
Logics . **LE9.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE10.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE10.Timer Out**	*Signal: Timer Output*
Logics . **LE10.Out**	*Signal: Latched Output (Q)*
Logics . **LE10.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE11.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE11.Timer Out**	*Signal: Timer Output*
Logics . **LE11.Out**	*Signal: Latched Output (Q)*
Logics . **LE11.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE12.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE12.Timer Out**	*Signal: Timer Output*
Logics . **LE12.Out**	*Signal: Latched Output (Q)*
Logics . **LE12.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE13.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE13.Timer Out**	*Signal: Timer Output*
Logics . **LE13.Out**	*Signal: Latched Output (Q)*
Logics . **LE13.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE14.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE14.Timer Out**	*Signal: Timer Output*
Logics . **LE14.Out**	*Signal: Latched Output (Q)*
Logics . **LE14.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE15.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE15.Timer Out**	*Signal: Timer Output*

1..n, DI-LogicList	Description
Logics . **LE15.Out**	*Signal: Latched Output (Q)*
Logics . **LE15.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE16.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE16.Timer Out**	*Signal: Timer Output*
Logics . **LE16.Out**	*Signal: Latched Output (Q)*
Logics . **LE16.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE17.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE17.Timer Out**	*Signal: Timer Output*
Logics . **LE17.Out**	*Signal: Latched Output (Q)*
Logics . **LE17.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE18.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE18.Timer Out**	*Signal: Timer Output*
Logics . **LE18.Out**	*Signal: Latched Output (Q)*
Logics . **LE18.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE19.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE19.Timer Out**	*Signal: Timer Output*
Logics . **LE19.Out**	*Signal: Latched Output (Q)*
Logics . **LE19.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE20.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE20.Timer Out**	*Signal: Timer Output*
Logics . **LE20.Out**	*Signal: Latched Output (Q)*
Logics . **LE20.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE21.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE21.Timer Out**	*Signal: Timer Output*
Logics . **LE21.Out**	*Signal: Latched Output (Q)*
Logics . **LE21.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE22.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE22.Timer Out**	*Signal: Timer Output*

1..n, DI-LogicList	Description
Logics . **LE22.Out**	*Signal: Latched Output (Q)*
Logics . **LE22.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE23.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE23.Timer Out**	*Signal: Timer Output*
Logics . **LE23.Out**	*Signal: Latched Output (Q)*
Logics . **LE23.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE24.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE24.Timer Out**	*Signal: Timer Output*
Logics . **LE24.Out**	*Signal: Latched Output (Q)*
Logics . **LE24.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE25.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE25.Timer Out**	*Signal: Timer Output*
Logics . **LE25.Out**	*Signal: Latched Output (Q)*
Logics . **LE25.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE26.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE26.Timer Out**	*Signal: Timer Output*
Logics . **LE26.Out**	*Signal: Latched Output (Q)*
Logics . **LE26.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE27.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE27.Timer Out**	*Signal: Timer Output*
Logics . **LE27.Out**	*Signal: Latched Output (Q)*
Logics . **LE27.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE28.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE28.Timer Out**	*Signal: Timer Output*
Logics . **LE28.Out**	*Signal: Latched Output (Q)*
Logics . **LE28.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE29.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE29.Timer Out**	*Signal: Timer Output*

1..n, DI-LogicList	Description
Logics . **LE29.Out**	*Signal: Latched Output (Q)*
Logics . **LE29.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE30.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE30.Timer Out**	*Signal: Timer Output*
Logics . **LE30.Out**	*Signal: Latched Output (Q)*
Logics . **LE30.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE31.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE31.Timer Out**	*Signal: Timer Output*
Logics . **LE31.Out**	*Signal: Latched Output (Q)*
Logics . **LE31.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE32.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE32.Timer Out**	*Signal: Timer Output*
Logics . **LE32.Out**	*Signal: Latched Output (Q)*
Logics . **LE32.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE33.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE33.Timer Out**	*Signal: Timer Output*
Logics . **LE33.Out**	*Signal: Latched Output (Q)*
Logics . **LE33.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE34.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE34.Timer Out**	*Signal: Timer Output*
Logics . **LE34.Out**	*Signal: Latched Output (Q)*
Logics . **LE34.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE35.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE35.Timer Out**	*Signal: Timer Output*
Logics . **LE35.Out**	*Signal: Latched Output (Q)*
Logics . **LE35.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE36.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE36.Timer Out**	*Signal: Timer Output*

1..n, DI-LogicList	Description
Logics . **LE36.Out**	*Signal: Latched Output (Q)*
Logics . **LE36.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE37.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE37.Timer Out**	*Signal: Timer Output*
Logics . **LE37.Out**	*Signal: Latched Output (Q)*
Logics . **LE37.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE38.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE38.Timer Out**	*Signal: Timer Output*
Logics . **LE38.Out**	*Signal: Latched Output (Q)*
Logics . **LE38.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE39.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE39.Timer Out**	*Signal: Timer Output*
Logics . **LE39.Out**	*Signal: Latched Output (Q)*
Logics . **LE39.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE40.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE40.Timer Out**	*Signal: Timer Output*
Logics . **LE40.Out**	*Signal: Latched Output (Q)*
Logics . **LE40.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE41.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE41.Timer Out**	*Signal: Timer Output*
Logics . **LE41.Out**	*Signal: Latched Output (Q)*
Logics . **LE41.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE42.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE42.Timer Out**	*Signal: Timer Output*
Logics . **LE42.Out**	*Signal: Latched Output (Q)*
Logics . **LE42.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE43.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE43.Timer Out**	*Signal: Timer Output*

1..n, DI-LogicList	Description
Logics . **LE43.Out**	*Signal: Latched Output (Q)*
Logics . **LE43.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE44.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE44.Timer Out**	*Signal: Timer Output*
Logics . **LE44.Out**	*Signal: Latched Output (Q)*
Logics . **LE44.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE45.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE45.Timer Out**	*Signal: Timer Output*
Logics . **LE45.Out**	*Signal: Latched Output (Q)*
Logics . **LE45.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE46.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE46.Timer Out**	*Signal: Timer Output*
Logics . **LE46.Out**	*Signal: Latched Output (Q)*
Logics . **LE46.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE47.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE47.Timer Out**	*Signal: Timer Output*
Logics . **LE47.Out**	*Signal: Latched Output (Q)*
Logics . **LE47.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE48.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE48.Timer Out**	*Signal: Timer Output*
Logics . **LE48.Out**	*Signal: Latched Output (Q)*
Logics . **LE48.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE49.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE49.Timer Out**	*Signal: Timer Output*
Logics . **LE49.Out**	*Signal: Latched Output (Q)*
Logics . **LE49.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE50.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE50.Timer Out**	*Signal: Timer Output*

1..n, DI-LogicList	Description
Logics . **LE50.Out**	*Signal: Latched Output (Q)*
Logics . **LE50.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE51.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE51.Timer Out**	*Signal: Timer Output*
Logics . **LE51.Out**	*Signal: Latched Output (Q)*
Logics . **LE51.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE52.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE52.Timer Out**	*Signal: Timer Output*
Logics . **LE52.Out**	*Signal: Latched Output (Q)*
Logics . **LE52.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE53.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE53.Timer Out**	*Signal: Timer Output*
Logics . **LE53.Out**	*Signal: Latched Output (Q)*
Logics . **LE53.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE54.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE54.Timer Out**	*Signal: Timer Output*
Logics . **LE54.Out**	*Signal: Latched Output (Q)*
Logics . **LE54.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE55.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE55.Timer Out**	*Signal: Timer Output*
Logics . **LE55.Out**	*Signal: Latched Output (Q)*
Logics . **LE55.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE56.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE56.Timer Out**	*Signal: Timer Output*
Logics . **LE56.Out**	*Signal: Latched Output (Q)*
Logics . **LE56.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE57.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE57.Timer Out**	*Signal: Timer Output*

1..n, DI-LogicList	Description
Logics . **LE57.Out**	*Signal: Latched Output (Q)*
Logics . **LE57.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE58.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE58.Timer Out**	*Signal: Timer Output*
Logics . **LE58.Out**	*Signal: Latched Output (Q)*
Logics . **LE58.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE59.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE59.Timer Out**	*Signal: Timer Output*
Logics . **LE59.Out**	*Signal: Latched Output (Q)*
Logics . **LE59.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE60.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE60.Timer Out**	*Signal: Timer Output*
Logics . **LE60.Out**	*Signal: Latched Output (Q)*
Logics . **LE60.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE61.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE61.Timer Out**	*Signal: Timer Output*
Logics . **LE61.Out**	*Signal: Latched Output (Q)*
Logics . **LE61.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE62.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE62.Timer Out**	*Signal: Timer Output*
Logics . **LE62.Out**	*Signal: Latched Output (Q)*
Logics . **LE62.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE63.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE63.Timer Out**	*Signal: Timer Output*
Logics . **LE63.Out**	*Signal: Latched Output (Q)*
Logics . **LE63.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE64.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE64.Timer Out**	*Signal: Timer Output*

1..n, DI-LogicList	Description
Logics . **LE64.Out**	*Signal: Latched Output (Q)*
Logics . **LE64.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE65.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE65.Timer Out**	*Signal: Timer Output*
Logics . **LE65.Out**	*Signal: Latched Output (Q)*
Logics . **LE65.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE66.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE66.Timer Out**	*Signal: Timer Output*
Logics . **LE66.Out**	*Signal: Latched Output (Q)*
Logics . **LE66.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE67.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE67.Timer Out**	*Signal: Timer Output*
Logics . **LE67.Out**	*Signal: Latched Output (Q)*
Logics . **LE67.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE68.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE68.Timer Out**	*Signal: Timer Output*
Logics . **LE68.Out**	*Signal: Latched Output (Q)*
Logics . **LE68.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE69.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE69.Timer Out**	*Signal: Timer Output*
Logics . **LE69.Out**	*Signal: Latched Output (Q)*
Logics . **LE69.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE70.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE70.Timer Out**	*Signal: Timer Output*
Logics . **LE70.Out**	*Signal: Latched Output (Q)*
Logics . **LE70.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE71.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE71.Timer Out**	*Signal: Timer Output*

1..n, DI-LogicList	Description
Logics . **LE71.Out**	*Signal: Latched Output (Q)*
Logics . **LE71.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE72.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE72.Timer Out**	*Signal: Timer Output*
Logics . **LE72.Out**	*Signal: Latched Output (Q)*
Logics . **LE72.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE73.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE73.Timer Out**	*Signal: Timer Output*
Logics . **LE73.Out**	*Signal: Latched Output (Q)*
Logics . **LE73.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE74.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE74.Timer Out**	*Signal: Timer Output*
Logics . **LE74.Out**	*Signal: Latched Output (Q)*
Logics . **LE74.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE75.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE75.Timer Out**	*Signal: Timer Output*
Logics . **LE75.Out**	*Signal: Latched Output (Q)*
Logics . **LE75.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE76.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE76.Timer Out**	*Signal: Timer Output*
Logics . **LE76.Out**	*Signal: Latched Output (Q)*
Logics . **LE76.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE77.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE77.Timer Out**	*Signal: Timer Output*
Logics . **LE77.Out**	*Signal: Latched Output (Q)*
Logics . **LE77.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE78.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE78.Timer Out**	*Signal: Timer Output*

1..n, DI-LogicList	Description
Logics . **LE78.Out**	*Signal: Latched Output (Q)*
Logics . **LE78.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE79.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE79.Timer Out**	*Signal: Timer Output*
Logics . **LE79.Out**	*Signal: Latched Output (Q)*
Logics . **LE79.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE80.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE80.Timer Out**	*Signal: Timer Output*
Logics . **LE80.Out**	*Signal: Latched Output (Q)*
Logics . **LE80.Out inverted**	*Signal: Negated Latched Output (Q NOT)*

CB Manager

Circuit Breaker States

Selection list referenced by the following parameters:

- ⮡ Sync . CB Pos Detect

CB Manager	Description
“-”	*No assignment*
SG[1] . **Pos**	*Signal: Circuit Breaker Position (0 = Indeterminate, 1 = OFF, 2 = ON, 3 = Disturbed)*

1..n, SyncRequestList

Selection list referenced by the following parameters:

- ⮡ Sync . CBCloseInitiate

1..n, SyncRequestList	Description
“-”	*No assignment*
SG[1] . **Sync ON request**	*Signal: Synchronous ON request*

1..n, SyncRequestList	Description
DI Slot X1 . **DI 1**	*Signal: Digital Input*
DI Slot X1 . **DI 2**	*Signal: Digital Input*
DI Slot X1 . **DI 3**	*Signal: Digital Input*
DI Slot X1 . **DI 4**	*Signal: Digital Input*
DI Slot X1 . **DI 5**	*Signal: Digital Input*
DI Slot X1 . **DI 6**	*Signal: Digital Input*
DI Slot X1 . **DI 7**	*Signal: Digital Input*
DI Slot X1 . **DI 8**	*Signal: Digital Input*
Logics . **LE1.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE1.Timer Out**	*Signal: Timer Output*
Logics . **LE1.Out**	*Signal: Latched Output (Q)*
Logics . **LE1.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE2.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE2.Timer Out**	*Signal: Timer Output*
Logics . **LE2.Out**	*Signal: Latched Output (Q)*
Logics . **LE2.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE3.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE3.Timer Out**	*Signal: Timer Output*
Logics . **LE3.Out**	*Signal: Latched Output (Q)*
Logics . **LE3.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE4.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE4.Timer Out**	*Signal: Timer Output*
Logics . **LE4.Out**	*Signal: Latched Output (Q)*
Logics . **LE4.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE5.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE5.Timer Out**	*Signal: Timer Output*
Logics . **LE5.Out**	*Signal: Latched Output (Q)*
Logics . **LE5.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE6.Gate Out**	*Signal: Output of the logic gate*

1..n, SyncRequestList	Description
Logics . **LE6.Timer Out**	*Signal: Timer Output*
Logics . **LE6.Out**	*Signal: Latched Output (Q)*
Logics . **LE6.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE7.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE7.Timer Out**	*Signal: Timer Output*
Logics . **LE7.Out**	*Signal: Latched Output (Q)*
Logics . **LE7.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE8.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE8.Timer Out**	*Signal: Timer Output*
Logics . **LE8.Out**	*Signal: Latched Output (Q)*
Logics . **LE8.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE9.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE9.Timer Out**	*Signal: Timer Output*
Logics . **LE9.Out**	*Signal: Latched Output (Q)*
Logics . **LE9.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE10.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE10.Timer Out**	*Signal: Timer Output*
Logics . **LE10.Out**	*Signal: Latched Output (Q)*
Logics . **LE10.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE11.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE11.Timer Out**	*Signal: Timer Output*
Logics . **LE11.Out**	*Signal: Latched Output (Q)*
Logics . **LE11.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE12.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE12.Timer Out**	*Signal: Timer Output*
Logics . **LE12.Out**	*Signal: Latched Output (Q)*
Logics . **LE12.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE13.Gate Out**	*Signal: Output of the logic gate*

1..n, SyncRequestList	Description
Logics . **LE13.Timer Out**	*Signal: Timer Output*
Logics . **LE13.Out**	*Signal: Latched Output (Q)*
Logics . **LE13.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE14.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE14.Timer Out**	*Signal: Timer Output*
Logics . **LE14.Out**	*Signal: Latched Output (Q)*
Logics . **LE14.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE15.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE15.Timer Out**	*Signal: Timer Output*
Logics . **LE15.Out**	*Signal: Latched Output (Q)*
Logics . **LE15.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE16.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE16.Timer Out**	*Signal: Timer Output*
Logics . **LE16.Out**	*Signal: Latched Output (Q)*
Logics . **LE16.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE17.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE17.Timer Out**	*Signal: Timer Output*
Logics . **LE17.Out**	*Signal: Latched Output (Q)*
Logics . **LE17.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE18.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE18.Timer Out**	*Signal: Timer Output*
Logics . **LE18.Out**	*Signal: Latched Output (Q)*
Logics . **LE18.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE19.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE19.Timer Out**	*Signal: Timer Output*
Logics . **LE19.Out**	*Signal: Latched Output (Q)*
Logics . **LE19.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE20.Gate Out**	*Signal: Output of the logic gate*

1..n, SyncRequestList	Description
Logics . **LE20.Timer Out**	*Signal: Timer Output*
Logics . **LE20.Out**	*Signal: Latched Output (Q)*
Logics . **LE20.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE21.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE21.Timer Out**	*Signal: Timer Output*
Logics . **LE21.Out**	*Signal: Latched Output (Q)*
Logics . **LE21.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE22.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE22.Timer Out**	*Signal: Timer Output*
Logics . **LE22.Out**	*Signal: Latched Output (Q)*
Logics . **LE22.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE23.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE23.Timer Out**	*Signal: Timer Output*
Logics . **LE23.Out**	*Signal: Latched Output (Q)*
Logics . **LE23.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE24.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE24.Timer Out**	*Signal: Timer Output*
Logics . **LE24.Out**	*Signal: Latched Output (Q)*
Logics . **LE24.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE25.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE25.Timer Out**	*Signal: Timer Output*
Logics . **LE25.Out**	*Signal: Latched Output (Q)*
Logics . **LE25.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE26.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE26.Timer Out**	*Signal: Timer Output*
Logics . **LE26.Out**	*Signal: Latched Output (Q)*
Logics . **LE26.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE27.Gate Out**	*Signal: Output of the logic gate*

1..n, SyncRequestList	Description
Logics . **LE27.Timer Out**	*Signal: Timer Output*
Logics . **LE27.Out**	*Signal: Latched Output (Q)*
Logics . **LE27.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE28.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE28.Timer Out**	*Signal: Timer Output*
Logics . **LE28.Out**	*Signal: Latched Output (Q)*
Logics . **LE28.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE29.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE29.Timer Out**	*Signal: Timer Output*
Logics . **LE29.Out**	*Signal: Latched Output (Q)*
Logics . **LE29.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE30.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE30.Timer Out**	*Signal: Timer Output*
Logics . **LE30.Out**	*Signal: Latched Output (Q)*
Logics . **LE30.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE31.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE31.Timer Out**	*Signal: Timer Output*
Logics . **LE31.Out**	*Signal: Latched Output (Q)*
Logics . **LE31.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE32.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE32.Timer Out**	*Signal: Timer Output*
Logics . **LE32.Out**	*Signal: Latched Output (Q)*
Logics . **LE32.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE33.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE33.Timer Out**	*Signal: Timer Output*
Logics . **LE33.Out**	*Signal: Latched Output (Q)*
Logics . **LE33.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE34.Gate Out**	*Signal: Output of the logic gate*

1..n, SyncRequestList	Description
Logics . **LE34.Timer Out**	*Signal: Timer Output*
Logics . **LE34.Out**	*Signal: Latched Output (Q)*
Logics . **LE34.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE35.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE35.Timer Out**	*Signal: Timer Output*
Logics . **LE35.Out**	*Signal: Latched Output (Q)*
Logics . **LE35.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE36.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE36.Timer Out**	*Signal: Timer Output*
Logics . **LE36.Out**	*Signal: Latched Output (Q)*
Logics . **LE36.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE37.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE37.Timer Out**	*Signal: Timer Output*
Logics . **LE37.Out**	*Signal: Latched Output (Q)*
Logics . **LE37.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE38.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE38.Timer Out**	*Signal: Timer Output*
Logics . **LE38.Out**	*Signal: Latched Output (Q)*
Logics . **LE38.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE39.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE39.Timer Out**	*Signal: Timer Output*
Logics . **LE39.Out**	*Signal: Latched Output (Q)*
Logics . **LE39.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE40.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE40.Timer Out**	*Signal: Timer Output*
Logics . **LE40.Out**	*Signal: Latched Output (Q)*
Logics . **LE40.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE41.Gate Out**	*Signal: Output of the logic gate*

1..n, SyncRequestList	Description
Logics . **LE41.Timer Out**	*Signal: Timer Output*
Logics . **LE41.Out**	*Signal: Latched Output (Q)*
Logics . **LE41.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE42.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE42.Timer Out**	*Signal: Timer Output*
Logics . **LE42.Out**	*Signal: Latched Output (Q)*
Logics . **LE42.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE43.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE43.Timer Out**	*Signal: Timer Output*
Logics . **LE43.Out**	*Signal: Latched Output (Q)*
Logics . **LE43.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE44.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE44.Timer Out**	*Signal: Timer Output*
Logics . **LE44.Out**	*Signal: Latched Output (Q)*
Logics . **LE44.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE45.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE45.Timer Out**	*Signal: Timer Output*
Logics . **LE45.Out**	*Signal: Latched Output (Q)*
Logics . **LE45.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE46.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE46.Timer Out**	*Signal: Timer Output*
Logics . **LE46.Out**	*Signal: Latched Output (Q)*
Logics . **LE46.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE47.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE47.Timer Out**	*Signal: Timer Output*
Logics . **LE47.Out**	*Signal: Latched Output (Q)*
Logics . **LE47.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE48.Gate Out**	*Signal: Output of the logic gate*

1..n, SyncRequestList	Description
Logics . **LE48.Timer Out**	*Signal: Timer Output*
Logics . **LE48.Out**	*Signal: Latched Output (Q)*
Logics . **LE48.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE49.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE49.Timer Out**	*Signal: Timer Output*
Logics . **LE49.Out**	*Signal: Latched Output (Q)*
Logics . **LE49.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE50.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE50.Timer Out**	*Signal: Timer Output*
Logics . **LE50.Out**	*Signal: Latched Output (Q)*
Logics . **LE50.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE51.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE51.Timer Out**	*Signal: Timer Output*
Logics . **LE51.Out**	*Signal: Latched Output (Q)*
Logics . **LE51.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE52.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE52.Timer Out**	*Signal: Timer Output*
Logics . **LE52.Out**	*Signal: Latched Output (Q)*
Logics . **LE52.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE53.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE53.Timer Out**	*Signal: Timer Output*
Logics . **LE53.Out**	*Signal: Latched Output (Q)*
Logics . **LE53.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE54.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE54.Timer Out**	*Signal: Timer Output*
Logics . **LE54.Out**	*Signal: Latched Output (Q)*
Logics . **LE54.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE55.Gate Out**	*Signal: Output of the logic gate*

1..n, SyncRequestList	Description
Logics . **LE55.Timer Out**	*Signal: Timer Output*
Logics . **LE55.Out**	*Signal: Latched Output (Q)*
Logics . **LE55.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE56.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE56.Timer Out**	*Signal: Timer Output*
Logics . **LE56.Out**	*Signal: Latched Output (Q)*
Logics . **LE56.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE57.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE57.Timer Out**	*Signal: Timer Output*
Logics . **LE57.Out**	*Signal: Latched Output (Q)*
Logics . **LE57.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE58.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE58.Timer Out**	*Signal: Timer Output*
Logics . **LE58.Out**	*Signal: Latched Output (Q)*
Logics . **LE58.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE59.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE59.Timer Out**	*Signal: Timer Output*
Logics . **LE59.Out**	*Signal: Latched Output (Q)*
Logics . **LE59.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE60.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE60.Timer Out**	*Signal: Timer Output*
Logics . **LE60.Out**	*Signal: Latched Output (Q)*
Logics . **LE60.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE61.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE61.Timer Out**	*Signal: Timer Output*
Logics . **LE61.Out**	*Signal: Latched Output (Q)*
Logics . **LE61.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE62.Gate Out**	*Signal: Output of the logic gate*

1..n, SyncRequestList	Description
Logics . **LE62.Timer Out**	*Signal: Timer Output*
Logics . **LE62.Out**	*Signal: Latched Output (Q)*
Logics . **LE62.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE63.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE63.Timer Out**	*Signal: Timer Output*
Logics . **LE63.Out**	*Signal: Latched Output (Q)*
Logics . **LE63.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE64.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE64.Timer Out**	*Signal: Timer Output*
Logics . **LE64.Out**	*Signal: Latched Output (Q)*
Logics . **LE64.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE65.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE65.Timer Out**	*Signal: Timer Output*
Logics . **LE65.Out**	*Signal: Latched Output (Q)*
Logics . **LE65.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE66.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE66.Timer Out**	*Signal: Timer Output*
Logics . **LE66.Out**	*Signal: Latched Output (Q)*
Logics . **LE66.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE67.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE67.Timer Out**	*Signal: Timer Output*
Logics . **LE67.Out**	*Signal: Latched Output (Q)*
Logics . **LE67.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE68.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE68.Timer Out**	*Signal: Timer Output*
Logics . **LE68.Out**	*Signal: Latched Output (Q)*
Logics . **LE68.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE69.Gate Out**	*Signal: Output of the logic gate*

1..n, SyncRequestList	Description
Logics . **LE69.Timer Out**	*Signal: Timer Output*
Logics . **LE69.Out**	*Signal: Latched Output (Q)*
Logics . **LE69.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE70.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE70.Timer Out**	*Signal: Timer Output*
Logics . **LE70.Out**	*Signal: Latched Output (Q)*
Logics . **LE70.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE71.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE71.Timer Out**	*Signal: Timer Output*
Logics . **LE71.Out**	*Signal: Latched Output (Q)*
Logics . **LE71.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE72.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE72.Timer Out**	*Signal: Timer Output*
Logics . **LE72.Out**	*Signal: Latched Output (Q)*
Logics . **LE72.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE73.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE73.Timer Out**	*Signal: Timer Output*
Logics . **LE73.Out**	*Signal: Latched Output (Q)*
Logics . **LE73.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE74.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE74.Timer Out**	*Signal: Timer Output*
Logics . **LE74.Out**	*Signal: Latched Output (Q)*
Logics . **LE74.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE75.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE75.Timer Out**	*Signal: Timer Output*
Logics . **LE75.Out**	*Signal: Latched Output (Q)*
Logics . **LE75.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE76.Gate Out**	*Signal: Output of the logic gate*

1..n, SyncRequestList	Description
Logics . **LE76.Timer Out**	*Signal: Timer Output*
Logics . **LE76.Out**	*Signal: Latched Output (Q)*
Logics . **LE76.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE77.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE77.Timer Out**	*Signal: Timer Output*
Logics . **LE77.Out**	*Signal: Latched Output (Q)*
Logics . **LE77.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE78.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE78.Timer Out**	*Signal: Timer Output*
Logics . **LE78.Out**	*Signal: Latched Output (Q)*
Logics . **LE78.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE79.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE79.Timer Out**	*Signal: Timer Output*
Logics . **LE79.Out**	*Signal: Latched Output (Q)*
Logics . **LE79.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE80.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE80.Timer Out**	*Signal: Timer Output*
Logics . **LE80.Out**	*Signal: Latched Output (Q)*
Logics . **LE80.Out inverted**	*Signal: Negated Latched Output (Q NOT)*

Trigger

Determining the trigger mode for the Breaker Failure. The selection will pickup the Breaker Failure as well as the assignments (Trigger 1, Trigger 2, Trigger 3). They are OR connected.

Selection list referenced by the following parameters:

- ⮡ CBF . Trigger

Trigger	Description
- . -	*no assignment*

Trigger	Description
All Trips	*All trip signals that are assigned to this breaker (within the trip manager) will start the BF module.*
External Trips	*All external trips that are assigned to this breaker (within the trip manager) will start the BF module.*

External Trips

All external trips that are assigned to this breaker (within the trip manager) will start the BF module.

External Trips	Description
“-”	*No assignment*
Intertripping . **TripCmd**	*Signal: Trip Command*
ExP[1] . **TripCmd**	*Signal: Trip Command*
ExP[2] . **TripCmd**	*Signal: Trip Command*
ExP[3] . **TripCmd**	*Signal: Trip Command*
ExP[4] . **TripCmd**	*Signal: Trip Command*

Current Trips

All current trips that are assigned to this breaker (within the trip manager) will start the BF module.

Current Trips	Description
“-”	*No assignment*

Trigger

Determining the trigger mode for the Breaker Failure. The selection will pickup the Breaker Failure as well as the assignments (Trigger 1, Trigger 2, Trigger 3). They are OR connected.

Selection list referenced by the following parameters:

- ⮡ CBF . Trigger1

Trigger	Description
“-”	*No assignment*
V[1] . **TripCmd**	*Signal: Trip Command*
V[2] . **TripCmd**	*Signal: Trip Command*
V[3] . **TripCmd**	*Signal: Trip Command*
V[4] . **TripCmd**	*Signal: Trip Command*
V[5] . **TripCmd**	*Signal: Trip Command*
V[6] . **TripCmd**	*Signal: Trip Command*
df/dt . **TripCmd**	*Signal: Trip Command*
delta phi . **TripCmd**	*Signal: Trip Command*
Intertripping . **TripCmd**	*Signal: Trip Command*
LVRT[1] . **TripCmd**	*Signal: Trip Command*
LVRT[2] . **TripCmd**	*Signal: Trip Command*
VG[1] . **TripCmd**	*Signal: Trip Command*
VG[2] . **TripCmd**	*Signal: Trip Command*
V012[1] . **TripCmd**	*Signal: Trip Command*
V012[2] . **TripCmd**	*Signal: Trip Command*
V012[3] . **TripCmd**	*Signal: Trip Command*
V012[4] . **TripCmd**	*Signal: Trip Command*
V012[5] . **TripCmd**	*Signal: Trip Command*
V012[6] . **TripCmd**	*Signal: Trip Command*
f[1] . **TripCmd**	*Signal: Trip Command*
f[2] . **TripCmd**	*Signal: Trip Command*
f[3] . **TripCmd**	*Signal: Trip Command*
f[4] . **TripCmd**	*Signal: Trip Command*
f[5] . **TripCmd**	*Signal: Trip Command*
f[6] . **TripCmd**	*Signal: Trip Command*
ExP[1] . **TripCmd**	*Signal: Trip Command*
ExP[2] . **TripCmd**	*Signal: Trip Command*
ExP[3] . **TripCmd**	*Signal: Trip Command*
ExP[4] . **TripCmd**	*Signal: Trip Command*
DI Slot X1 . **DI 1**	*Signal: Digital Input*
DI Slot X1 . **DI 2**	*Signal: Digital Input*

Trigger	Description
DI Slot X1 . **DI 3**	*Signal: Digital Input*
DI Slot X1 . **DI 4**	*Signal: Digital Input*
DI Slot X1 . **DI 5**	*Signal: Digital Input*
DI Slot X1 . **DI 6**	*Signal: Digital Input*
DI Slot X1 . **DI 7**	*Signal: Digital Input*
DI Slot X1 . **DI 8**	*Signal: Digital Input*
Logics . **LE1.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE1.Timer Out**	*Signal: Timer Output*
Logics . **LE1.Out**	*Signal: Latched Output (Q)*
Logics . **LE1.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE2.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE2.Timer Out**	*Signal: Timer Output*
Logics . **LE2.Out**	*Signal: Latched Output (Q)*
Logics . **LE2.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE3.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE3.Timer Out**	*Signal: Timer Output*
Logics . **LE3.Out**	*Signal: Latched Output (Q)*
Logics . **LE3.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE4.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE4.Timer Out**	*Signal: Timer Output*
Logics . **LE4.Out**	*Signal: Latched Output (Q)*
Logics . **LE4.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE5.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE5.Timer Out**	*Signal: Timer Output*
Logics . **LE5.Out**	*Signal: Latched Output (Q)*
Logics . **LE5.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE6.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE6.Timer Out**	*Signal: Timer Output*
Logics . **LE6.Out**	*Signal: Latched Output (Q)*

Trigger	Description
Logics . **LE6.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE7.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE7.Timer Out**	*Signal: Timer Output*
Logics . **LE7.Out**	*Signal: Latched Output (Q)*
Logics . **LE7.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE8.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE8.Timer Out**	*Signal: Timer Output*
Logics . **LE8.Out**	*Signal: Latched Output (Q)*
Logics . **LE8.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE9.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE9.Timer Out**	*Signal: Timer Output*
Logics . **LE9.Out**	*Signal: Latched Output (Q)*
Logics . **LE9.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE10.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE10.Timer Out**	*Signal: Timer Output*
Logics . **LE10.Out**	*Signal: Latched Output (Q)*
Logics . **LE10.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE11.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE11.Timer Out**	*Signal: Timer Output*
Logics . **LE11.Out**	*Signal: Latched Output (Q)*
Logics . **LE11.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE12.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE12.Timer Out**	*Signal: Timer Output*
Logics . **LE12.Out**	*Signal: Latched Output (Q)*
Logics . **LE12.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE13.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE13.Timer Out**	*Signal: Timer Output*
Logics . **LE13.Out**	*Signal: Latched Output (Q)*

Trigger	Description
Logics . **LE13.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE14.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE14.Timer Out**	*Signal: Timer Output*
Logics . **LE14.Out**	*Signal: Latched Output (Q)*
Logics . **LE14.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE15.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE15.Timer Out**	*Signal: Timer Output*
Logics . **LE15.Out**	*Signal: Latched Output (Q)*
Logics . **LE15.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE16.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE16.Timer Out**	*Signal: Timer Output*
Logics . **LE16.Out**	*Signal: Latched Output (Q)*
Logics . **LE16.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE17.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE17.Timer Out**	*Signal: Timer Output*
Logics . **LE17.Out**	*Signal: Latched Output (Q)*
Logics . **LE17.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE18.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE18.Timer Out**	*Signal: Timer Output*
Logics . **LE18.Out**	*Signal: Latched Output (Q)*
Logics . **LE18.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE19.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE19.Timer Out**	*Signal: Timer Output*
Logics . **LE19.Out**	*Signal: Latched Output (Q)*
Logics . **LE19.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE20.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE20.Timer Out**	*Signal: Timer Output*
Logics . **LE20.Out**	*Signal: Latched Output (Q)*

Trigger	Description
Logics . **LE20.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE21.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE21.Timer Out**	*Signal: Timer Output*
Logics . **LE21.Out**	*Signal: Latched Output (Q)*
Logics . **LE21.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE22.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE22.Timer Out**	*Signal: Timer Output*
Logics . **LE22.Out**	*Signal: Latched Output (Q)*
Logics . **LE22.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE23.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE23.Timer Out**	*Signal: Timer Output*
Logics . **LE23.Out**	*Signal: Latched Output (Q)*
Logics . **LE23.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE24.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE24.Timer Out**	*Signal: Timer Output*
Logics . **LE24.Out**	*Signal: Latched Output (Q)*
Logics . **LE24.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE25.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE25.Timer Out**	*Signal: Timer Output*
Logics . **LE25.Out**	*Signal: Latched Output (Q)*
Logics . **LE25.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE26.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE26.Timer Out**	*Signal: Timer Output*
Logics . **LE26.Out**	*Signal: Latched Output (Q)*
Logics . **LE26.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE27.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE27.Timer Out**	*Signal: Timer Output*
Logics . **LE27.Out**	*Signal: Latched Output (Q)*

Trigger	Description
Logics . **LE27.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE28.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE28.Timer Out**	*Signal: Timer Output*
Logics . **LE28.Out**	*Signal: Latched Output (Q)*
Logics . **LE28.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE29.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE29.Timer Out**	*Signal: Timer Output*
Logics . **LE29.Out**	*Signal: Latched Output (Q)*
Logics . **LE29.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE30.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE30.Timer Out**	*Signal: Timer Output*
Logics . **LE30.Out**	*Signal: Latched Output (Q)*
Logics . **LE30.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE31.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE31.Timer Out**	*Signal: Timer Output*
Logics . **LE31.Out**	*Signal: Latched Output (Q)*
Logics . **LE31.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE32.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE32.Timer Out**	*Signal: Timer Output*
Logics . **LE32.Out**	*Signal: Latched Output (Q)*
Logics . **LE32.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE33.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE33.Timer Out**	*Signal: Timer Output*
Logics . **LE33.Out**	*Signal: Latched Output (Q)*
Logics . **LE33.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE34.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE34.Timer Out**	*Signal: Timer Output*
Logics . **LE34.Out**	*Signal: Latched Output (Q)*

Trigger	Description
Logics . **LE34.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE35.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE35.Timer Out**	*Signal: Timer Output*
Logics . **LE35.Out**	*Signal: Latched Output (Q)*
Logics . **LE35.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE36.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE36.Timer Out**	*Signal: Timer Output*
Logics . **LE36.Out**	*Signal: Latched Output (Q)*
Logics . **LE36.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE37.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE37.Timer Out**	*Signal: Timer Output*
Logics . **LE37.Out**	*Signal: Latched Output (Q)*
Logics . **LE37.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE38.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE38.Timer Out**	*Signal: Timer Output*
Logics . **LE38.Out**	*Signal: Latched Output (Q)*
Logics . **LE38.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE39.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE39.Timer Out**	*Signal: Timer Output*
Logics . **LE39.Out**	*Signal: Latched Output (Q)*
Logics . **LE39.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE40.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE40.Timer Out**	*Signal: Timer Output*
Logics . **LE40.Out**	*Signal: Latched Output (Q)*
Logics . **LE40.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE41.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE41.Timer Out**	*Signal: Timer Output*
Logics . **LE41.Out**	*Signal: Latched Output (Q)*

Trigger	Description
Logics . **LE41.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE42.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE42.Timer Out**	*Signal: Timer Output*
Logics . **LE42.Out**	*Signal: Latched Output (Q)*
Logics . **LE42.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE43.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE43.Timer Out**	*Signal: Timer Output*
Logics . **LE43.Out**	*Signal: Latched Output (Q)*
Logics . **LE43.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE44.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE44.Timer Out**	*Signal: Timer Output*
Logics . **LE44.Out**	*Signal: Latched Output (Q)*
Logics . **LE44.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE45.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE45.Timer Out**	*Signal: Timer Output*
Logics . **LE45.Out**	*Signal: Latched Output (Q)*
Logics . **LE45.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE46.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE46.Timer Out**	*Signal: Timer Output*
Logics . **LE46.Out**	*Signal: Latched Output (Q)*
Logics . **LE46.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE47.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE47.Timer Out**	*Signal: Timer Output*
Logics . **LE47.Out**	*Signal: Latched Output (Q)*
Logics . **LE47.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE48.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE48.Timer Out**	*Signal: Timer Output*
Logics . **LE48.Out**	*Signal: Latched Output (Q)*

Trigger	Description
Logics . **LE48.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE49.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE49.Timer Out**	*Signal: Timer Output*
Logics . **LE49.Out**	*Signal: Latched Output (Q)*
Logics . **LE49.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE50.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE50.Timer Out**	*Signal: Timer Output*
Logics . **LE50.Out**	*Signal: Latched Output (Q)*
Logics . **LE50.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE51.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE51.Timer Out**	*Signal: Timer Output*
Logics . **LE51.Out**	*Signal: Latched Output (Q)*
Logics . **LE51.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE52.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE52.Timer Out**	*Signal: Timer Output*
Logics . **LE52.Out**	*Signal: Latched Output (Q)*
Logics . **LE52.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE53.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE53.Timer Out**	*Signal: Timer Output*
Logics . **LE53.Out**	*Signal: Latched Output (Q)*
Logics . **LE53.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE54.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE54.Timer Out**	*Signal: Timer Output*
Logics . **LE54.Out**	*Signal: Latched Output (Q)*
Logics . **LE54.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE55.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE55.Timer Out**	*Signal: Timer Output*
Logics . **LE55.Out**	*Signal: Latched Output (Q)*

Trigger	Description
Logics . **LE55.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE56.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE56.Timer Out**	*Signal: Timer Output*
Logics . **LE56.Out**	*Signal: Latched Output (Q)*
Logics . **LE56.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE57.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE57.Timer Out**	*Signal: Timer Output*
Logics . **LE57.Out**	*Signal: Latched Output (Q)*
Logics . **LE57.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE58.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE58.Timer Out**	*Signal: Timer Output*
Logics . **LE58.Out**	*Signal: Latched Output (Q)*
Logics . **LE58.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE59.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE59.Timer Out**	*Signal: Timer Output*
Logics . **LE59.Out**	*Signal: Latched Output (Q)*
Logics . **LE59.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE60.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE60.Timer Out**	*Signal: Timer Output*
Logics . **LE60.Out**	*Signal: Latched Output (Q)*
Logics . **LE60.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE61.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE61.Timer Out**	*Signal: Timer Output*
Logics . **LE61.Out**	*Signal: Latched Output (Q)*
Logics . **LE61.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE62.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE62.Timer Out**	*Signal: Timer Output*
Logics . **LE62.Out**	*Signal: Latched Output (Q)*

Trigger	Description
Logics . **LE62.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE63.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE63.Timer Out**	*Signal: Timer Output*
Logics . **LE63.Out**	*Signal: Latched Output (Q)*
Logics . **LE63.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE64.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE64.Timer Out**	*Signal: Timer Output*
Logics . **LE64.Out**	*Signal: Latched Output (Q)*
Logics . **LE64.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE65.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE65.Timer Out**	*Signal: Timer Output*
Logics . **LE65.Out**	*Signal: Latched Output (Q)*
Logics . **LE65.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE66.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE66.Timer Out**	*Signal: Timer Output*
Logics . **LE66.Out**	*Signal: Latched Output (Q)*
Logics . **LE66.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE67.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE67.Timer Out**	*Signal: Timer Output*
Logics . **LE67.Out**	*Signal: Latched Output (Q)*
Logics . **LE67.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE68.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE68.Timer Out**	*Signal: Timer Output*
Logics . **LE68.Out**	*Signal: Latched Output (Q)*
Logics . **LE68.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE69.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE69.Timer Out**	*Signal: Timer Output*
Logics . **LE69.Out**	*Signal: Latched Output (Q)*

Trigger	Description
Logics . **LE69.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE70.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE70.Timer Out**	*Signal: Timer Output*
Logics . **LE70.Out**	*Signal: Latched Output (Q)*
Logics . **LE70.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE71.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE71.Timer Out**	*Signal: Timer Output*
Logics . **LE71.Out**	*Signal: Latched Output (Q)*
Logics . **LE71.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE72.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE72.Timer Out**	*Signal: Timer Output*
Logics . **LE72.Out**	*Signal: Latched Output (Q)*
Logics . **LE72.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE73.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE73.Timer Out**	*Signal: Timer Output*
Logics . **LE73.Out**	*Signal: Latched Output (Q)*
Logics . **LE73.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE74.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE74.Timer Out**	*Signal: Timer Output*
Logics . **LE74.Out**	*Signal: Latched Output (Q)*
Logics . **LE74.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE75.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE75.Timer Out**	*Signal: Timer Output*
Logics . **LE75.Out**	*Signal: Latched Output (Q)*
Logics . **LE75.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE76.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE76.Timer Out**	*Signal: Timer Output*
Logics . **LE76.Out**	*Signal: Latched Output (Q)*

Trigger	Description
Logics . **LE76.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE77.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE77.Timer Out**	*Signal: Timer Output*
Logics . **LE77.Out**	*Signal: Latched Output (Q)*
Logics . **LE77.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE78.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE78.Timer Out**	*Signal: Timer Output*
Logics . **LE78.Out**	*Signal: Latched Output (Q)*
Logics . **LE78.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE79.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE79.Timer Out**	*Signal: Timer Output*
Logics . **LE79.Out**	*Signal: Latched Output (Q)*
Logics . **LE79.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE80.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE80.Timer Out**	*Signal: Timer Output*
Logics . **LE80.Out**	*Signal: Latched Output (Q)*
Logics . **LE80.Out inverted**	*Signal: Negated Latched Output (Q NOT)*

Mode

general operation mode

Selection list referenced by the following parameters:

- ⮡ TCS . Mode

Mode	Description
Closed	*Selects that the breaker is going to be monitored when the breaker is closed.*
Either	*Selects that the breaker is going to be monitored when the breaker is either closed or open.*

PSet-Switch

Switching Parameter Set

Selection list referenced by the following parameters:

- ⮡ Sys . PSet-Switch

PSet-Switch	Description
PS1	*The currently active Parameter Set is PS1*
PS2	*The currently active Parameter Set is PS2*
PS3	*The currently active Parameter Set is PS3*
PS4	*The currently active Parameter Set is PS4*
PSS via Inp fct	*Parameter Set Switch via input function*
PSS via Scada	*Parameter Set Switch via Scada. Write into this output byte the integer of the parameter set that should become active (e.g. 4 => Switch onto parameter set 4).*

1..n, PSS

List of the available Parameter Setting Group Switching Signals

Selection list referenced by the following parameters:

- ⮡ Sys . PS1: activated by

1..n, PSS	Description
“-”	*No assignment*
VTS . **Alarm**	*Signal: Alarm Voltage Transformer Measuring Circuit Supervision*
DI Slot X1 . **DI 1**	*Signal: Digital Input*
DI Slot X1 . **DI 2**	*Signal: Digital Input*
DI Slot X1 . **DI 3**	*Signal: Digital Input*
DI Slot X1 . **DI 4**	*Signal: Digital Input*
DI Slot X1 . **DI 5**	*Signal: Digital Input*
DI Slot X1 . **DI 6**	*Signal: Digital Input*
DI Slot X1 . **DI 7**	*Signal: Digital Input*
DI Slot X1 . **DI 8**	*Signal: Digital Input*

1..n, PSS	Description
Logics . **LE1.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE1.Timer Out**	*Signal: Timer Output*
Logics . **LE1.Out**	*Signal: Latched Output (Q)*
Logics . **LE1.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE2.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE2.Timer Out**	*Signal: Timer Output*
Logics . **LE2.Out**	*Signal: Latched Output (Q)*
Logics . **LE2.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE3.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE3.Timer Out**	*Signal: Timer Output*
Logics . **LE3.Out**	*Signal: Latched Output (Q)*
Logics . **LE3.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE4.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE4.Timer Out**	*Signal: Timer Output*
Logics . **LE4.Out**	*Signal: Latched Output (Q)*
Logics . **LE4.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE5.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE5.Timer Out**	*Signal: Timer Output*
Logics . **LE5.Out**	*Signal: Latched Output (Q)*
Logics . **LE5.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE6.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE6.Timer Out**	*Signal: Timer Output*
Logics . **LE6.Out**	*Signal: Latched Output (Q)*
Logics . **LE6.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE7.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE7.Timer Out**	*Signal: Timer Output*
Logics . **LE7.Out**	*Signal: Latched Output (Q)*
Logics . **LE7.Out inverted**	*Signal: Negated Latched Output (Q NOT)*

1..n, PSS	Description
Logics . **LE8.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE8.Timer Out**	*Signal: Timer Output*
Logics . **LE8.Out**	*Signal: Latched Output (Q)*
Logics . **LE8.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE9.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE9.Timer Out**	*Signal: Timer Output*
Logics . **LE9.Out**	*Signal: Latched Output (Q)*
Logics . **LE9.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE10.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE10.Timer Out**	*Signal: Timer Output*
Logics . **LE10.Out**	*Signal: Latched Output (Q)*
Logics . **LE10.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE11.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE11.Timer Out**	*Signal: Timer Output*
Logics . **LE11.Out**	*Signal: Latched Output (Q)*
Logics . **LE11.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE12.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE12.Timer Out**	*Signal: Timer Output*
Logics . **LE12.Out**	*Signal: Latched Output (Q)*
Logics . **LE12.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE13.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE13.Timer Out**	*Signal: Timer Output*
Logics . **LE13.Out**	*Signal: Latched Output (Q)*
Logics . **LE13.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE14.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE14.Timer Out**	*Signal: Timer Output*
Logics . **LE14.Out**	*Signal: Latched Output (Q)*
Logics . **LE14.Out inverted**	*Signal: Negated Latched Output (Q NOT)*

1..n, PSS	Description
Logics . **LE15.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE15.Timer Out**	*Signal: Timer Output*
Logics . **LE15.Out**	*Signal: Latched Output (Q)*
Logics . **LE15.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE16.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE16.Timer Out**	*Signal: Timer Output*
Logics . **LE16.Out**	*Signal: Latched Output (Q)*
Logics . **LE16.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE17.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE17.Timer Out**	*Signal: Timer Output*
Logics . **LE17.Out**	*Signal: Latched Output (Q)*
Logics . **LE17.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE18.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE18.Timer Out**	*Signal: Timer Output*
Logics . **LE18.Out**	*Signal: Latched Output (Q)*
Logics . **LE18.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE19.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE19.Timer Out**	*Signal: Timer Output*
Logics . **LE19.Out**	*Signal: Latched Output (Q)*
Logics . **LE19.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE20.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE20.Timer Out**	*Signal: Timer Output*
Logics . **LE20.Out**	*Signal: Latched Output (Q)*
Logics . **LE20.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE21.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE21.Timer Out**	*Signal: Timer Output*
Logics . **LE21.Out**	*Signal: Latched Output (Q)*
Logics . **LE21.Out inverted**	*Signal: Negated Latched Output (Q NOT)*

1..n, PSS	Description
Logics . **LE22.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE22.Timer Out**	*Signal: Timer Output*
Logics . **LE22.Out**	*Signal: Latched Output (Q)*
Logics . **LE22.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE23.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE23.Timer Out**	*Signal: Timer Output*
Logics . **LE23.Out**	*Signal: Latched Output (Q)*
Logics . **LE23.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE24.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE24.Timer Out**	*Signal: Timer Output*
Logics . **LE24.Out**	*Signal: Latched Output (Q)*
Logics . **LE24.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE25.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE25.Timer Out**	*Signal: Timer Output*
Logics . **LE25.Out**	*Signal: Latched Output (Q)*
Logics . **LE25.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE26.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE26.Timer Out**	*Signal: Timer Output*
Logics . **LE26.Out**	*Signal: Latched Output (Q)*
Logics . **LE26.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE27.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE27.Timer Out**	*Signal: Timer Output*
Logics . **LE27.Out**	*Signal: Latched Output (Q)*
Logics . **LE27.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE28.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE28.Timer Out**	*Signal: Timer Output*
Logics . **LE28.Out**	*Signal: Latched Output (Q)*
Logics . **LE28.Out inverted**	*Signal: Negated Latched Output (Q NOT)*

1..n, PSS	Description
Logics . **LE29.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE29.Timer Out**	*Signal: Timer Output*
Logics . **LE29.Out**	*Signal: Latched Output (Q)*
Logics . **LE29.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE30.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE30.Timer Out**	*Signal: Timer Output*
Logics . **LE30.Out**	*Signal: Latched Output (Q)*
Logics . **LE30.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE31.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE31.Timer Out**	*Signal: Timer Output*
Logics . **LE31.Out**	*Signal: Latched Output (Q)*
Logics . **LE31.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE32.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE32.Timer Out**	*Signal: Timer Output*
Logics . **LE32.Out**	*Signal: Latched Output (Q)*
Logics . **LE32.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE33.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE33.Timer Out**	*Signal: Timer Output*
Logics . **LE33.Out**	*Signal: Latched Output (Q)*
Logics . **LE33.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE34.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE34.Timer Out**	*Signal: Timer Output*
Logics . **LE34.Out**	*Signal: Latched Output (Q)*
Logics . **LE34.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE35.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE35.Timer Out**	*Signal: Timer Output*
Logics . **LE35.Out**	*Signal: Latched Output (Q)*
Logics . **LE35.Out inverted**	*Signal: Negated Latched Output (Q NOT)*

1..n, PSS	Description
Logics . **LE36.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE36.Timer Out**	*Signal: Timer Output*
Logics . **LE36.Out**	*Signal: Latched Output (Q)*
Logics . **LE36.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE37.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE37.Timer Out**	*Signal: Timer Output*
Logics . **LE37.Out**	*Signal: Latched Output (Q)*
Logics . **LE37.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE38.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE38.Timer Out**	*Signal: Timer Output*
Logics . **LE38.Out**	*Signal: Latched Output (Q)*
Logics . **LE38.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE39.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE39.Timer Out**	*Signal: Timer Output*
Logics . **LE39.Out**	*Signal: Latched Output (Q)*
Logics . **LE39.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE40.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE40.Timer Out**	*Signal: Timer Output*
Logics . **LE40.Out**	*Signal: Latched Output (Q)*
Logics . **LE40.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE41.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE41.Timer Out**	*Signal: Timer Output*
Logics . **LE41.Out**	*Signal: Latched Output (Q)*
Logics . **LE41.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE42.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE42.Timer Out**	*Signal: Timer Output*
Logics . **LE42.Out**	*Signal: Latched Output (Q)*
Logics . **LE42.Out inverted**	*Signal: Negated Latched Output (Q NOT)*

1..n, PSS	Description
Logics . **LE43.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE43.Timer Out**	*Signal: Timer Output*
Logics . **LE43.Out**	*Signal: Latched Output (Q)*
Logics . **LE43.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE44.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE44.Timer Out**	*Signal: Timer Output*
Logics . **LE44.Out**	*Signal: Latched Output (Q)*
Logics . **LE44.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE45.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE45.Timer Out**	*Signal: Timer Output*
Logics . **LE45.Out**	*Signal: Latched Output (Q)*
Logics . **LE45.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE46.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE46.Timer Out**	*Signal: Timer Output*
Logics . **LE46.Out**	*Signal: Latched Output (Q)*
Logics . **LE46.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE47.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE47.Timer Out**	*Signal: Timer Output*
Logics . **LE47.Out**	*Signal: Latched Output (Q)*
Logics . **LE47.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE48.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE48.Timer Out**	*Signal: Timer Output*
Logics . **LE48.Out**	*Signal: Latched Output (Q)*
Logics . **LE48.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE49.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE49.Timer Out**	*Signal: Timer Output*
Logics . **LE49.Out**	*Signal: Latched Output (Q)*
Logics . **LE49.Out inverted**	*Signal: Negated Latched Output (Q NOT)*

1..n, PSS	Description
Logics . **LE50.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE50.Timer Out**	*Signal: Timer Output*
Logics . **LE50.Out**	*Signal: Latched Output (Q)*
Logics . **LE50.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE51.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE51.Timer Out**	*Signal: Timer Output*
Logics . **LE51.Out**	*Signal: Latched Output (Q)*
Logics . **LE51.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE52.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE52.Timer Out**	*Signal: Timer Output*
Logics . **LE52.Out**	*Signal: Latched Output (Q)*
Logics . **LE52.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE53.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE53.Timer Out**	*Signal: Timer Output*
Logics . **LE53.Out**	*Signal: Latched Output (Q)*
Logics . **LE53.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE54.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE54.Timer Out**	*Signal: Timer Output*
Logics . **LE54.Out**	*Signal: Latched Output (Q)*
Logics . **LE54.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE55.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE55.Timer Out**	*Signal: Timer Output*
Logics . **LE55.Out**	*Signal: Latched Output (Q)*
Logics . **LE55.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE56.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE56.Timer Out**	*Signal: Timer Output*
Logics . **LE56.Out**	*Signal: Latched Output (Q)*
Logics . **LE56.Out inverted**	*Signal: Negated Latched Output (Q NOT)*

1..n, PSS	Description
Logics . **LE57.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE57.Timer Out**	*Signal: Timer Output*
Logics . **LE57.Out**	*Signal: Latched Output (Q)*
Logics . **LE57.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE58.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE58.Timer Out**	*Signal: Timer Output*
Logics . **LE58.Out**	*Signal: Latched Output (Q)*
Logics . **LE58.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE59.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE59.Timer Out**	*Signal: Timer Output*
Logics . **LE59.Out**	*Signal: Latched Output (Q)*
Logics . **LE59.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE60.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE60.Timer Out**	*Signal: Timer Output*
Logics . **LE60.Out**	*Signal: Latched Output (Q)*
Logics . **LE60.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE61.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE61.Timer Out**	*Signal: Timer Output*
Logics . **LE61.Out**	*Signal: Latched Output (Q)*
Logics . **LE61.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE62.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE62.Timer Out**	*Signal: Timer Output*
Logics . **LE62.Out**	*Signal: Latched Output (Q)*
Logics . **LE62.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE63.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE63.Timer Out**	*Signal: Timer Output*
Logics . **LE63.Out**	*Signal: Latched Output (Q)*
Logics . **LE63.Out inverted**	*Signal: Negated Latched Output (Q NOT)*

1..n, PSS	Description
Logics . **LE64.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE64.Timer Out**	*Signal: Timer Output*
Logics . **LE64.Out**	*Signal: Latched Output (Q)*
Logics . **LE64.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE65.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE65.Timer Out**	*Signal: Timer Output*
Logics . **LE65.Out**	*Signal: Latched Output (Q)*
Logics . **LE65.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE66.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE66.Timer Out**	*Signal: Timer Output*
Logics . **LE66.Out**	*Signal: Latched Output (Q)*
Logics . **LE66.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE67.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE67.Timer Out**	*Signal: Timer Output*
Logics . **LE67.Out**	*Signal: Latched Output (Q)*
Logics . **LE67.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE68.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE68.Timer Out**	*Signal: Timer Output*
Logics . **LE68.Out**	*Signal: Latched Output (Q)*
Logics . **LE68.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE69.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE69.Timer Out**	*Signal: Timer Output*
Logics . **LE69.Out**	*Signal: Latched Output (Q)*
Logics . **LE69.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE70.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE70.Timer Out**	*Signal: Timer Output*
Logics . **LE70.Out**	*Signal: Latched Output (Q)*
Logics . **LE70.Out inverted**	*Signal: Negated Latched Output (Q NOT)*

1..n, PSS	Description
Logics . **LE71.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE71.Timer Out**	*Signal: Timer Output*
Logics . **LE71.Out**	*Signal: Latched Output (Q)*
Logics . **LE71.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE72.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE72.Timer Out**	*Signal: Timer Output*
Logics . **LE72.Out**	*Signal: Latched Output (Q)*
Logics . **LE72.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE73.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE73.Timer Out**	*Signal: Timer Output*
Logics . **LE73.Out**	*Signal: Latched Output (Q)*
Logics . **LE73.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE74.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE74.Timer Out**	*Signal: Timer Output*
Logics . **LE74.Out**	*Signal: Latched Output (Q)*
Logics . **LE74.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE75.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE75.Timer Out**	*Signal: Timer Output*
Logics . **LE75.Out**	*Signal: Latched Output (Q)*
Logics . **LE75.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE76.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE76.Timer Out**	*Signal: Timer Output*
Logics . **LE76.Out**	*Signal: Latched Output (Q)*
Logics . **LE76.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE77.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE77.Timer Out**	*Signal: Timer Output*
Logics . **LE77.Out**	*Signal: Latched Output (Q)*
Logics . **LE77.Out inverted**	*Signal: Negated Latched Output (Q NOT)*

1..n, PSS	Description
Logics . **LE78.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE78.Timer Out**	*Signal: Timer Output*
Logics . **LE78.Out**	*Signal: Latched Output (Q)*
Logics . **LE78.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE79.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE79.Timer Out**	*Signal: Timer Output*
Logics . **LE79.Out**	*Signal: Latched Output (Q)*
Logics . **LE79.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE80.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE80.Timer Out**	*Signal: Timer Output*
Logics . **LE80.Out**	*Signal: Latched Output (Q)*
Logics . **LE80.Out inverted**	*Signal: Negated Latched Output (Q NOT)*

Mode

general operation mode

Selection list referenced by the following parameters:

- ⮡ df/dt . df/dt mode

Mode	Description
absolute df/dt	*positive and negative rise of frequency frequency*
positive df/dt	*positive rise of frequency*
negative df/dt	*negative rise of frequency frequency*

Mode

general operation mode

Selection list referenced by the following parameters:

- ⮡ delta phi . df/dt mode

Mode	Description
absolute df/dt	*positive and negative rise of frequency frequency*
positive df/dt	*positive rise of frequency*
negative df/dt	*negative rise of frequency frequency*

Measuring Mode

Measuring/Supervision Mode: Determines if the phase-to-phase or phase-to-earth voltages are to be supervised

Selection list referenced by the following parameters:

- LVRT[1] . Measuring Mode

Measuring Mode	Description
Phase to Ground	*The voltage transformers are connected to phase-to-ground voltages*
Phase to Phase	*The voltage transformers are connected to phase-to-phase voltages*

Measuring method

Measuring method: fundamental or rms or 3rd harmonic (only generator protection relays)

Selection list referenced by the following parameters:

- LVRT[1] . Measuring method

Measuring method	Description
Fundamental	*Protection is based on Fundamental (1st. Harmonic)*
True RMS	*Protection is based on root-mean-square value (True RMS)*

Alarm Mode

Alarm criterion for the voltage protection stage.

Selection list referenced by the following parameters:

- LVRT[1] . Alarm Mode

Alarm Mode	Description
any one	*any one: Trip Command, if the tripping criterion is fulfilled within at least one phase.*
any two	*any two: Trip Command only if the tripping criterion is fulfilled in minimum two phases.*
all	*all: Trip Command for 3p-faults, i.e. if the tripping criterion is fulfilled in all three phases.*
only 2	*only 2: Trip Command for 2p-faults, i.e. if the tripping criterion is fulfilled in exactly two phases.*

VTS Block

Blocking of the module if the voltage transformer supervision detects a fault.

Selection list referenced by the following parameters:

- ⮡ V[1] . Meas Circuit Superv
- ⮡ LVRT[1] . Meas Circuit Superv
- ⮡ VG[1] . Meas Circuit Superv
- ⮡ V012[1] . Meas Circuit Superv
- ⮡ ReCon[1] . Meas Circuit Superv

VTS Block	Description
Sys . **inactive**	*inactive*
VTS . **active**	*active*

Reconnect. Release Cond

This parameter ensures that the mains voltage is recovered.

Selection list referenced by the following parameters:

- ⮡ ReCon[1] . Reconnect. Release Cond

Reconnect. Release Cond	Description
V Internal Release	*Release signal is being generated by internal voltage measuring values. The line-to-line voltage exceeds 95% Vn.*

Reconnect. Release Cond	Description
V Ext Release PCC	*Release signal is being generated by the PCC (External Release). The line-to-line voltage exceeds 95% Vn.*
Both	*Both: Release signal is being generated by the PCC (External Release) and by internal voltage measuring values.*

Measuring method

Measuring method: fundamental or rms or "sliding average supervision"

Selection list referenced by the following parameters:

- ReCon[1] . Measuring method

Measuring method	Description
Fundamental	*Protection is based on Fundamental (1st. Harmonic)*
True RMS	*Protection is based on root-mean-square value (True RMS)*
Vavg	*Sliding Voltage Average Supervision. Note: The settings for the average calculation have to be made within menu [Device Para/Statistics/Vavg].*

SyncMode

Synchrocheck mode: GENERATOR2SYSTEM = Synchronizing generator to system (breaker close initiate needed). SYSTEM2SYSTEM = SynchronCheck between two systems (Stand-Alone, no breaker info needed)

Selection list referenced by the following parameters:

- Sync . SyncMode

SyncMode	Description
System2System	*SYSTEM2SYSTEM = SynchronCheck between two systems (Stand-Alone, no breaker info needed)*
Generator2System	*GENERATOR2SYSTEM = Synchronizing generator to system (breaker close initiate needed).*

Measuring Mode

Measuring/Supervision Mode: Determines if the phase-to-phase or phase-to-earth voltages are to be supervised

Selection list referenced by the following parameters:

- ⮡ V[1] . Measuring Mode

Measuring Mode	Description
Phase to Ground	*The voltage transformers are connected to phase-to-ground voltages*
Phase to Phase	*The voltage transformers are connected to phase-to-phase voltages*

Measuring method

Measuring method: fundamental or rms or "sliding average supervision"

Selection list referenced by the following parameters:

- ⮡ V[1] . Measuring method

Measuring method	Description
Fundamental	*Protection is based on Fundamental (1st. Harmonic)*
True RMS	*Protection is based on root-mean-square value (True RMS)*
Vavg	*Sliding Voltage Average Supervision. Note: The settings for the average calculation have to be made within menu [Device Para/Statistics/Vavg].*

Alarm Mode

Alarm criterion for the voltage protection stage.

Selection list referenced by the following parameters:

- ⮡ V[1] . Alarm Mode

Alarm Mode	Description
any one	*any one: Trip Command, if the tripping criterion is fulfilled within at least one phase.*
any two	*any two*
all	*all: Trip Command for 3p-faults, i.e. if the tripping criterion is fulfilled in all three phases.*

VX Source

Selection if VG is measured or calculated (neutral voltage or residual voltage)

Selection list referenced by the following parameters:

- ⮡ VG[1] . VX Source

VX Source	Description
measured	*VX/VG is measured at the 4th measuring input*
calculated	*VX/VG is measured at the 4th measuring input*

Measuring method

Measuring method: fundamental or rms or 3rd harmonic (only generator protection relays)

Selection list referenced by the following parameters:

- ⮡ VG[1] . Measuring method

Measuring method	Description
Fundamental	*Protection is based on Fundamental (1st. Harmonic)*
True RMS	*Protection is based on root-mean-square value (True RMS)*

Mode

general operation mode

Selection list referenced by the following parameters:

- ⮡ f[1] . df/dt mode

Mode	Description
absolute df/dt	*positive and negative rise of frequency frequency*
positive df/dt	*positive rise of frequency*
negative df/dt	*negative rise of frequency frequency*

NonIL ResetMode

Non-Interlocking ResetMode

Selection list referenced by the following parameters:

- ⮡ Ctrl . Res NonIL

NonIL ResetMode	Description
single Operation	*single Operation*
timeout	*timeout*
permanent	*permanent*

Manipulate Position

WARNING! Fake Position - Manual Position Manipulation

Selection list referenced by the following parameters:

- ⮡ SG[1] . Manipulate Position

Manipulate Position	Description
inactive	*inactive*
Pos OFF	*Signal: Circuit Breaker is in OFF-Position*
Pos ON	*Signal: Circuit Breaker is in ON-Position*

1..n, Trip Cmds

List of available Trip Commands

Selection list referenced by the following parameters:

- ⮡ SG[1] . Off Cmd1
- ⮡ SG[1] . Off Cmd2
- ⮡ SG[1] . Off Cmd3
- ⮡ SG[1] . Off Cmd4
- ⮡ SG[1] . Off Cmd5

1..n, Trip Cmds	Description
“-”	*No assignment*

1..n, Trip Cmds	Description
V[1] . **TripCmd**	*Signal: Trip Command*
V[2] . **TripCmd**	*Signal: Trip Command*
V[3] . **TripCmd**	*Signal: Trip Command*
V[4] . **TripCmd**	*Signal: Trip Command*
V[5] . **TripCmd**	*Signal: Trip Command*
V[6] . **TripCmd**	*Signal: Trip Command*
df/dt . **TripCmd**	*Signal: Trip Command*
delta phi . **TripCmd**	*Signal: Trip Command*
Intertripping . **TripCmd**	*Signal: Trip Command*
LVRT[1] . **TripCmd**	*Signal: Trip Command*
LVRT[2] . **TripCmd**	*Signal: Trip Command*
VG[1] . **TripCmd**	*Signal: Trip Command*
VG[2] . **TripCmd**	*Signal: Trip Command*
V012[1] . **TripCmd**	*Signal: Trip Command*
V012[2] . **TripCmd**	*Signal: Trip Command*
V012[3] . **TripCmd**	*Signal: Trip Command*
V012[4] . **TripCmd**	*Signal: Trip Command*
V012[5] . **TripCmd**	*Signal: Trip Command*
V012[6] . **TripCmd**	*Signal: Trip Command*
f[1] . **TripCmd**	*Signal: Trip Command*
f[2] . **TripCmd**	*Signal: Trip Command*
f[3] . **TripCmd**	*Signal: Trip Command*
f[4] . **TripCmd**	*Signal: Trip Command*
f[5] . **TripCmd**	*Signal: Trip Command*
f[6] . **TripCmd**	*Signal: Trip Command*
ExP[1] . **TripCmd**	*Signal: Trip Command*
ExP[2] . **TripCmd**	*Signal: Trip Command*
ExP[3] . **TripCmd**	*Signal: Trip Command*
ExP[4] . **TripCmd**	*Signal: Trip Command*

1..n, In-SyncList

Selection list referenced by the following parameters:

- ⮡ SG[1] . Synchronism

1..n, In-SyncList	Description
“-”	*No assignment*
Sync . **Ready to Close**	*Signal: Ready to Close*
DI Slot X1 . **DI 1**	*Signal: Digital Input*
DI Slot X1 . **DI 2**	*Signal: Digital Input*
DI Slot X1 . **DI 3**	*Signal: Digital Input*
DI Slot X1 . **DI 4**	*Signal: Digital Input*
DI Slot X1 . **DI 5**	*Signal: Digital Input*
DI Slot X1 . **DI 6**	*Signal: Digital Input*
DI Slot X1 . **DI 7**	*Signal: Digital Input*
DI Slot X1 . **DI 8**	*Signal: Digital Input*
Logics . **LE1.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE1.Timer Out**	*Signal: Timer Output*
Logics . **LE1.Out**	*Signal: Latched Output (Q)*
Logics . **LE1.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE2.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE2.Timer Out**	*Signal: Timer Output*
Logics . **LE2.Out**	*Signal: Latched Output (Q)*
Logics . **LE2.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE3.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE3.Timer Out**	*Signal: Timer Output*
Logics . **LE3.Out**	*Signal: Latched Output (Q)*
Logics . **LE3.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE4.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE4.Timer Out**	*Signal: Timer Output*
Logics . **LE4.Out**	*Signal: Latched Output (Q)*
Logics . **LE4.Out inverted**	*Signal: Negated Latched Output (Q NOT)*

1..n, In-SyncList	Description
Logics . **LE5.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE5.Timer Out**	*Signal: Timer Output*
Logics . **LE5.Out**	*Signal: Latched Output (Q)*
Logics . **LE5.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE6.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE6.Timer Out**	*Signal: Timer Output*
Logics . **LE6.Out**	*Signal: Latched Output (Q)*
Logics . **LE6.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE7.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE7.Timer Out**	*Signal: Timer Output*
Logics . **LE7.Out**	*Signal: Latched Output (Q)*
Logics . **LE7.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE8.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE8.Timer Out**	*Signal: Timer Output*
Logics . **LE8.Out**	*Signal: Latched Output (Q)*
Logics . **LE8.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE9.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE9.Timer Out**	*Signal: Timer Output*
Logics . **LE9.Out**	*Signal: Latched Output (Q)*
Logics . **LE9.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE10.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE10.Timer Out**	*Signal: Timer Output*
Logics . **LE10.Out**	*Signal: Latched Output (Q)*
Logics . **LE10.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE11.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE11.Timer Out**	*Signal: Timer Output*
Logics . **LE11.Out**	*Signal: Latched Output (Q)*
Logics . **LE11.Out inverted**	*Signal: Negated Latched Output (Q NOT)*

1..n, In-SyncList	Description
Logics . **LE12.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE12.Timer Out**	*Signal: Timer Output*
Logics . **LE12.Out**	*Signal: Latched Output (Q)*
Logics . **LE12.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE13.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE13.Timer Out**	*Signal: Timer Output*
Logics . **LE13.Out**	*Signal: Latched Output (Q)*
Logics . **LE13.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE14.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE14.Timer Out**	*Signal: Timer Output*
Logics . **LE14.Out**	*Signal: Latched Output (Q)*
Logics . **LE14.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE15.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE15.Timer Out**	*Signal: Timer Output*
Logics . **LE15.Out**	*Signal: Latched Output (Q)*
Logics . **LE15.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE16.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE16.Timer Out**	*Signal: Timer Output*
Logics . **LE16.Out**	*Signal: Latched Output (Q)*
Logics . **LE16.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE17.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE17.Timer Out**	*Signal: Timer Output*
Logics . **LE17.Out**	*Signal: Latched Output (Q)*
Logics . **LE17.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE18.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE18.Timer Out**	*Signal: Timer Output*
Logics . **LE18.Out**	*Signal: Latched Output (Q)*
Logics . **LE18.Out inverted**	*Signal: Negated Latched Output (Q NOT)*

1..n, In-SyncList	Description
Logics . **LE19.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE19.Timer Out**	*Signal: Timer Output*
Logics . **LE19.Out**	*Signal: Latched Output (Q)*
Logics . **LE19.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE20.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE20.Timer Out**	*Signal: Timer Output*
Logics . **LE20.Out**	*Signal: Latched Output (Q)*
Logics . **LE20.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE21.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE21.Timer Out**	*Signal: Timer Output*
Logics . **LE21.Out**	*Signal: Latched Output (Q)*
Logics . **LE21.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE22.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE22.Timer Out**	*Signal: Timer Output*
Logics . **LE22.Out**	*Signal: Latched Output (Q)*
Logics . **LE22.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE23.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE23.Timer Out**	*Signal: Timer Output*
Logics . **LE23.Out**	*Signal: Latched Output (Q)*
Logics . **LE23.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE24.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE24.Timer Out**	*Signal: Timer Output*
Logics . **LE24.Out**	*Signal: Latched Output (Q)*
Logics . **LE24.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE25.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE25.Timer Out**	*Signal: Timer Output*
Logics . **LE25.Out**	*Signal: Latched Output (Q)*
Logics . **LE25.Out inverted**	*Signal: Negated Latched Output (Q NOT)*

1..n, In-SyncList	Description
Logics . **LE26.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE26.Timer Out**	*Signal: Timer Output*
Logics . **LE26.Out**	*Signal: Latched Output (Q)*
Logics . **LE26.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE27.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE27.Timer Out**	*Signal: Timer Output*
Logics . **LE27.Out**	*Signal: Latched Output (Q)*
Logics . **LE27.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE28.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE28.Timer Out**	*Signal: Timer Output*
Logics . **LE28.Out**	*Signal: Latched Output (Q)*
Logics . **LE28.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE29.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE29.Timer Out**	*Signal: Timer Output*
Logics . **LE29.Out**	*Signal: Latched Output (Q)*
Logics . **LE29.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE30.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE30.Timer Out**	*Signal: Timer Output*
Logics . **LE30.Out**	*Signal: Latched Output (Q)*
Logics . **LE30.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE31.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE31.Timer Out**	*Signal: Timer Output*
Logics . **LE31.Out**	*Signal: Latched Output (Q)*
Logics . **LE31.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE32.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE32.Timer Out**	*Signal: Timer Output*
Logics . **LE32.Out**	*Signal: Latched Output (Q)*
Logics . **LE32.Out inverted**	*Signal: Negated Latched Output (Q NOT)*

1..n, In-SyncList	Description
Logics . **LE33.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE33.Timer Out**	*Signal: Timer Output*
Logics . **LE33.Out**	*Signal: Latched Output (Q)*
Logics . **LE33.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE34.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE34.Timer Out**	*Signal: Timer Output*
Logics . **LE34.Out**	*Signal: Latched Output (Q)*
Logics . **LE34.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE35.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE35.Timer Out**	*Signal: Timer Output*
Logics . **LE35.Out**	*Signal: Latched Output (Q)*
Logics . **LE35.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE36.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE36.Timer Out**	*Signal: Timer Output*
Logics . **LE36.Out**	*Signal: Latched Output (Q)*
Logics . **LE36.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE37.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE37.Timer Out**	*Signal: Timer Output*
Logics . **LE37.Out**	*Signal: Latched Output (Q)*
Logics . **LE37.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE38.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE38.Timer Out**	*Signal: Timer Output*
Logics . **LE38.Out**	*Signal: Latched Output (Q)*
Logics . **LE38.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE39.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE39.Timer Out**	*Signal: Timer Output*
Logics . **LE39.Out**	*Signal: Latched Output (Q)*
Logics . **LE39.Out inverted**	*Signal: Negated Latched Output (Q NOT)*

1..n, In-SyncList	Description
Logics . **LE40.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE40.Timer Out**	*Signal: Timer Output*
Logics . **LE40.Out**	*Signal: Latched Output (Q)*
Logics . **LE40.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE41.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE41.Timer Out**	*Signal: Timer Output*
Logics . **LE41.Out**	*Signal: Latched Output (Q)*
Logics . **LE41.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE42.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE42.Timer Out**	*Signal: Timer Output*
Logics . **LE42.Out**	*Signal: Latched Output (Q)*
Logics . **LE42.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE43.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE43.Timer Out**	*Signal: Timer Output*
Logics . **LE43.Out**	*Signal: Latched Output (Q)*
Logics . **LE43.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE44.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE44.Timer Out**	*Signal: Timer Output*
Logics . **LE44.Out**	*Signal: Latched Output (Q)*
Logics . **LE44.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE45.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE45.Timer Out**	*Signal: Timer Output*
Logics . **LE45.Out**	*Signal: Latched Output (Q)*
Logics . **LE45.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE46.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE46.Timer Out**	*Signal: Timer Output*
Logics . **LE46.Out**	*Signal: Latched Output (Q)*
Logics . **LE46.Out inverted**	*Signal: Negated Latched Output (Q NOT)*

1..n, In-SyncList	Description
Logics . **LE47.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE47.Timer Out**	*Signal: Timer Output*
Logics . **LE47.Out**	*Signal: Latched Output (Q)*
Logics . **LE47.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE48.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE48.Timer Out**	*Signal: Timer Output*
Logics . **LE48.Out**	*Signal: Latched Output (Q)*
Logics . **LE48.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE49.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE49.Timer Out**	*Signal: Timer Output*
Logics . **LE49.Out**	*Signal: Latched Output (Q)*
Logics . **LE49.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE50.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE50.Timer Out**	*Signal: Timer Output*
Logics . **LE50.Out**	*Signal: Latched Output (Q)*
Logics . **LE50.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE51.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE51.Timer Out**	*Signal: Timer Output*
Logics . **LE51.Out**	*Signal: Latched Output (Q)*
Logics . **LE51.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE52.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE52.Timer Out**	*Signal: Timer Output*
Logics . **LE52.Out**	*Signal: Latched Output (Q)*
Logics . **LE52.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE53.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE53.Timer Out**	*Signal: Timer Output*
Logics . **LE53.Out**	*Signal: Latched Output (Q)*
Logics . **LE53.Out inverted**	*Signal: Negated Latched Output (Q NOT)*

1..n, In-SyncList	Description
Logics . **LE54.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE54.Timer Out**	*Signal: Timer Output*
Logics . **LE54.Out**	*Signal: Latched Output (Q)*
Logics . **LE54.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE55.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE55.Timer Out**	*Signal: Timer Output*
Logics . **LE55.Out**	*Signal: Latched Output (Q)*
Logics . **LE55.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE56.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE56.Timer Out**	*Signal: Timer Output*
Logics . **LE56.Out**	*Signal: Latched Output (Q)*
Logics . **LE56.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE57.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE57.Timer Out**	*Signal: Timer Output*
Logics . **LE57.Out**	*Signal: Latched Output (Q)*
Logics . **LE57.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE58.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE58.Timer Out**	*Signal: Timer Output*
Logics . **LE58.Out**	*Signal: Latched Output (Q)*
Logics . **LE58.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE59.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE59.Timer Out**	*Signal: Timer Output*
Logics . **LE59.Out**	*Signal: Latched Output (Q)*
Logics . **LE59.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE60.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE60.Timer Out**	*Signal: Timer Output*
Logics . **LE60.Out**	*Signal: Latched Output (Q)*
Logics . **LE60.Out inverted**	*Signal: Negated Latched Output (Q NOT)*

1..n, In-SyncList	Description
Logics . **LE61.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE61.Timer Out**	*Signal: Timer Output*
Logics . **LE61.Out**	*Signal: Latched Output (Q)*
Logics . **LE61.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE62.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE62.Timer Out**	*Signal: Timer Output*
Logics . **LE62.Out**	*Signal: Latched Output (Q)*
Logics . **LE62.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE63.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE63.Timer Out**	*Signal: Timer Output*
Logics . **LE63.Out**	*Signal: Latched Output (Q)*
Logics . **LE63.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE64.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE64.Timer Out**	*Signal: Timer Output*
Logics . **LE64.Out**	*Signal: Latched Output (Q)*
Logics . **LE64.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE65.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE65.Timer Out**	*Signal: Timer Output*
Logics . **LE65.Out**	*Signal: Latched Output (Q)*
Logics . **LE65.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE66.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE66.Timer Out**	*Signal: Timer Output*
Logics . **LE66.Out**	*Signal: Latched Output (Q)*
Logics . **LE66.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE67.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE67.Timer Out**	*Signal: Timer Output*
Logics . **LE67.Out**	*Signal: Latched Output (Q)*
Logics . **LE67.Out inverted**	*Signal: Negated Latched Output (Q NOT)*

1..n, In-SyncList	Description
Logics . **LE68.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE68.Timer Out**	*Signal: Timer Output*
Logics . **LE68.Out**	*Signal: Latched Output (Q)*
Logics . **LE68.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE69.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE69.Timer Out**	*Signal: Timer Output*
Logics . **LE69.Out**	*Signal: Latched Output (Q)*
Logics . **LE69.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE70.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE70.Timer Out**	*Signal: Timer Output*
Logics . **LE70.Out**	*Signal: Latched Output (Q)*
Logics . **LE70.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE71.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE71.Timer Out**	*Signal: Timer Output*
Logics . **LE71.Out**	*Signal: Latched Output (Q)*
Logics . **LE71.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE72.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE72.Timer Out**	*Signal: Timer Output*
Logics . **LE72.Out**	*Signal: Latched Output (Q)*
Logics . **LE72.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE73.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE73.Timer Out**	*Signal: Timer Output*
Logics . **LE73.Out**	*Signal: Latched Output (Q)*
Logics . **LE73.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE74.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE74.Timer Out**	*Signal: Timer Output*
Logics . **LE74.Out**	*Signal: Latched Output (Q)*
Logics . **LE74.Out inverted**	*Signal: Negated Latched Output (Q NOT)*

1..n, In-SyncList	Description
Logics . **LE75.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE75.Timer Out**	*Signal: Timer Output*
Logics . **LE75.Out**	*Signal: Latched Output (Q)*
Logics . **LE75.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE76.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE76.Timer Out**	*Signal: Timer Output*
Logics . **LE76.Out**	*Signal: Latched Output (Q)*
Logics . **LE76.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE77.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE77.Timer Out**	*Signal: Timer Output*
Logics . **LE77.Out**	*Signal: Latched Output (Q)*
Logics . **LE77.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE78.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE78.Timer Out**	*Signal: Timer Output*
Logics . **LE78.Out**	*Signal: Latched Output (Q)*
Logics . **LE78.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE79.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE79.Timer Out**	*Signal: Timer Output*
Logics . **LE79.Out**	*Signal: Latched Output (Q)*
Logics . **LE79.Out inverted**	*Signal: Negated Latched Output (Q NOT)*
Logics . **LE80.Gate Out**	*Signal: Output of the logic gate*
Logics . **LE80.Timer Out**	*Signal: Timer Output*
Logics . **LE80.Out**	*Signal: Latched Output (Q)*
Logics . **LE80.Out inverted**	*Signal: Negated Latched Output (Q NOT)*

LE1.Gate

Logic gate

Selection list referenced by the following parameters:

- ⮡ Logics . LE1.Gate

LE1.Gate	Description
AND	*AND Gate*
OR	*OR Gate*
NAND	*NAND Gate*
NOR	*NOR Gate*

Mode

general operation mode

Selection list referenced by the following parameters:

- ⮡ BO Slot X2 . Disarm Mode
- ⮡ BO Slot X2 . Force Mode

Mode	Description
permanent	*permanent*
timeout	*timeout*

active/inactive

Selection list referenced by the following parameters:

- ⮡ BO Slot X2 . DISARMED

active/inactive	Description
inactive	*inactive*
active	*active*

Relay operating modes

Selection list referenced by the following parameters:

- ⮡ BO Slot X2 . Force all Outs
- ⮡ BO Slot X2 . Force OR1

Relay operating modes	Description
Normal	*Normal*
De-Energized	*De-Energized*
Energized	*Energized*

State

Selection list referenced by the following parameters:

- ⮡ Sgen . State

State	Description
Off	*Off*
PreFault	*Pre Fault Duration*
FaultSimulation	*Duration of Fault Simulation*
PostFault	*Post Fault Duration*
Init Res	*Init Reset*

TripCmd Mode

Trip Command Mode: Select between two operating modes for the Fault Simulator: "cold simulation” (without tripping the circuit breaker), or "hot simulation” (i.e. the simulation is authorized to trip the circuit breaker)

Selection list referenced by the following parameters:

- ⮡ Sgen . TripCmd Mode

TripCmd Mode	Description
No TripCmd	*No Trip Command: The TripCmd of all protection functions is blocked. The protection function will possibly trip but not generate a TripCmd.*
With TripCmd	*With Trip Command: The trip of a protection function generates a TripCmd, that can open the circuit breaker.*

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